

DM54LS491A/DM74LS491A 10-Bit Counter

General Description

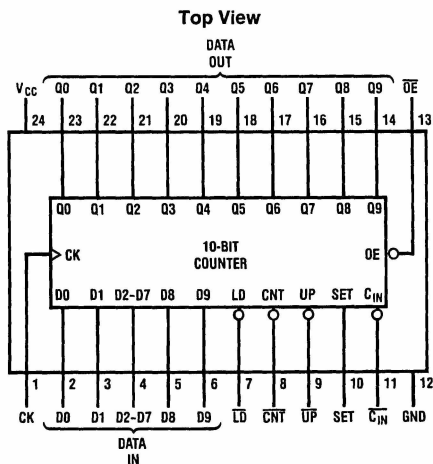
The ten-bit counter can count up, count down, set, and load 2 LSB's, 2 MSB's and 6 middle bits high or low as a group. All operations are synchronous with the clock. SET overrides LOAD, COUNT and HOLD. LOAD overrides COUNT. COUNT is conditional on C_{IN} , otherwise it holds.

All outputs are enabled when OE is low, otherwise HIGH-Z. The 24 mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Features

- CRT vertical and horizontal timing generation
- Bus-structured pinout
- Low current PNP inputs reduce loading
- TRI-STATE® outputs
- 24-pin SKINNYDIP saves space

Connection Diagram



TL/L/10222-1

Order Number DM54LS491AJ, DM74LS491AJ, DM74LS491AN or DM74LS491AV
See NS Package Number J24F, N24C or V28A

Function Table

$\overline{OE}$	CK	SET	LD	$\overline{CNT}$	C_{IN}	$\overline{UP}$	D9-D0	Q9-Q0	Operation
H	X	X	X	X	X	X	X	Z	Hi-Z
L	$\uparrow$	H	X	X	X	X	X	H	Set all HIGH
L	$\uparrow$	L	L	X	X	X	D	D	LOAD D
L	$\uparrow$	L	H	H	X	X	X	Q	HOLD
L	$\uparrow$	L	H	L	H	X	X	Q	HOLD
L	$\uparrow$	L	H	L	L	L	X	Q Plus 1	Count Up
L	$\uparrow$	L	H	L	L	H	X	Q Minus 1	Count Down

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C

ESD Tolerance

> 1000V

Czap = 100 pF

Rzap = 1500Ω

Test Method: Human Body Model

Test Specification: NSC SOP 5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55	25		0	25	75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Series 24A Over Recommended Operating Temperature Range

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	(Note 2)		2			V
V_{IL}	Low Level Input Voltage	(Note 2)				0.8	V
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18 \text{ mA}$			−0.8	−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}$ $V_{IL} = 0.8 \text{ V}$ $V_{IH} = 2 \text{ V}$	$I_{OH} = -2 \text{ mA}$ MIL $I_{OH} = -3.2 \text{ mA}$ COM	2.4	2.9		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$ $V_{IL} = 0.8 \text{ V}$ $V_{IH} = 2 \text{ V}$	$I_{OL} = 12 \text{ mA}$ MIL $I_{OL} = 24 \text{ mA}$ COM		0.3	0.5	V
I_{OZH}	Off-State Output Current (Note 3)	$V_{CC} = \text{Max}$ $V_{IL} = 0.8 \text{ V}$ $V_{IH} = 2 \text{ V}$	$V_O = 2.4 \text{ V}$			100	μA
I_{OZL}			$V_O = 0.4 \text{ V}$			−100	μA
I_I	Maximum Input Current	$V_{CC} = \text{Max}$, $V_I = 5.5 \text{ V}$				1	mA
I_{IH}	High Level Input Current (Note 3)	$V_{CC} = \text{Max}$, $V_I = 2.4 \text{ V}$				25	μA
I_{IL}	Low Level Input Current (Note 3)	$V_{CC} = \text{Max}$, $V_I = 0.4 \text{ V}$			−0.04	−0.25	mA
I_{OS}	Output Short-Circuit Current	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$ (Note 4)	−30	−70	−130	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$			135	180	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

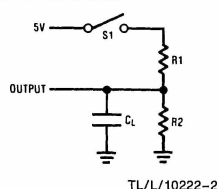
Note 3: I/O leakage as the worst case of I_{OZX} or I_{IX} , e.g., I_{IL} and I_{OZL} .

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Recommended Operating Conditions

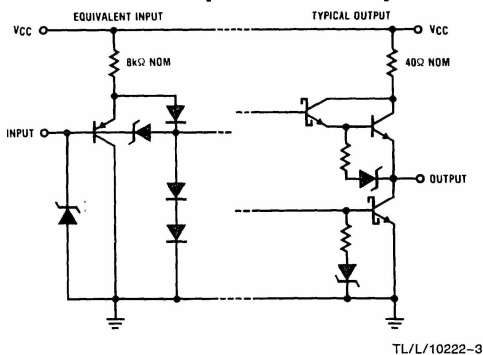
Symbol	Parameter	Test Condition	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
t_S	Setup Time from Input		40	20		30	20		ns
t_W	Width of Clock	High	20	7		15	7		ns
		Low	35	15		25	15		ns
t_H	Hold Time		0	-15		0	-15		ns
t_{CLK}	Clock to Output	$C_L = 50 \text{ pF}$		10	25		10	15	ns
t_{pzx}	Output Enable Delay	$C_L = 50 \text{ pF}$		19	35		19	30	ns
t_{pxz}	Output Disable Delay	$C_L = 5 \text{ pF}$		15	35		15	30	ns
f_{MAX}	Maximum Frequency		15.3	32		22.2	32		MHz

Test Load

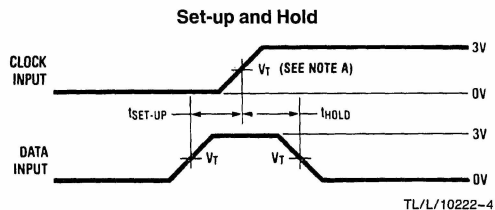


MIL	COM'L
$R1 = 390$	$R1 = 200$
$R2 = 750$	$R2 = 390$

Schematic of Inputs and Outputs



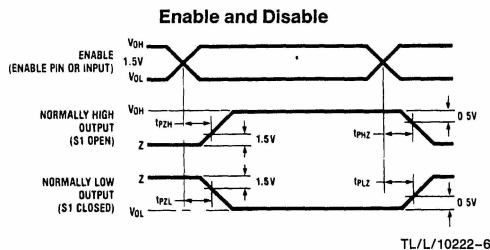
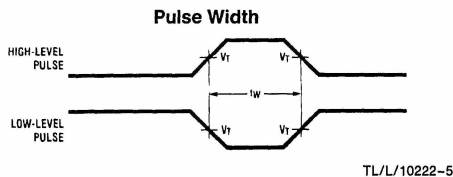
Test Waveforms



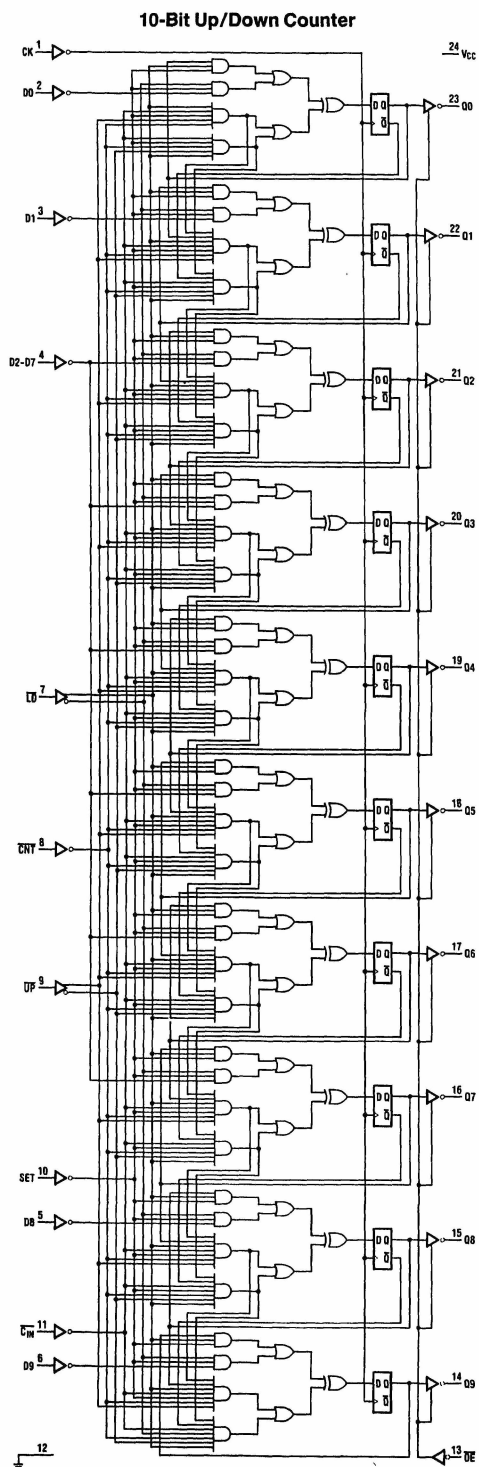
Note A: $V_T = 1.5V$.

Note B: C_L includes probe and jig capacitance.

Note B: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.



Logic Diagram



TL/L/10222-7