National Semiconductor

DM54LS498A/DM74LS498A Octal Shift Register

General Description

The LS498A is an 8-bit synchronous shift register with parallel load and hold capability. Two function-select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7–D0) into the output register (Q7–Q0). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register Q, one bit to the left; Q0 is replaced by LIRO. LIRO outputs Q0.

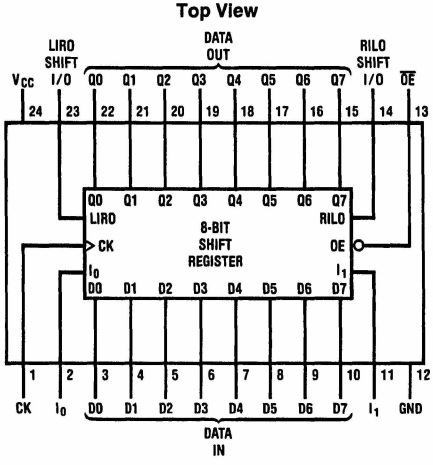
The output register (Q7–Q0)—is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application.

Features

- Octal shift register for serial to parallel and parallel to serial applications
- 8 bits match byte boundaries
- Low current PNP inputs reduce loading
- Bus-structured pinout
- TRI-STATE® outputs
- 24-pin SKINNYDIP saves space
- Expandable in 8-bit increments

Connection Diagram



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Order Number DM54LS498AJ, DM74LS498AJ, DM74LS498AN or DM74LS498AV
See NS Package Number J24F, N24C or V28A

Function Table

$\overline{OE}$	CK	I1	I0	D7–D0	Q7–Q0	Operation
H	X	X	X	X	Z	HI-Z
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C
ESD Tolerance	>1000V
Czap = 100 pF	
Rzap = 1500Ω	
Test Method: Human Body Model	
Test Specification: NSC SOP 5-028	

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55	25		0	25	75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Series 24A Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	(Note 2)		2			V
V_{IL}	Low Level Input Voltage	(Note 2)				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2 mA MIL	2.4	2.9		V
			I_{OH} = −3.2 mA COM				
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 12 mA MIL		0.3	0.5	V
			I_{OL} = 24 mA COM				
I_{OZH}	Off-State Output Current (Note 3)	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.4V			100	μA
I_{OZL}			V_O = 0.4V			−100	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = Max, V_I = 2.4V				25	μA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = Max, V_I = 0.4V			−0.04	−0.25	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	V_O = 0V (Note 4)	−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max			135	180	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

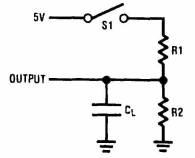
Note 3: I/O leakage as the worst case of IOZX or IIX, e.g., I_{IL} and IOZL.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Operating Conditions

Symbol	Parameter		Test Conditions	Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
T_S	Setup Time from Input			40	20		30	20		ns
T_W	Width of Clock	High		20	7		15	7		ns
		Low		35	15		25	15		ns
T_{PD}	I0, I1 to LIRO, RILO		C_L = 50 pF		23	35		23	30	ns
T_{CLK}	Clock to Output		C_L = 50 pF		10	25		10	15	ns
T_{PZX}	Output Enable Delay		C_L = 50 pF		19	35		19	30	ns
T_{PX}	Output Disable Delay		C_L = 5 pF		15	35		15	30	ns
T_H	Hold Time			0	−15		0	−15		ns
f_{MAX}	Maximum Frequency			15.3	32		22.2	32		MHz

Test Load



MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

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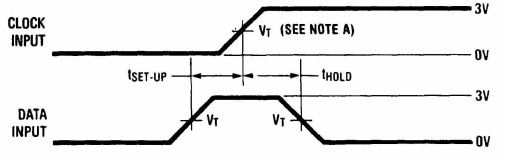
Test Waveforms

Set-Up and Hold



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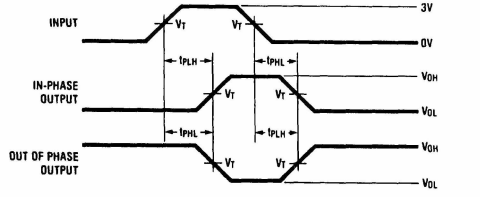
Propagation Delay



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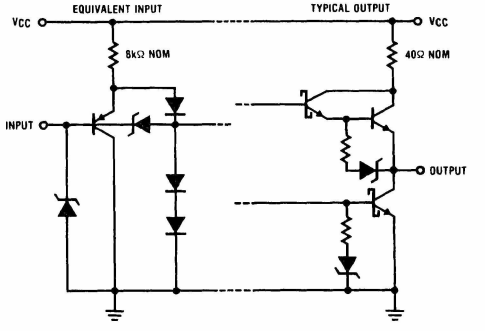
Note A: V_T = 1.5V.

Note B: C_L includes probe and jig capacitance.

Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Schematic of Inputs and Outputs



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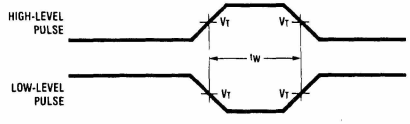
Pulse Width



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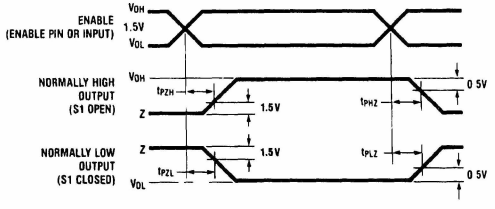
Enable and Disable



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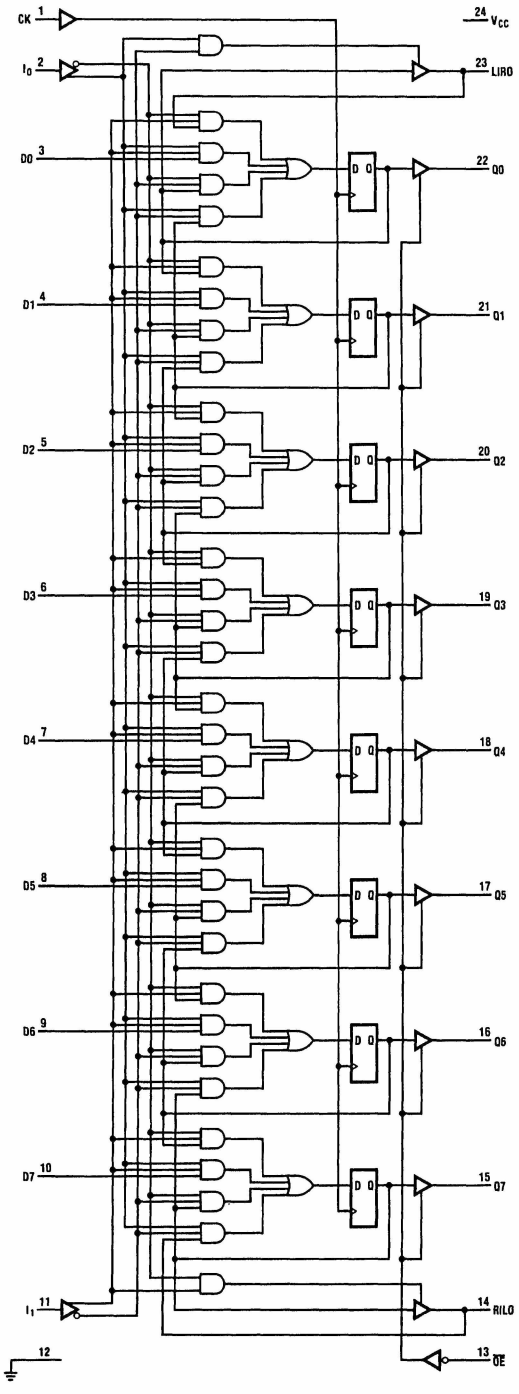
Logic Diagram

Octal Shift Register



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