National Semiconductor

54LS502/DM74LS502
8-Bit Successive Approximation Register

General Description

The LS502 is an 8-bit register with the interstage logic necessary to perform serial-to-parallel conversion and provide an active LOW Conversion Complete ($\overline{CC}$) signal coincident with storage of the eighth bit. An active LOW Start ($\overline{S}$) input performs synchronous initialization which forces Q7 LOW and all other outputs HIGH. Subsequent clocks shift this Q7 LOW signal downstream which simultaneously backfills the register such that the first serial data (D input) bit is stored in Q7, the second bit in Q6, the third in Q5, etc. The serial input data is also synchronized by an auxiliary flip-flop and brought out on Q_D.

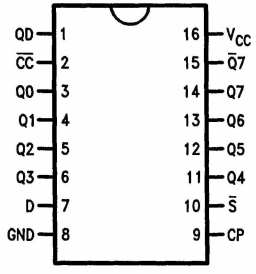
Designed primarily for use in the successive approximation technique for analog-to-digital conversion, the LS502 can also be used as a serial-to-parallel converter ring counter and as the storage and control element in recursive digital routines.

Features

- Low power Schottky version of 2502
- Storage and control for successive approximation A to D conversion
- Performs serial-to-parallel conversion

Connection Diagram

Dual-In-Line Package



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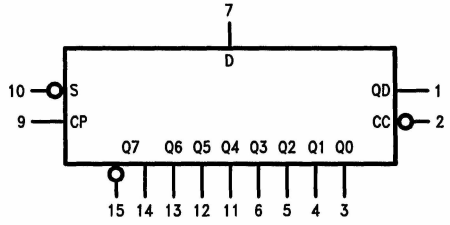
Order Number 54LS502DMQB, 54LS502FMQB, DM74LS502WM or DM74LS502N
See NS Package Number J16A, M16B, N16E or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
D	Serial Data Input
$\overline{S}$	Start Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q_D	Synchronized Serial Data Output
$\overline{CC}$	Conversion Complete Output (Active LOW)
Q0–Q7	Parallel Register Outputs
$\overline{Q7}$	Complement of Q7 Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS502			DM74LS502			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW $\overline{S}$ to CP	5 5			5 5			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW $\overline{S}$ to CP	5 5			5 5			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW D to CP	5 5			5 5			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D to CP	5 5			5 5			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	20 20			20 20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V, T_A = +25°C$ (See Section 1 for test waveforms and output loads)

Symbol	Parameter	$R_L = 2\,k\Omega, C_L = 15\,pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	25		MHz
t_{PLH}	Propagation Delay		35	ns
t_{PHL}	CP to Q_n or $\overline{CC}$		25	

Functional Description

The register stages are composed of transparent RS latches arranged in master/slave pairs. The master and slave latches are enabled separately by non-overlapping complementary signals $\phi 1$ and $\phi 2$ derived internally from the CP input. Master latches are enabled when CP is LOW and slave latches are enabled when CP is HIGH. Information is transferred from master to slave, and thus to the outputs, by the LOW-to-HIGH transition of CP.

Initializing the register requires a LOW signal on $\overline{S}$ while exercising CP. With $\overline{S}$ and CP LOW, all master latches are SET (Q side HIGH). A LOW-to-HIGH CP transition, with $\overline{S}$ remaining LOW, then forces the slave latches to the condition wherein Q7 is LOW and all other register outputs, including $\overline{CC}$, are HIGH. This condition will prevail as long as $\overline{S}$ remains LOW, regardless of subsequent CP rising edge. To start the conversion process, $\overline{S}$ must return to the HIGH state. On the next CP rising edge, the information stored in the serial data input latch is transferred to Q_D and Q7, while Q6 is forced to the LOW state. On the rising edge of the next seven clocks, this LOW signal is shifted downstream, one bit at a time, while the serial data enters the register position one bit behind this LOW signal, as shown in the Truth Table. Note that after a serial data bit appears at a particular output, that register position undergoes no further changes. After the shifted LOW signal reaches $\overline{CC}$, the register is locked up and no further changes can occur until the register is initialized for the next conversion process.

Figure a shows a simplified hook-up of a LS502, a D/A converter and a comparator arranged to convert an analog input voltage into an 8-bit binary number by the successive approximation technique. *Figure b* is an idealized graph showing the various values that the D/A converter output voltage can assume in the course of the conversion. The vertical axis is calibrated in fractions of the full-scale output capability of the D/A converter and the horizontal axis represents the successive states of the Truth Table. At time t1, Q7 is LOW and Q6–Q0 are HIGH, causing the D/A output to be one-half of full scale. If the analog input voltage is greater than this voltage the comparator output (hence the D input of the LS502) will be LOW, and at times t2 the D/A output will rise to three-fourths of full scale because Q7 will remain LOW and contribute 50% while Q6 is forced LOW and contributes another 25%. On the other hand, if the analog input voltage is less than one-half of full scale, the comparator output will be HIGH and Q7 will go HIGH at t2. Q6 will still be forced LOW at t2, and the D/A output will decrease to 25% of full scale. Thus with each successive clock, the D/A output will change by smaller increments. When the conversion is completed at t9, the binary number represented by the register outputs will be the numerator of the fraction n/256, representing the analog input voltage as a fraction of the full scale output D/A converter.

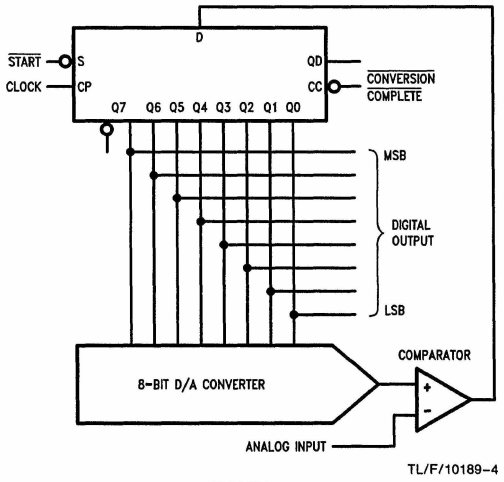

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FIGURE a.

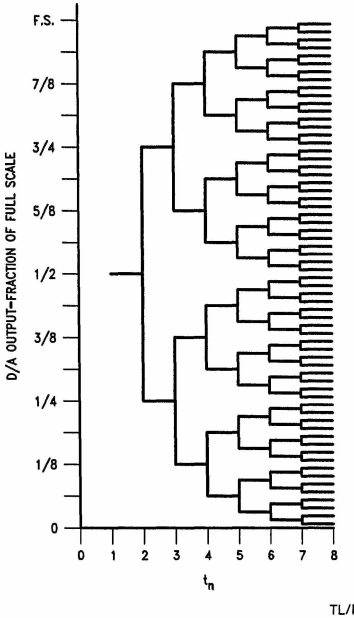

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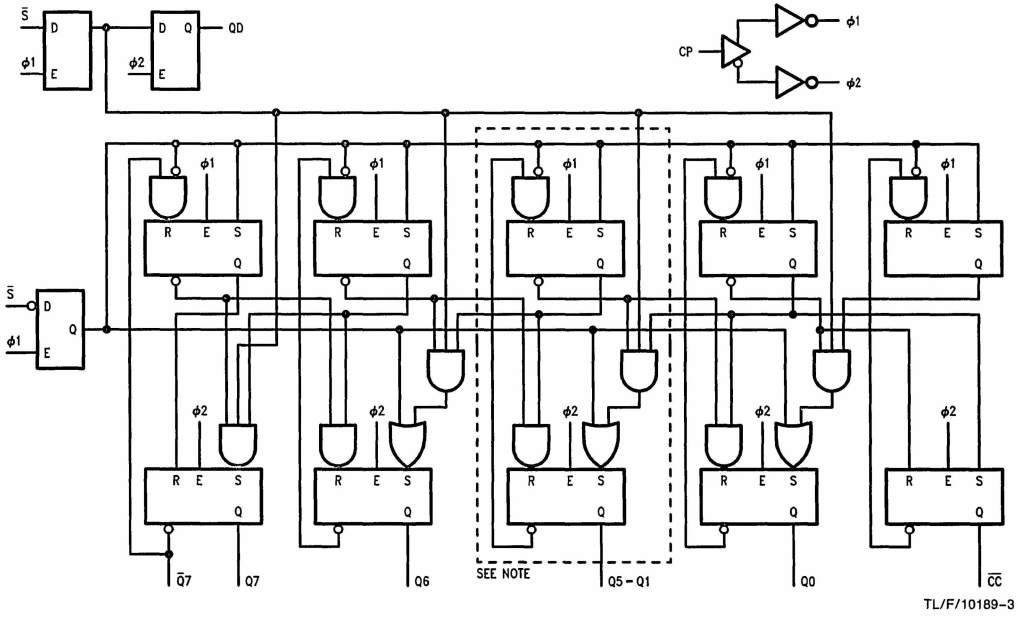
FIGURE b.

Truth Table

Time	Inputs		Outputs									
t_n	D	$\overline{S}$	Q_D	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	X	L	H	H	H	H	H	H	H	H
2	D6	H	D7	D7	L	H	H	H	H	H	H	H
3	D6	H	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	H	X	D7	D6	D5	D4	D3	D2	D1	D0	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Note: Cell logic is repeated for register stages Q5 to Q1.