National Semiconductor

DM74LS574
Octal D-Type Flip-Flop (with TRI-STATE® Outputs)

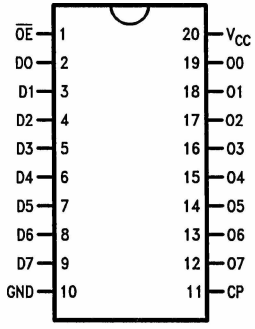
General Description

The 'LS574 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'LS374 except for the pinouts.

Connection Diagram

Dual-In-Line Package



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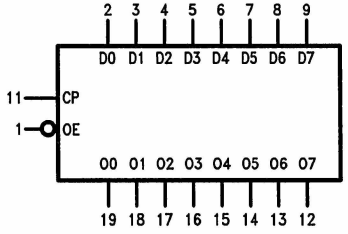
Order Number DM74LS574WM or DM74LS574N
See NS Package Number M20B or N20A

Logic Symbol



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V_{CC} = Pin 20
GND = Pin 10

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions $V_{CC} = +5.0V, T_A = +25°C$

Symbol	Parameter	DM74LS574			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Dn to CP	20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Dn to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−20	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit (Note 2) Output Current	V_{CC} = Max	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for test waveforms and output load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 45 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to On		28 28	ns
t_{PZH} t_{PZL}	Output Enable Time		28 28	ns
t_{PHZ} t_{PLZ}	Output Disable Time		20 25	ns

Functional Description

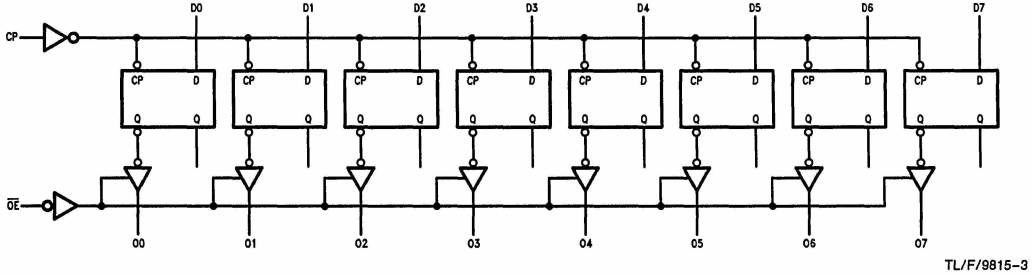
The LS574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Outputs Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedence state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs		Outputs	
Dn	CP	OE	On
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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