National Semiconductor

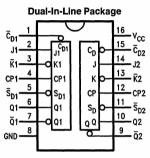
DM74S109 Dual JK Positive **Edge-Triggered Flip-Flop**

General Description

S109

This device consists of two high speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to 'S74 data sheet) by connecting the J and \overline{K} inputs together.

Connection Diagram



Order Number DM74S109N See NS Package Number N16E

Truth Table

Inputs		Outputs		
@ t _n		@ t _n + 1		
J	к	Q	Q	
L	н	No Change		
L	L	L	н	
н	н	н	L	
н	L	Toggles		

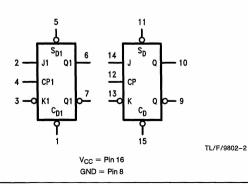
 t_{Π} = Bit time before clock pulse

tn +1 = Bit time after clock pulse

H = HIGH Voltage Level

L = LOW Voltage Level

Logic Symbol



TL/F/9802-1

Asynchronous Inputs:

LOW input to SD sets Q to HIGH level LOW input to \overline{C}_D sets Q to LOW level Clear and Set are independent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and Q HIGH

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM74S	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation

Recommended Operating Conditions

Symbol	Parameter	DM74S109			Units
		Min	Nom	Max	
V _{CC}	Supply Voltage	4.75	5	5.25	v
V _{IH}	High Level Input Voltage	2			v
VIL	Low Level Input Voltage			0.8	v
I _{OH}	High Level Output Current			-1	mA
lol	Low Level Output Current			20	mA
T _A	Free Air Operating Temperature	0		70	°C
t _s (H) t _s (L)	Setup Time J_n or \overline{K}_n to CP _n	6.0 6.0			ns
t _h (H) t _h (L)	Hold Time J_n or \overline{K}_n to CP_n	0 0			ns
t _w (H) t _w (L)	CP _n Pulse Width	7.0 6.5			ns
t _w (L)	\overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width LOW	6.0			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min$, $I_I = -18 \text{ mA}$			-1.2	v
V _{OH}	High Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max$	2.7	3.4		v
V _{OL}	Low Level Output Voltage	$V_{CC} = Min$, $I_{OL} = Max$ $V_{IH} = Min$		0.35	0.5	v
łı	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$			1	mA
IIH	High Level Input Current	$V_{CC} = Max, V_1 = 2.7V$			50	μΑ
կլ	Low Level Input Current	$V_{CC} = Max, V_1 = 0.5V$			-2.0	mA
los	Short Circuit Output Current	V _{CC} = Max (Note 2)	-40		-100	mA
ICC	Supply Current	V _{CC} = Max V _{CP} = 0V			52	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

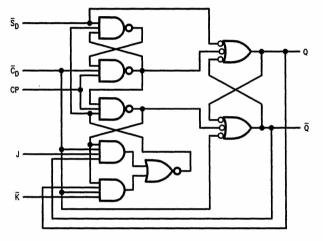
Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25^{\circ}C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	CL = RL =	Units	
		Min	Max	
f _{max}	Maximum Clock Frequency	75		MHz
t _{PLH} t _{PHL}	Propagation Delay CP_n to Q_n or \overline{Q}_n		9.0 11	ns
t _{PLH} t _{PHL}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n		6.0 11	ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Logic Diagram (one half shown)



TL/F/9802-3