DM7093/DM8093 tri-state quad buffers
DM7094/DM8094 tri-state quad buffers

general description

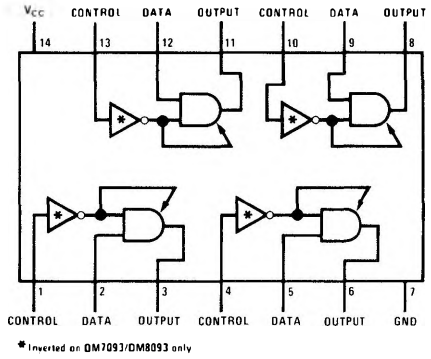
The DM7093/DM8093 and DM7094/DM8094 are quad 2-input buffers which accept normal TTL or DTL input levels and have outputs which provide either normal low-impedance TTL output characteristics or a high impedance state. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state. The other input simply passes the non-inverted data through the buffer. The DM7093/DM8093 and DM7094/DM8094 differ only in the activating logic state of the control input. The DM7093/DM8093 provides the high impedance state when a logical "1" is applied to the control input; the DM7094/DM8094 operates similarly with a logical "0". Features of these buffers include:

- Series 54/74 TTL and 930 DTL Compatible
- Same Pin Breakout as SN5400/SN7400 TTL and 946 DTL
- Up to 128 Buffers can be Connected to a Common Bus-Line
- 12 ns Propagation Delay
- High Capacitive Drive Capability
- Independent Control of each Buffer

This unique tri-state concept allows outputs to be tied together and then connected to a common bus line. Normal TTL outputs cannot be connected due to the low-impedance logical "1" output current which one device would have to sink from the other. If however on all but one of the connected devices both the upper and lower output transistors are turned off, then the one remaining device in the normal low impedance state will have to supply to or sink from the other devices only a small amount of leakage current. This is exactly what occurs on the DM7093/DM8093 and DM7094/DM8094.

(Continued on page 17)

logic and connection diagram



truth tables

DM7093/DM8093

DATA	CONTROL	OUTPUT
1	0	1
0	0	0
X	1	Hi-Z

X = Irrelevant

DM7094/DM8094

DATA	CONTROL	OUTPUT
1	1	1
0	1	0
X	0	Hi-Z

X = Irrelevant

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Time that two bus-connected devices may be in opposite low impedance states simultaneously (5% duty cycle)	10 msec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7093, DM7094	−55°C to +125°C
DM8093, DM8094	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETERS		CONDITIONS	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
Input Clamp Voltage	DM7093/94	V_{CC} = 4.5V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
	DM8093/94	V_{CC} = 4.75V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	DM7093/94	V_{CC} = 4.5V	2.0			V
	DM8093/94	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM7093/94	V_{CC} = 4.5V			0.8	V
	DM8093/94	V_{CC} = 4.75V			0.8	V
Logical "1" Input Current	DM7093/94	V_{CC} = 5.5V, V_{IN} = 2.4V			40	µA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 2.4V			40	µA
Logical "1" Input Current	DM7093/94	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current (Control Input Only)	DM7093/94	V_{CC} = 5.5V, V_{IN} = 0.4V			−1.6	mA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 0.4V			−1.6	mA
Logical "0" Input Current (Data Input Only)	DM7093/94	V_{CC} = 5.5V, V_{IN} = 0.4V, $V_{CONTROL}$ = 2.0V (DM7093/8093) 0.8V (DM7094/8094)			−40	µA
		V_{CC} = 5.5V, V_{IN} = 0.4V, $V_{CONTROL}$ = 0.8V (DM7093/8093) 2.0V (DM7094/8094)			−1.6	mA
	DM8093/94	V_{CC} = 5.25V, V_{IN} = 0.4V, $V_{CONTROL}$ = 2.0V (DM7093/8093) 0.8V (DM7094/8094)			−40	µA
		V_{CC} = 5.25V, V_{IN} = 0.4V, $V_{CONTROL}$ = 0.8V (DM7093/8093) 2.0V (DM7094/8094)			−1.6	mA
Logical "1" Output Voltage	DM7093/94	V_{CC} = 4.5V, I_o = −2.0 mA	2.4	3.3		V
	DM8093/94	V_{CC} = 4.75V, I_o = −5.2 mA	2.4	3.3		V
Logical "0" Output Voltage	DM7093/94	V_{CC} = 4.5, I_o = 16 mA		.23	0.4	V
	DM8093/94	V_{CC} = 4.75, I_o = 16 mA		.23	0.4	V
Output Short Current (Note 2)	DM7093/94	V_{CC} = 5.5V, V_o = 0V	−30	−45	−70	mA
	DM8093/94	V_{CC} = 5.25V, V_o = 0V	−28	−45	−70	mA
Supply Current	DM7093	V_{CC} = 5.5V		32	54	mA
	DM8093	V_{CC} = 5.25V		32	54	mA
Supply Current	DM7094	V_{CC} = 5.5V		36	62	mA
	DM8094	V_{CC} = 5.25V		36	62	mA
Output Disable Current	DM7093/94	V_{CC} = 5.5V, V_o = 2.4V			40	µA
		V_{CC} = 5.5V, V_o = 0.4V			−40	µA
	DM8093/94	V_{CC} = 5.25V, V_o = 2.4V			40	µA
		V_{CC} = 5.25V, V_o = 0.4V			−40	µA
V_{CC} Clamp		V_{CC} = 0V, I_o = 12 mA			1.5	V
Ground Clamp		V_{CC} = 0V, I_o = −12 mA			−1.5	V
t_{pd1}	DM7093/8093	V_{CC} = 5.0V, T_A = 25°C		12	23	ns
	DM7094/8094	V_{CC} = 5.0V, T_A = 25°C		12	23	ns
t_{pd0}	DM7093/8093	V_{CC} = 5.0V, T_A = 25°C		12	18	ns
	DM7094/8094	V_{CC} = 5.0V, T_A = 25°C		12	18	ns
t_{1H}	DM7093/8093	V_{CC} = 5.0V, T_A = 25°C		5	10	ns
	DM7094/8094	V_{CC} = 5.0V, T_A = 25°C		12	18	ns
t_{0H}	DM7093/8093	V_{CC} = 5.0V, T_A = 25°C		14	24	ns
	DM7094/8094	V_{CC} = 5.0V, T_A = 25°C		18	29	ns
t_{H1}	DM7093/8093	V_{CC} = 5.0V, T_A = 25°C		14	21	ns
	DM7094/8094	V_{CC} = 5.0V, T_A = 25°C		14	21	ns
t_{H0}	DM7093/8093	V_{CC} = 5.0V, T_A = 25°C		13	25	ns
	DM7094/8094	V_{CC} = 5.0V, T_A = 25°C		13	25	ns

NOTE 1: Unless otherwise specified the min-max limits across the −55°C to +125°C temperature range for the DM7093 & DM7094 and across the 0°C to 70°C temperature range for the DM8093 & DM8094. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

NOTE 2: Only one output at a time should be shorted.

NOTE 3: MIN and MAX values refer to the absolute values.

general description (cont.)

A typical system connection is shown in Figure 1. While true that in a TTL system open-collector gates could be used to perform the logic function of these tri-state elements, neither waveform integrity nor optimum speed would be achieved. The low output impedance of the DM7093/DM8093 and DM7094/DM8094 provides good capacitance drive capability and rapid transition from the logical "0" to logical "1" level thus assuring both speed and waveform integrity.

It is possible to connect as many as 128 devices to a common bus-line and still have adequate drive capability to allow fan-out from the bus. The example shown in Figure 2 indicates how this guarantee can be made under worst-case conditions.

Another advantage of these buffers is that in the high impedance state their inputs do not present the normal loading to the driving device. This is significant when it is desirable to transmit in both directions over a common line. Figure 3 illustrates such a system. Assume one device in group A is driving the bus-line; and the gates at B are receiving the signals. All outputs at C and D are gated into the high-impedance state. Normally the fan-out from the driving gate at A would be calculated at 4–2 from B and 2 from D, plus additional slight loading from those outputs in the high impedance state. But since the logical "0" input current on D's inputs deliver only 40 μA when these devices are gated into the high impedance state, the loading is significantly reduced. It's true that the logical "1" fan-out remains the same (40 μA times the number of inputs and high-impedance-state outputs). However since the logical "1" fan-out capability of these tri-state devices is 130 while the logical "0" fan-out capability is only 10, it is obvious that the logical "0" fan-out is the limiting item and that a significant increase in the number of inputs which can be tied to the bus-line can be achieved by reducing the number of ~1.6 mA logical "0" loads.

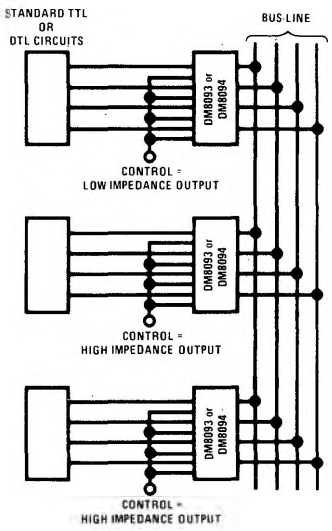


FIGURE 1

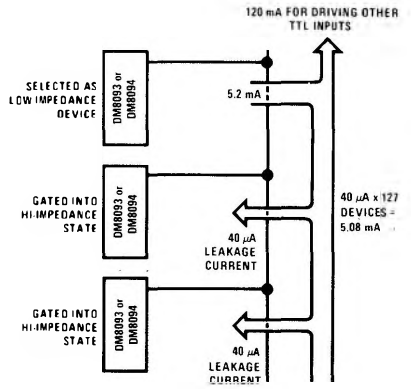


FIGURE 2

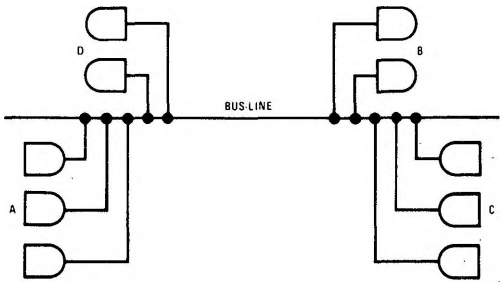
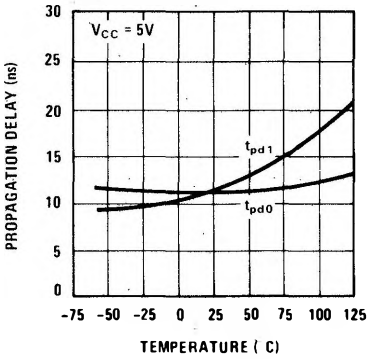


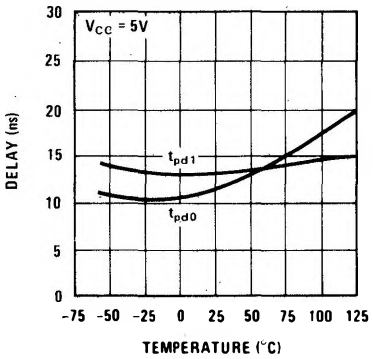
FIGURE 3

typical performance

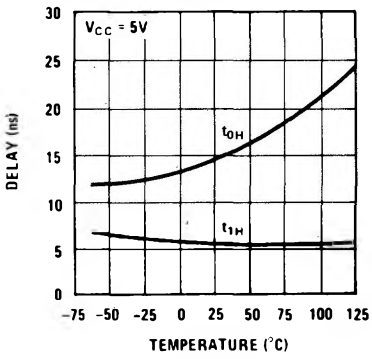
Propagation Delay vs Temperature (DM7093/DM8093)



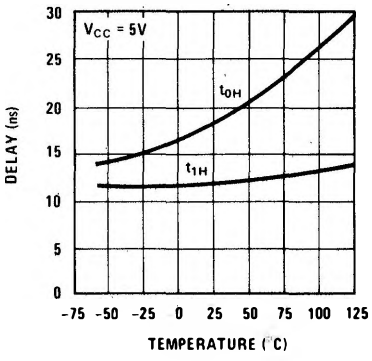
Propagation Delay vs Temperature (DM7094/DM8094)



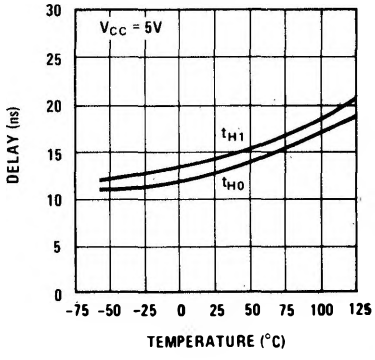
Delay From Control to High Impedance State (DM7093/DM8093)



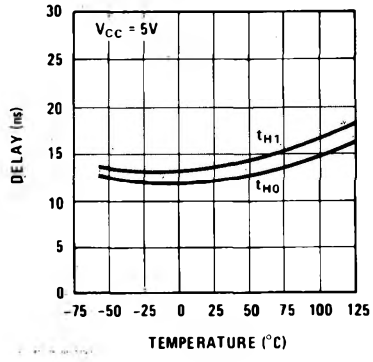
Delay from Control to High Impedance State (DM7094/DM8094)



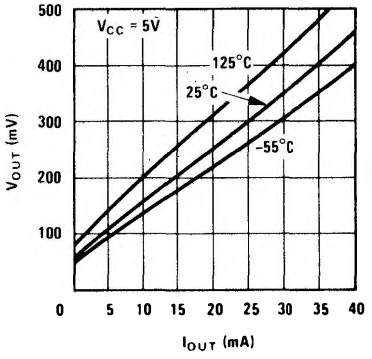
Delay from Control to Low Impedance State (DM7093/DM8093)



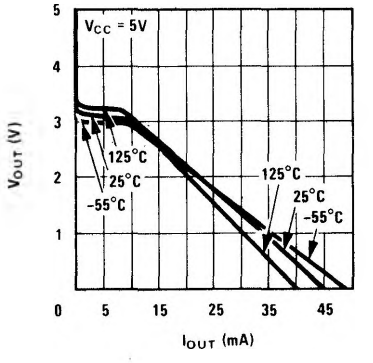
Delay from Control to Low Impedance State (DM7094/DM8094)



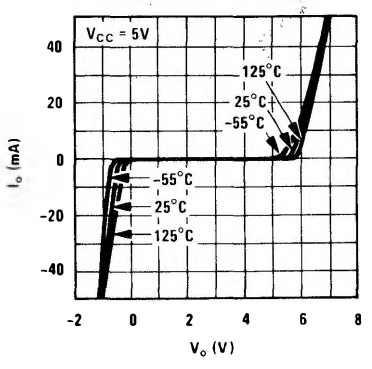
Logical "0" Output Voltage vs Sink Current



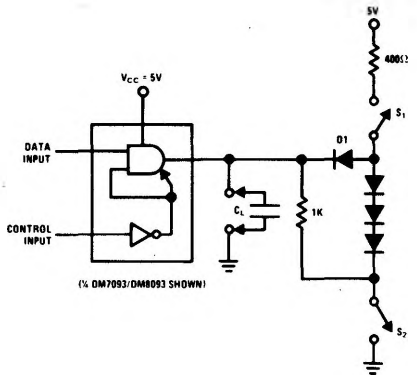
Logical "1" Output Voltage vs Source Current



I_{OUT} vs V_{OUT} (High Impedance Output State)



ac test circuit



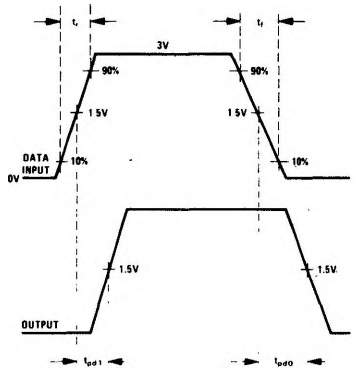
	S_1	S_2	C_L
t_{pd1}	CLOSED	CLOSED	50 pF
t_{pd0}	CLOSED	CLOSED	50 pF
t_{0H}	CLOSED	CLOSED	5 pF*
t_{1H}	CLOSED	CLOSED	5 pF*
t_{H0}	CLOSED	OPEN	50 pF
t_{H1}	OPEN	CLOSED	50 pF

*Approximate value of jig capacitance only

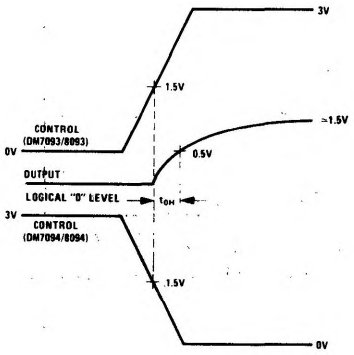
switching time waveforms

INPUT CHARACTERISTICS
FREQ: 1 MHz
PULSE WIDTH: 100 ns
$t_r = t_f \leq 10$ ns
AMPLITUDE = 3V

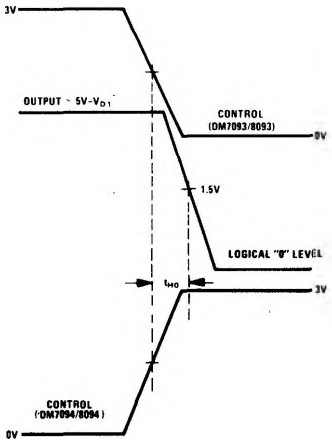
t_{pd1} & t_{pd0}



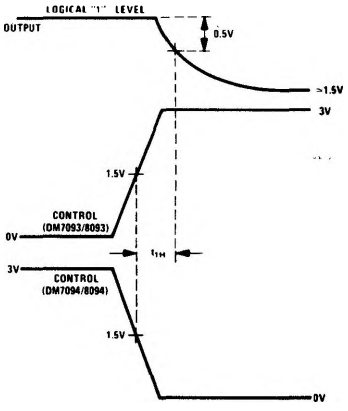
t_{0H}



t_{H0}



t_{1H}



t_{H1}