Tri-State Logic

DM7831/DM8831 tri-state line driver

general description

Through simple logic control, the DM7831/DM8831 can be used as either a quad single-ended line driver or a dual differential line driver. It is specifically designed for party line (bus-organized) systems. Key features include:

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line.

mode of operation

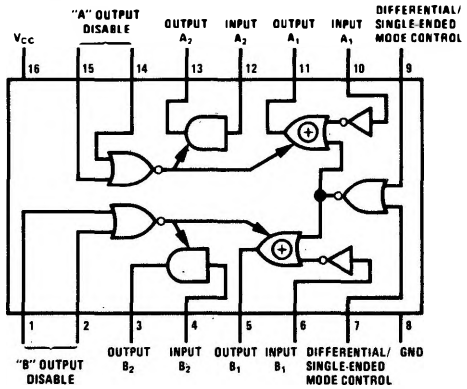
To operate as a quad single-ended line driver apply logical "0"s to the Output Disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs. The inputs to the A channels should be connected together and the inputs to the B channels should be connected together. In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_2 outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other

(Continued on page 29)

connection and logic diagram



truth-table (Shown for A Channels Only)

"A" OUTPUT DISABLE		DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL		INPUT A_1	OUTPUT A_1	INPUT A_2	OUTPUT A_2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A_1	Logical "1" or Logical "0"	Same as Input A_2
0	0	X	1	Logical "1" or Logical "0"	Opposite of Input A_1	Logical "1" or Logical "0"	Same as Input A_2
		1	X				
1	X	X	X	X	High impedance state	X	High impedance state
X	1						

X = Don't Care

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range DM7831	−55°C to +125°C
DM8831	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously	10 ms

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7831	V_{CC} = 4.5V	2.0			V
	DM8831	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7831	V_{CC} = 4.5V			0.8	V
	DM8831	V_{CC} = 4.75V				
Logical "1" Output Voltage	DM7831	V_{CC} = 4.5V, I_O = −40 mA	1.8	2.8		V
		V_{CC} = 4.5V, I_O = −2 mA	2.4	3.1		V
	DM8831	V_{CC} = 4.75V, I_O = −40 mA	1.8	2.8		V
		V_{CC} = 4.75V, I_O = −5.2 mA	2.4	3.0		V
Logical "0" Output Voltage	DM7831	V_{CC} = 4.5V, I_O = 40 mA		0.29	0.50	V
		V_{CC} = 4.5V, I_O = 32 mA			.40	V
	DM8831	V_{CC} = 4.75V, I_O = 40 mA		0.29	0.50	V
		V_{CC} = 4.75V, I_O = 32 mA			.40	V
Logical "1" Input Current	DM7831	V_{CC} = 5.5V, V_{IN} = 5.5V			1	mA
	DM8831	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "0" Input Current	DM7831	V_{CC} = 5.5V, V_{IN} = 0.4V		−1.0	−1.6	mA
	DM8831	V_{CC} = 5.25V, V_{IN} = 0.4V				
Output Disable Current	DM7831	V_{CC} = 5.5V, V_O = 2.4V			40	μA
	DM8831	V_{CC} = 5.25V, V_O = 0.4V			−40	μA
Output Short Circuit Current	DM7831	V_{CC} = 5.5V	−40 (Note 2)	−100	−120 (Note 2)	mA
	DM8831	V_{CC} = 5.25V				
Supply Current	DM7831	V_{CC} = 5.5V		57	90	mA
	DM8831	V_{CC} = 5.25V				
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Output Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{OUT} = −12 mA			−1.5	V
		I_{OUT} = +12 mA			V_{CC}+1.5	V
Propagation Delay to a Logical "0" from Inputs A_1, A_2, B_1, B_2, Differential Single-ended Mode Control to Outputs, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C		13	25	ns
Propagation Delay to a Logical "1" from Inputs A_1, A_2, B_1, B_2, Differential Single-ended Mode Control to Outputs, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		13	25	ns
Delay from Disable Inputs to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5.0V, T_A = 25°C		6	12	ns
Delay from Disable Inputs to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5.0V, T_A = 25°C		14	22	ns
Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State), t_{Hi}		V_{CC} = 5.0V, T_A = 25°C		14	22	ns
Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State), t_{H0}		V_{CC} = 5.0V, T_A = 25°C		18	27	ns

Note 1: Unless otherwise specified min/max limits apply across the −55° to +125°C temperature range for the DM7831 and across the 0°C to 70°C temperature range for the DM8831. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Applies for T_A = 125°C only. Only one output should be shorted at a time.

mode of operation (cont.)

DM7831/DM8831's (Figure 1), all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DM7831/DM8831's (Figure 2).

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DM7831/DM8831's and still have available drive for the bus line (Figure 3).

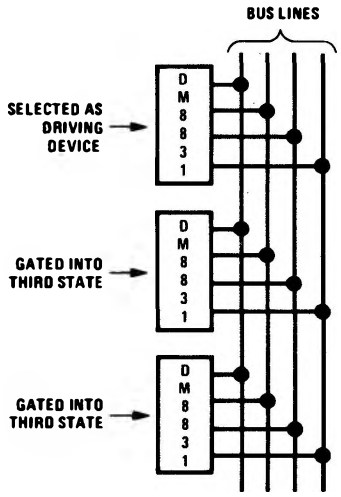


Figure 1

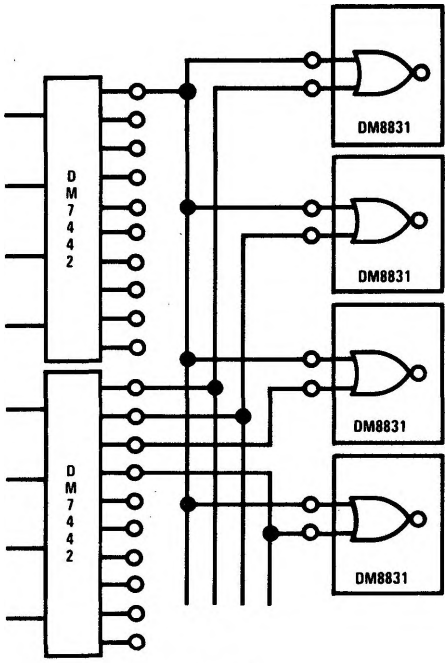


Figure 2

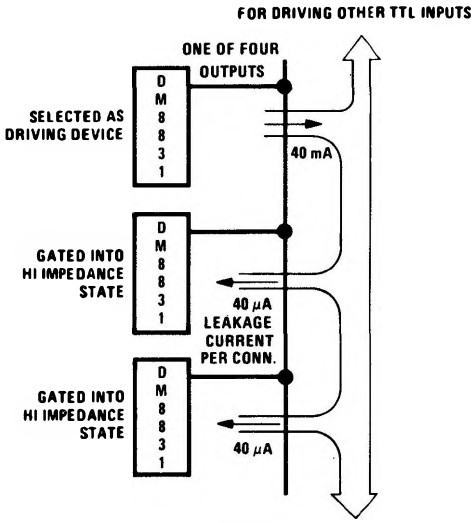
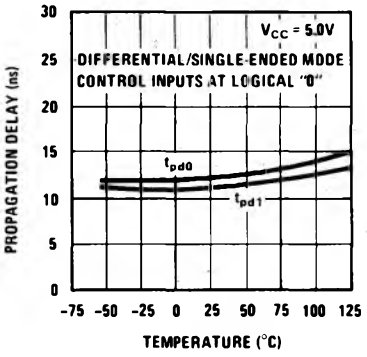


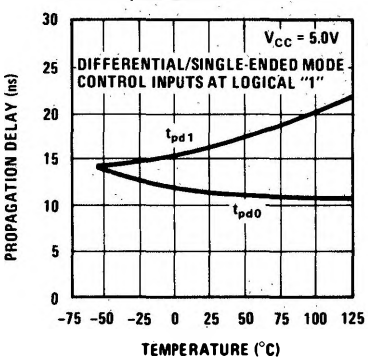
Figure 3

typical performance characteristics

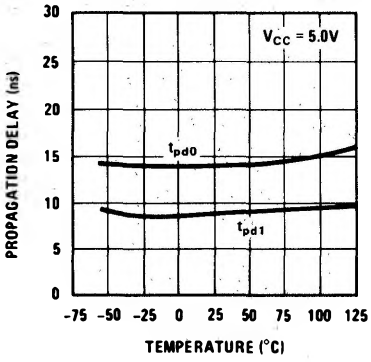
Propagation Delay from Input to Output (Channel 1)



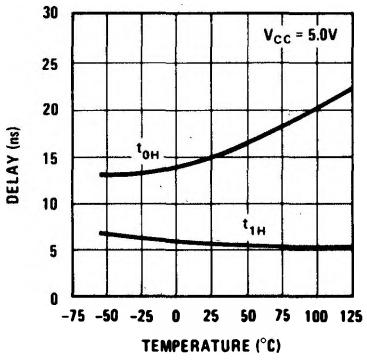
Propagation Delay from Input to Output (Channel 1)



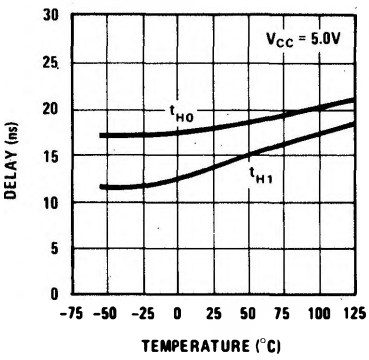
Propagation Delay from Input to Output (Channel 2)



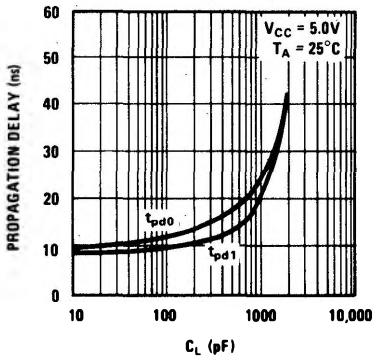
Delay from Disable to High Impedance State



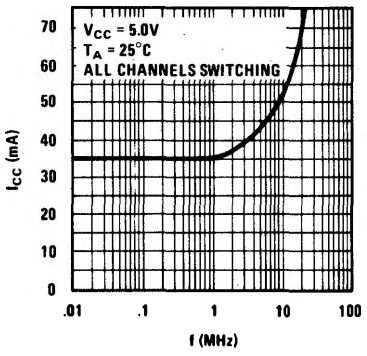
Delay from Disable to Low Impedance State



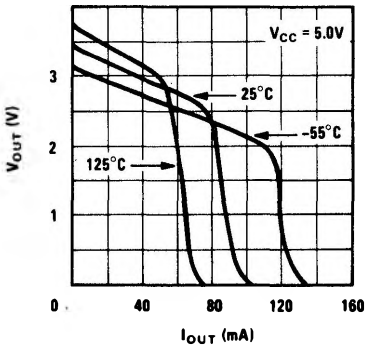
Propagation Delay vs Load Capacitance



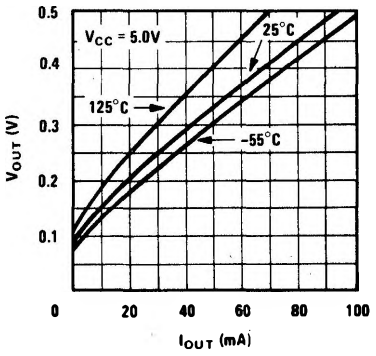
Total Supply Current vs Frequency



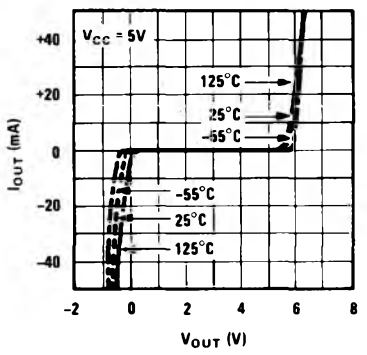
Logical "1" Output Voltage vs Source Current



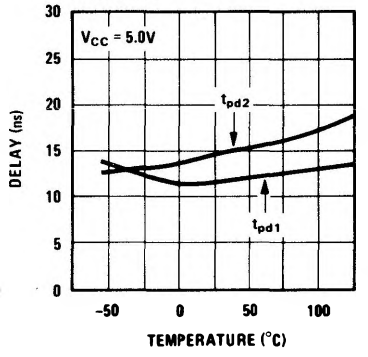
Logical "0" Output Voltage vs Sink Current

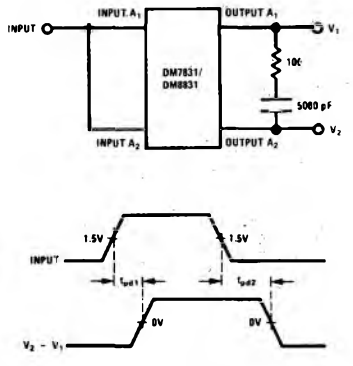


I_{OUT} vs V_{OUT} High Impedance Output State



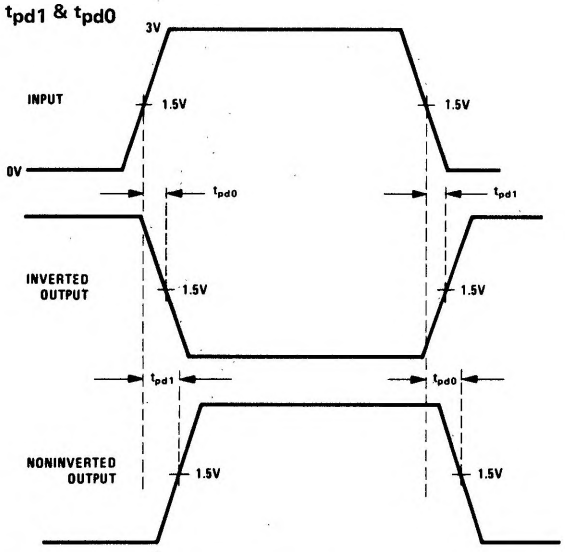
Propagation Delay in Differential Mode





switching time waveforms

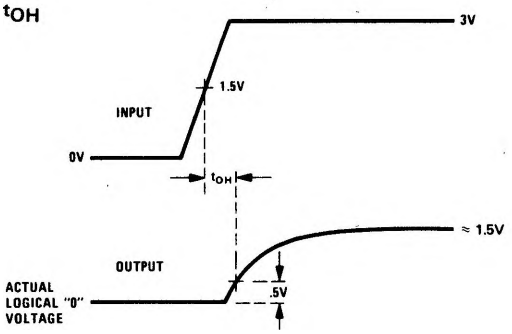
t_{pd1} & t_{pd0}



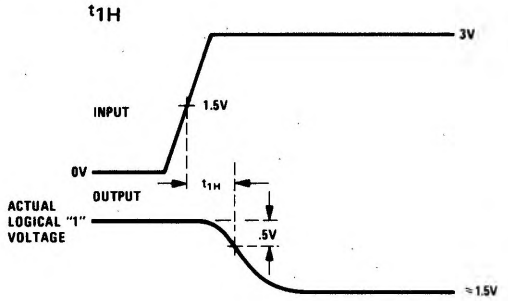
Input characteristic

Amplitude = 3V
frequency = 1 MHz, 50% duty cycle.
$t_r = t_f \leq 10$ nsec (10% to 90%)

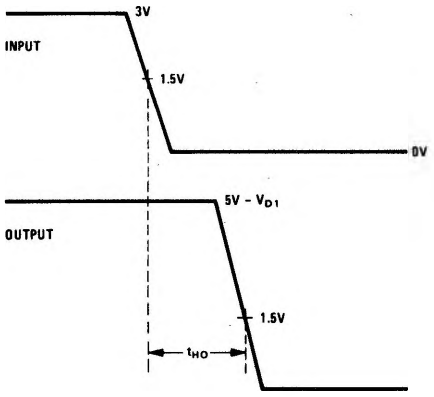
t_{OH}



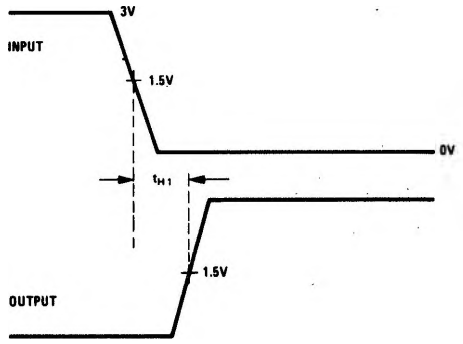
t_{1H}



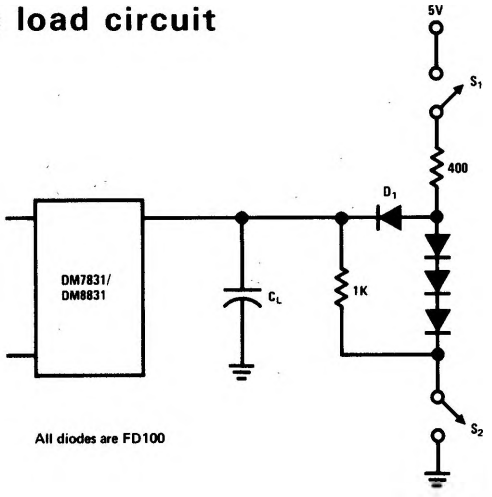
t_{HO}



t_{H1}



ac load circuit



All diodes are FD100

	Switch S_1	Switch S_2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{0H}	closed	closed	* 5 pF
t_{1H}	closed	closed	* 5 pF
t_{HO}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*jig capacitance