National Semiconductor

9300/DM9300 4-Bit Parallel-Access Shift Register

General Description

The 9300 4-bit registers feature parallel inputs, parallel outputs, $J\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction Q_A toward Q_D).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the $J\overline{K}$ inputs. These inputs permit the first stage to perform as a $J\overline{K}$, D or T-type flip-flop as shown in the function table.

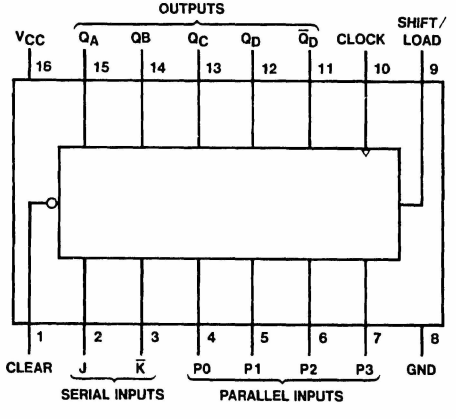
These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

Features

- Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Positive edge-triggered clocking
- J and $\overline{K}$ inputs to first stage
- Typical shift frequency—39 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6600–1

Order Number 9300DMQB, 9300FMQB or DM9300N
See NS Package Number J16A, N16E or W16A

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	P0	P1	P2	P3					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Bn}	$\overline{Q}_{Cn}$

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care

↑ = Transition from low-to-high level

a, b, c, d, = The level of steady state input at P0, P1, P2, or P3 respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.8	mA
I_{OL}	Low Level Output Current				9.6			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		30	0		30	MHz
t_W	Pulse Width (Note 5)	Clock	17			16	11		ns
		Clear	25			30	15		
t_{SU}	Setup Time (Note 5)	S/L	36			30	13		ns
		Data	18			20	13		
		Clear	36			30	13		
t_H	Data Hold Time (Note 5)		0			0	−11		ns
t_{REL}	S/L Release Time (Notes 1 and 5)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Input			40	μA
			CP Input			80	
			$\overline{PE}$ Input			92	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Input			−1.6	mA
			CP Input			−3.2	
			$\overline{PE}$ Input			−3.7	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	MIL	−20		−80	mA
			COM	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)	MIL			86	mA
			COM			92	

Note 1: RELEASE TIME: $t_{RELEASE}$ is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) *not* to respond.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to J, K, and data inputs, I_{CC} is measured by applying momentary ground, then 4.5V to CLEAR, and then to CLOCK.

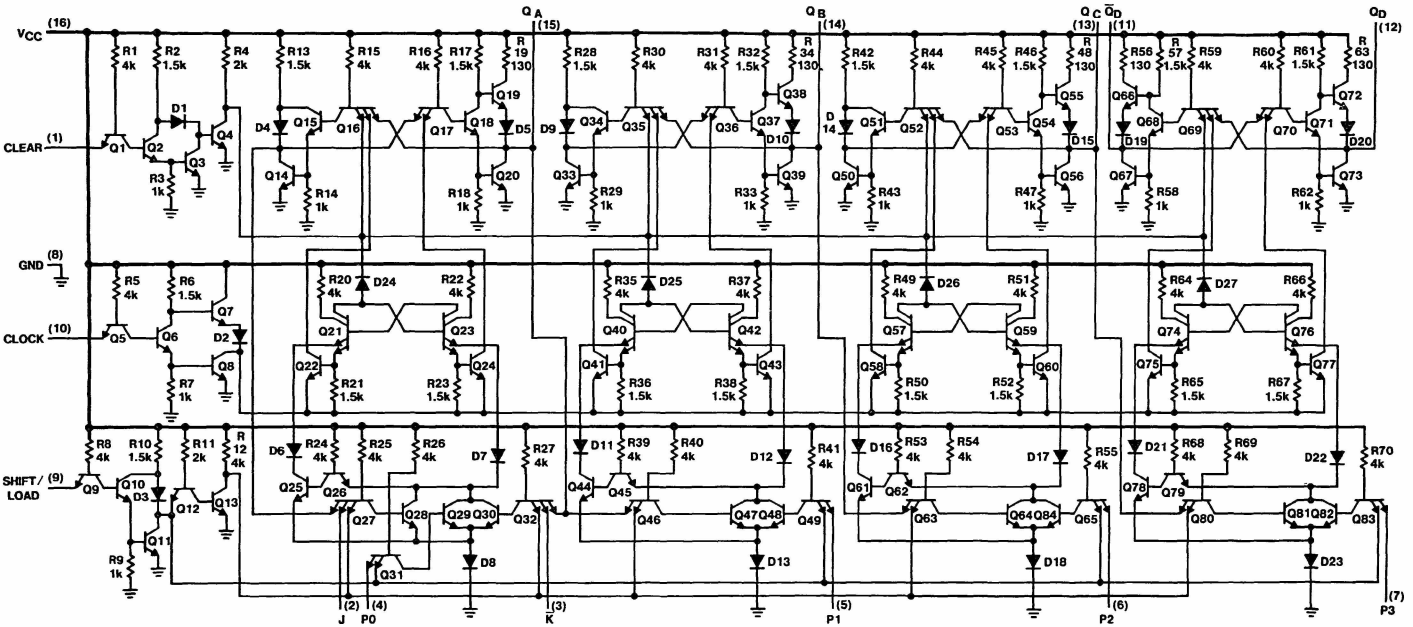
Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Military		Commercial		Units
			R_L = 400Ω, C_L = 15 pF		R_L = 400Ω, C_L = 15 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		20		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		24		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		37		30	ns

Schematic Diagram

DM9300



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