DM9300 / DM8300 (9300-51/9300-59) four-bit shift register

general description

The DM9300/DM8300 is a four-bit multi-function shift register designed to work at typical speeds of 25 MHz.

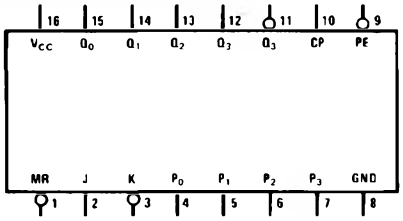
It features a common asynchronous Reset input which resets the register independent of any other input. In addition, the J and $\overline{K}$ inputs to the first flip flop enable greater flexibility in the operation of the register. (See truth table.)

The $\overline{PE}$ (Parallel Enable) control allows information to be entered from the parallel inputs or be shifted right. When the $\overline{PE}$ input is in the logical "0" state, the information on the parallel inputs will be entered into the flip flops on the subsequent clock pulse. A logical "1" level on the PE control will allow shifting to the right.

The outputs change state on the positive-going transition of the clock input.

This register is completely compatible with Series 54/74 and CCSL devices. Input diode clamps are provided for additional system reliability.

connection diagram



truth table

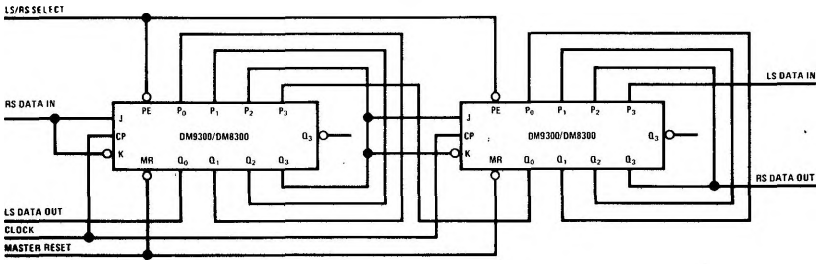
J	$\overline{K}$	Q_0 at t_{n+1}
0	0	0
0	1	Q_0 at t_n (no change)
1	0	$\overline{Q}_0$ at t_n (toggle)
1	1	1

($\overline{PE}$ = logical "1", $\overline{MR}$ = logical "1")

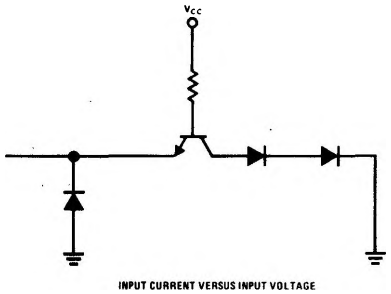
typical application

Eight Bit Left/Right Shift Register

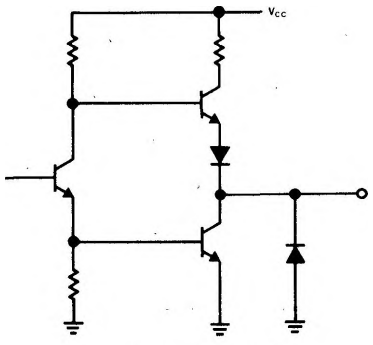
This register shifts left or right on each shift clock, depending upon the condition of the LS/RS select input. If this input is high, right shift occurs and if low, left shift occurs.



equivalent circuits



INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
(Q_0, Q_1, Q_2, Q_3 AND $\overline{Q}_3$)

absolute maximum ratings

V_{CC} Voltage Range		-.5V to 7V
Input Voltage Range		-.5V to 5.5V
Output Voltage (Logical "1" state)		5.5V
Operating Temperature Range	DM9300(9300-51)	-55°C to +125°C
	DM8300(9300-59)	0°C to 75°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C MIN	LIMITS -55°C MAX	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5V, I_{OH} = -0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5V, I_{OL} = 9.6 mA V_{CC} = 4.5V, I_{OL} = 7.44 mA
V_H	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.10	-1.6		-1.6	mA	V_{CC} = 5.5V
	J, K, MR, P_0, P_1, P_2 & P_3		-1.24		-0.97	-1.24		-1.24	mA	V_{CC} = 4.5V V_F = 0.4V
I_R	Input Leakage Current J, K, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.5V, V_R = 4.5V

electrical characteristics (T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN	LIMITS 0°C MAX	LIMITS +25°C MIN	LIMITS +25°C TYP	LIMITS +25°C MAX	LIMITS +75°C MIN	LIMITS +75°C MAX	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75V, I_{OH} = -0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 5.25V, I_{OL} = 9.6 mA
V_H	Input High Voltage	1.9		1.8			1.6		Volts	V_{CC} = 4.75V, I_{OL} = 8.5 mA Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.0	-1.6		-1.6	mA	V_{CC} = 5.25V
	J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3		-1.41		-0.9	-1.41		-1.41	mA	V_{CC} = 4.75V, V_F = 0.45V
I_R	Input Leakage Current J, $\overline{K}$, MR, P_0, P_1, P_2 & P_3				15	60		60	μA	V_{CC} = 5.25V, V_R = 4.5V

switching characteristics (T_A = 25°C)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		17	35	ns	V_{CC} = 5.0V, C_L = 15 pF
t_{pd-}	Turn On Delay		22	45	ns	(See Figs. 1 & 2a)
f_{sr}	Shift Right Frequency	15	30		MHz	V_{CC} = 5.0V, C_L = 15 pF (See Figs. 1 & 2c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	10		ns	V_{CC} = 5.0V
t_r	Release Time		10	0	ns	C_L = 15 pF
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	20		ns	(See Figs. 2a & 2b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		17	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		28		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		13		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

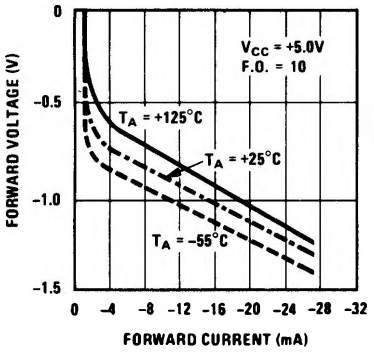
SET UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip flop(s) not to respond.

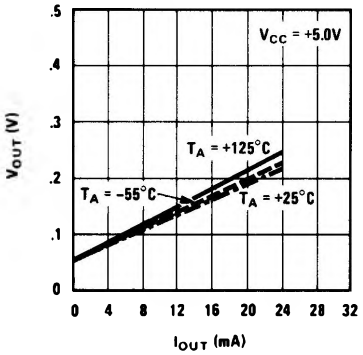
RECOVERY TIME FOR $\overline{MR}$: $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip flop(s) to respond to the clock.

typical performance characteristics

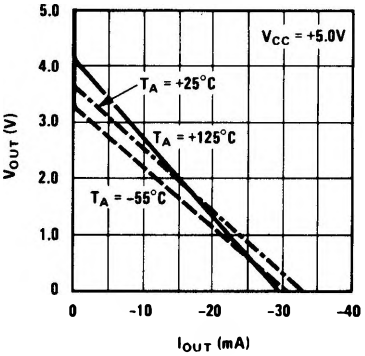
Input Clamp Diode Characteristics



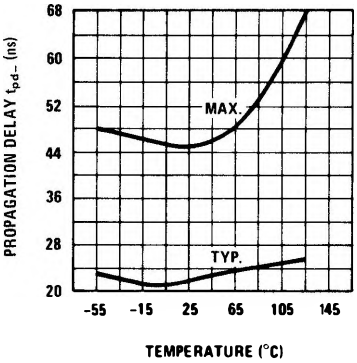
Logical "0" Output Voltage vs Sink Current



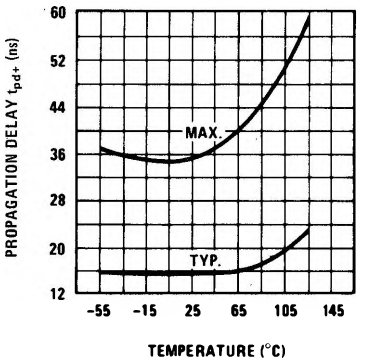
Logical "1" Output Voltage vs Source Current



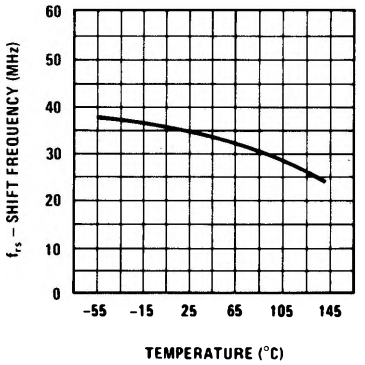
t_{pd-} Propagation Delay – Clock to Q_3 or $\overline{Q}_3$ Outputs vs Temp.



t_{pd+} Propagation Delay – Clock to Q_3 or $\overline{Q}_3$ Outputs vs Temp.



f_{rs} – Shift Frequency vs Temp.



ac test circuit

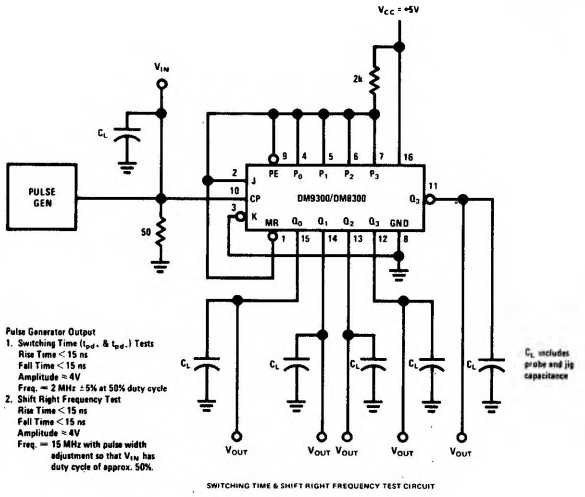


Figure 1

switching time waveforms

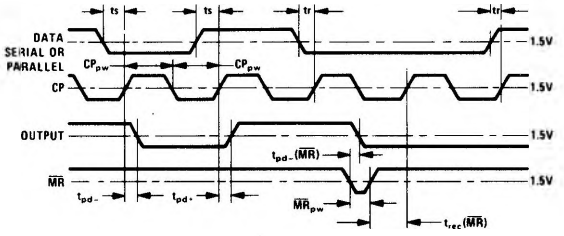


Figure 2a

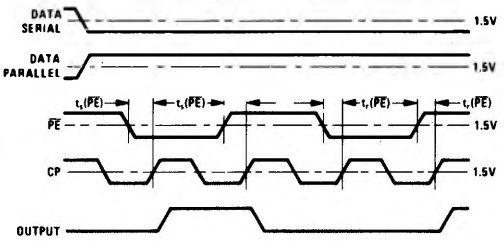


Figure 2b

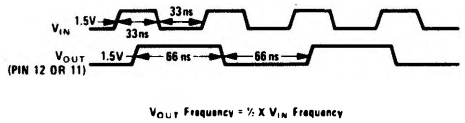


Figure 2c