National Semiconductor

DM93S00
4-Bit Universal Shift Register

General Description

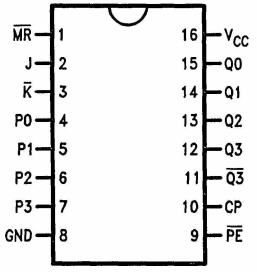
This device is 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

Features

- Asynchronous master reset
- J, $\overline{K}$ inputs to first stage

Connection Diagram

Dual-In-Line Package



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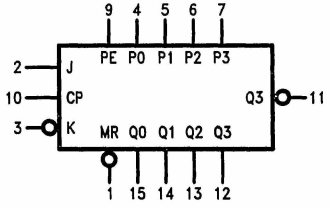
Order Number DM93S00N
See NS Package Number N16E

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Truth Table

Operating Mode	Inputs ($\overline{MR}$ = H)							Outputs @ tn+1				
	$\overline{PE}$	J	$\overline{K}$	P0	P1	P2	P3	Q0	Q1	Q2	Q3	$\overline{Q3}$
Shift Mode	H	L	L	X	X	X	X	L	Q0	Q1	Q2	$\overline{Q2}$
	H	L	H	X	X	X	X	Q0	Q0	Q1	Q2	$\overline{Q2}$
	H	H	L	X	X	X	X	$\overline{Q0}$	Q0	Q1	Q2	$\overline{Q2}$
	H	H	H	X	X	X	X	H	Q0	Q1	Q2	$\overline{Q2}$
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

*tn+1 = State after next LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S00			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW, J, $\overline{K}$ and P0–P3 to CP	6.0 6.0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, J, $\overline{K}$ and P0–P3 to CP	0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, $\overline{PE}$ to CP	8.0 8.0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW, $\overline{PE}$ to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	7.0 7.0			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	12			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2.0	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	20		80	mA
I_{CC}	Supply Current	V_{CC} = Max			120	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Shift Frequency	70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Qn		8.5 12	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		23	ns

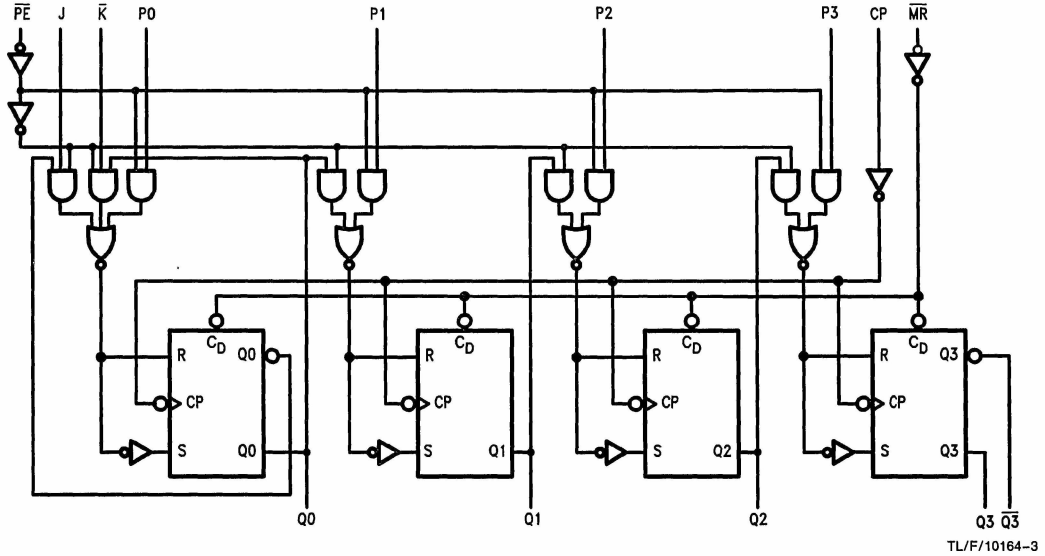
Functional Description

The Logic Diagrams and Truth Table indicate the functional characteristics of the DM93S00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.

The DM93S00 has two primary modes of operation, shift right (Q0 → Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction Q0 → Q1 → Q2 → Q3 following each LOW-to-HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the DM93S00 appears as four common clocked D flip-flops. The data on the parallel inputs P0–P3 is transferred to the respective Q0–Q3 outputs following the LOW-to-HIGH clock transition. Shift left operation (Q3 → Q2) can be achieved by tying the Qn outputs to the Pn−1 inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. Since the DM93S00 utilizes edge triggering, there is no restriction on the activity of the J, $\overline{K}$, Pn and $\overline{PE}$ inputs for logic operation—except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

Logic Diagram



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