National Semiconductor

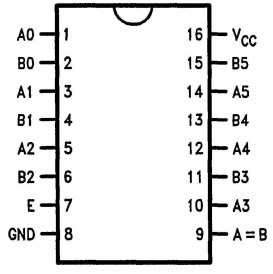
DM93S46
High-Speed 6-Bit Identity Comparator

General Description

The DM93S46 is a very high speed 6-bit identity comparator. The device compares two words of up to six bits and indicates identity in less than 12 ns. It is easily expandable to any word length by using either serial or parallel expansion techniques. When the Enable input (E) is LOW, it forces the output LOW.

Connection Diagram

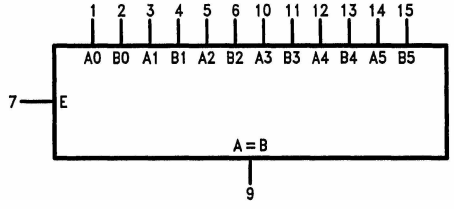
Dual-In-Line Package



TL/F/9807–1

Order Number DM93S46N
See NS Package Number N16E

Logic Symbol



TL/F/9807–2

V_{CC} = Pin 16
GND = Pin 18

Pin Name	Description
A0–A5	Word A Inputs
B0–B5	Word B Inputs
E	Enable Input (Active High)
A=B	A Equal to B Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM93S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM93S46			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−20	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	Conditions	CL = 15 pF		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	E = 4.5V, Other Inputs = 4.5V, Test Each Input Individually	3.0 3.0	17 17	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to A = B	E = 4.5V, Other Inputs = Gnd, Test Each Input Individually	3.0 3.0	14 15	ns
t_{PLH} t_{PHL}	Propagation Delay E to A = B	A_n = B_n	2.0 2.0	10 10	ns

Functional Description

The DM93S46 is a very high speed 6-bit identity comparator. The A = B output is HIGH when the Enable (E) is HIGH and the two 6-bit words are equal. Equality is determined by Exclusive-NOR circuits which individually compare the equivalent bits from each word. When any two of the equivalent bits from each word have different logic levels, the A = B output is LOW.

$$(A = B) = (\overline{A0 \oplus B0}) \bullet (\overline{A1 \oplus B1}) \bullet (\overline{A2 \oplus B2}) \bullet (\overline{A3 \oplus B3}) \bullet (\overline{A4 \oplus B4}) \bullet (\overline{A5 \oplus B5}) \bullet E$$

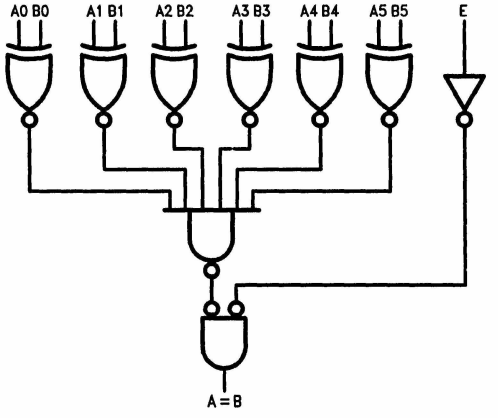
An active HIGH Enable (E) provides a means of fast ripple expansion. By connecting the A = B output of the first stage of the comparator to the enable of the next stage, the comparator can be expanded in 6-bit increments at an additional 4.5 ns per stage. An even faster expansion technique is achieved by connecting the A = B outputs to a Schottky NAND gate. This method compares two words of up to 78 bits each in 15 ns (typical) using the '133 13-input Schottky NAND gate.

Truth Table

Inputs		Output
E	**A_n, B_n**	**A = B**
L	$A_n = B_n$	L
L	$A_n \neq B_n$	L
H	$A_n \neq B_n$	L
H	$A_n = B_n$	H

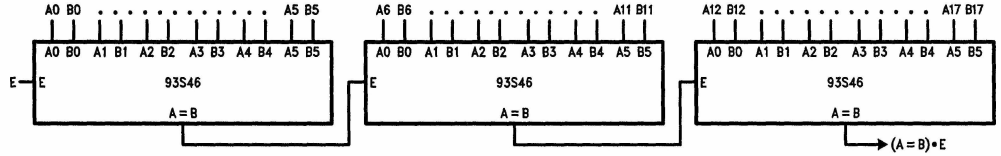
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



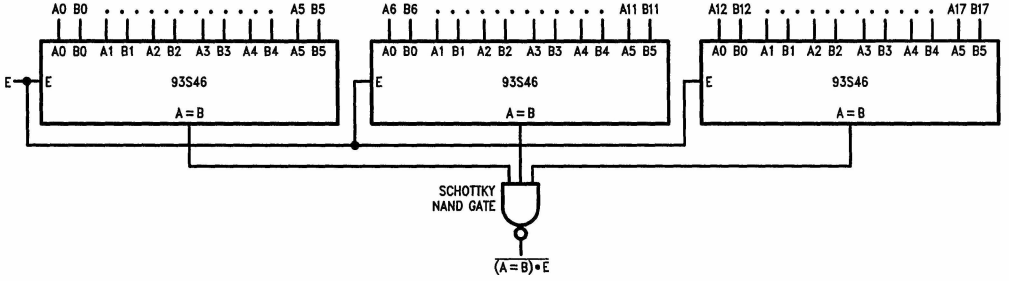
TL/F/9807–5

Ripple Expansion



TL/F/9807–3

Note: This simple method of expansion adds 4.5 ns for each additional '46 used.



TL/F/9807–4

Note: This method of expansion adds one gate delay (≃3 ns) to the '46, independent of the word length that is compared.