



96LS02/DM96LS02 Dual Retriggerable Resettable Monostable Multivibrator

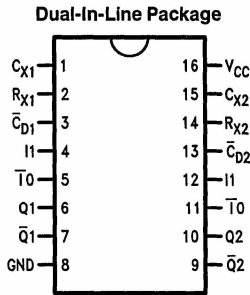
General Description

The 96LS02 is a dual retriggerable and resettable monostable multivibrator. The one-shot provides exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 M Ω reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 for increased noise immunity.

Features

- Required timing capacitance reduced by factors of 10 to 100 over conventional designs
- Broad timing resistor range—1.0 k Ω to 2.0 M Ω
- Output Pulse Width is variable over a 2000:1 range by resistor control
- Propagation delay of 35 ns
- 0.3V hysteresis on trigger inputs
- Output pulse width independent of duty cycle
- 35 ns to ∞ output pulse width range

Connection Diagram



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Order Number 96LS02DMQB, 96LS02FMQB, DM96LS02M or DM96LS02N
See NS Package Number J16A, M16A, N16E or W16A

Pin Names	Description
$\bar{I}0$	Trigger Input (Active Falling Edge)
$\bar{I}0$	Schmitt Trigger Input (Active Falling Edge)
I1	Schmitt Trigger Input (Active Rising Edge)
$\bar{C}D$	Direct Clear Input (Active LOW)
Q	True Pulse Output
$\bar{Q}$	Complementary Pulse Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage 10V

Operating Free Air Temperature Range

96LS Military -55°C to +125°C

DM96LS Commercial 0°C to +70°C

Storage Temperature Range -65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	96LS02 (MIL)			DM96LS02 (COM)			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	MIL 2.5			V
			COM 2.7	3.4		
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min	MIL		0.4	V
			COM	0.35	0.5	
		I _{OL} = 4 mA, V _{CC} = Min	COM	0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 10V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max	MIL	-20	-100	mA
		(Note 2)	COM	-20	-100	
I _{CC}	Supply Current	V _{CC} = Max			36	mA
V _{T+}	Positive-Going Threshold Voltage, I ₀ , I ₁				2.0	V
V _{T-}	Negative-Going Threshold Voltage, I ₀ , I ₁		MIL	0.7		V
			COM	0.8		

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25^\circ C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	96LS (MIL)		DM96LS (COM)		Units
		C _L = 15 pF		C _L = 15 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay I ₀ to Q		45		55	ns
t _{PHL}	Propagation Delay I ₀ to Q̄		33		50	ns
t _{PLH}	Propagation Delay I ₁ to Q		45		60	ns
t _{PHL}	Propagation Delay I ₁ to Q̄		33		55	ns
t _{PHL}	Propagation Delay C̄ _D to Q		25		30	ns
t _{PLH}	Propagation Delay C̄ _D to Q̄		30		35	ns
t _w (L)	I ₀ Pulse Width LOW	15		15		ns
t _w (H)	I ₁ Pulse With HIGH	30		30		ns
t _w (L)	C̄ _D Pulse Width LOW	22		22		ns
t _w (H)	Minimum Q Pulse Width HIGH	20	70	25	55	ns
t _w	Q Pulse Witdh	4.25	5.0	4.1	4.5	μs
R _X	Timing Resistor Range*			1	1000	kΩ
t	Change in Q Pulse Width over Temperature				1.0	%
t	Change in Q Pulse Width over V _{CC} Range				0.8 1.5	%

*Applies only over commercial V_{CC} and T_A range for 96S02.

Functional Description

The 96LS02 dual retriggerable resettable monostable multivibrator has two DC coupled trigger inputs per function, one active LOW ($\bar{I}0$) and one active HIGH (I1). The I1 input and $\bar{I}0$ input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are DC coupled making triggering independent of input transition times. When input conditions for triggering are met, the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\bar{Q}$ output to $\bar{I}0$ or the Q output to I1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

Operation Notes

TIMING

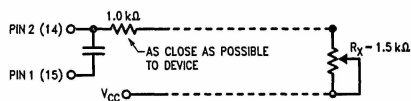
1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 k Ω to 1.0 M Ω (96LS02).
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (−) terminal to pin 2(14) and R_X . Pin 1(15) will remain positive with respect to pin 2(14) during the timing cycle.
4. The output pulse width t_w for $R_X \geq 10\text{ k}\Omega$ and $C_X \geq 1000\text{ pF}$ is determined as follows:

$$t_w = 0.43 R_X C_X$$

Where R_X is in k Ω , C_X is in pF, t is in ns or R_X is in k Ω , C_X is in μF , t is in ms.

5. The output pulse width for $R_X < 10\text{ k}\Omega$ or $C_X < 1000\text{ pF}$ should be determined from pulse width versus C_X or R_X graphs.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



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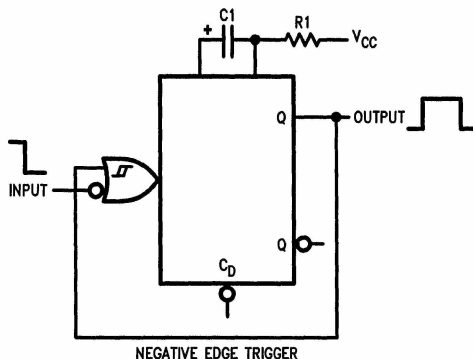
Operation Notes (Continued)

7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

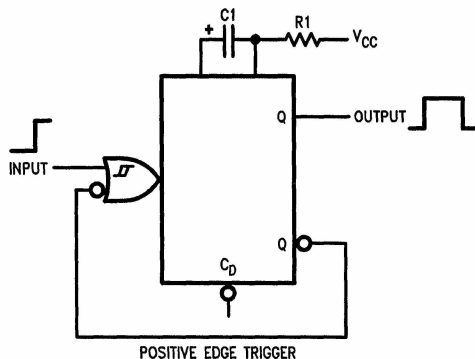
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a $0.01\ \mu F$ to $0.1\ \mu F$ bypass capacitor between V_{CC} and ground located near the circuit is recommended.

TRIGGERING

1. The minimum negative pulse width into $\bar{I}0$ is 8.0 ns; the minimum positive pulse width into $I1$ is 12 ns.



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Triggering Truth Table

Pin No's.			Operation
5(11)	4(12)	3(13)	
H $\rightarrow$ L	L	H	Trigger
H	L $\rightarrow$ H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level $\geq V_{IH}$

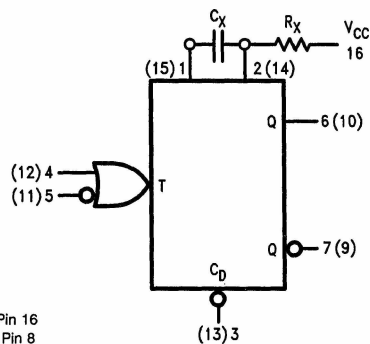
L = LOW Voltage Level $\leq V_{IL}$

X = Immaterial (either H or L)

H → L = HIGH to LOW Voltage Level Transition

L → H = LOW to HIGH Voltage Level Transition

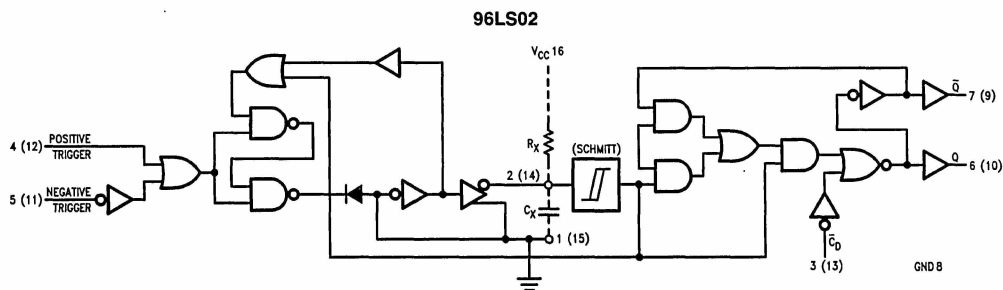
Logic Symbol



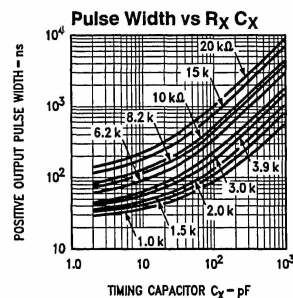
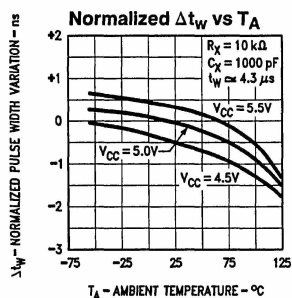
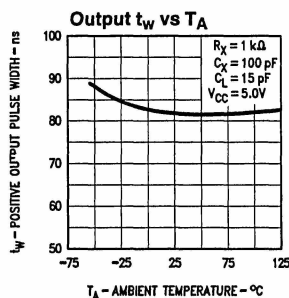
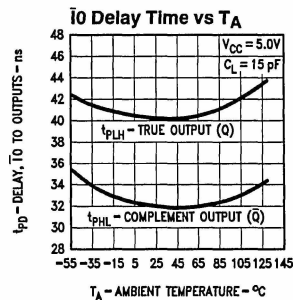
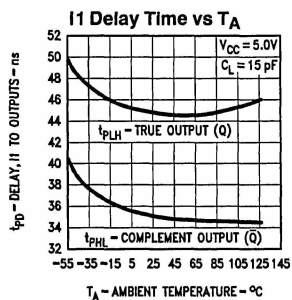
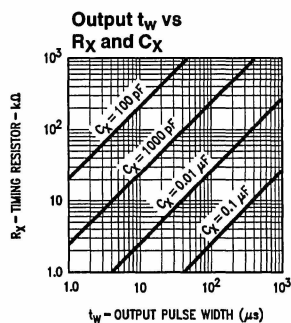
V_{CC} = Pin 16
GND = Pin 8

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Logic Diagram



Typical Performance Characteristics



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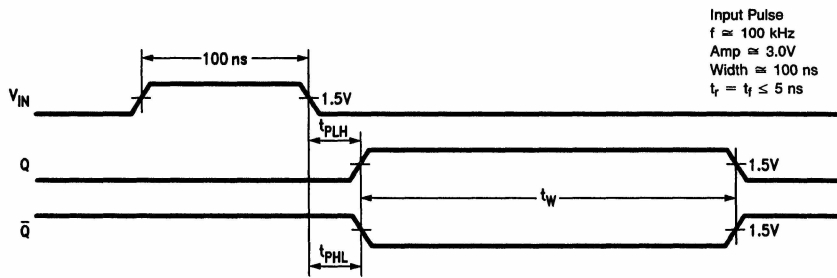


FIGURE A

TL/F/9816-8