

# DN8667NS

## 8-Bit Shift Register Latch Constant Current Driver IC

### ■ Overview

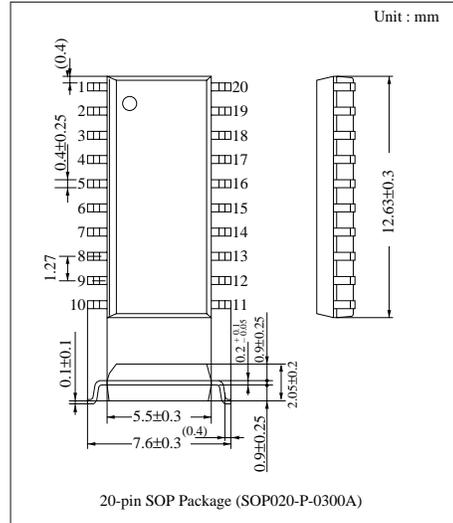
The DN8667NS is a semiconductor integrated circuit which incorporates a 8-bit shift register, a latch driver and a constant current driver to satisfy the demand for equalization of LED panel brightness. It also incorporates the serial-in and serial-out/parallel-out functions. It employs the Bi-CMOS process : The 8-step shift register block and latch block consist of CMOS while the 8-step parallel driver block is bipolar.

### ■ Features

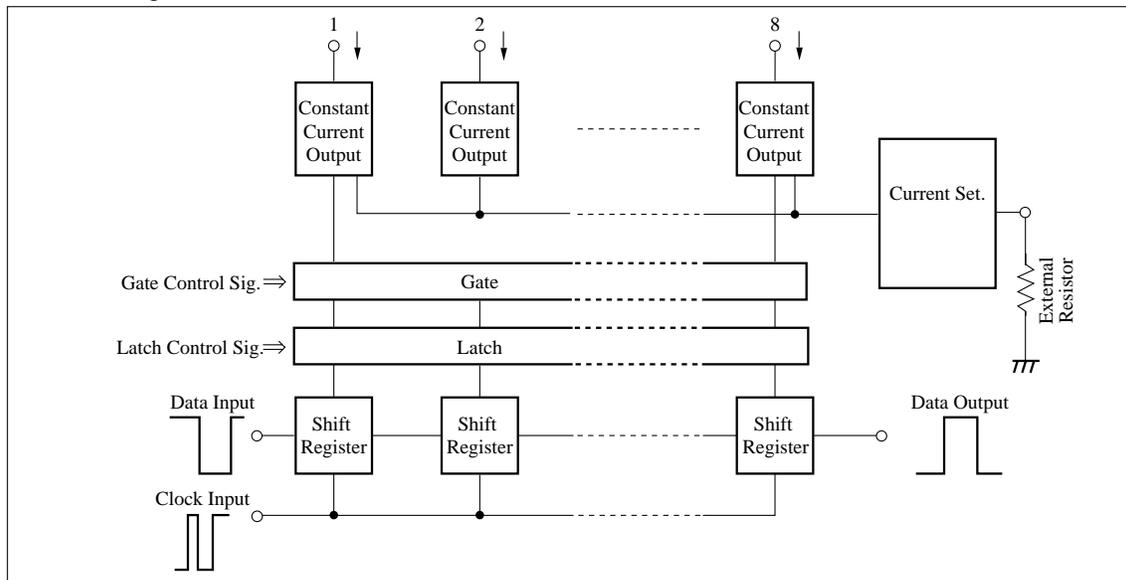
- Serial-in, serial-out/parallel-out
- Cascade connection possible
- Constant current output (0 to 100 mA able to be set by one external resistor)
- Output-forced ON/OFF terminal attached (EN)
- Input/Output CMOS compatible

### ■ Application

- LED panel drive



### ■ Block Diagram



### ■ Absolute Maximum Rating (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	0 to + 7.0	V
Output voltage	V <sub>O</sub>	0 to + 14	V
Output current	I <sub>O</sub>	150	mA
Power dissipation*	P <sub>D</sub>	1.28	W
Operating ambient temperature	T <sub>opr</sub>	-20 to + 85	°C
Storage temperature	T <sub>stg</sub>	-55 to + 150	°C

\* For printed board SM, it decreases with rate of 10.24 mW/°C from Ta = 25 °C.

### ■ Recommended Operation Range (Ta=25 °C)

Parameter	Symbol	Range
Operating supply voltage	V <sub>CC</sub>	4.5V to 5.5V

### ■ Electrical Characteristics (V<sub>CC</sub>=5V, Ta=25 ± 2°C)

Parameter	Symbol	Condition	min	typ	max	Unit		
Input voltage	Positive direction	V <sub>T+</sub>	$\begin{cases} V_{SOUT} = 0.1, V_{CC} - 0.1V \\  I_{SOUT}  = 20\mu A \end{cases}$	0.35V <sub>CC</sub>	—	0.7V <sub>CC</sub>	V	
	Negative direction	V <sub>T-</sub>	$\begin{cases} I_O (\overline{Qn}) = -10\mu A, 90mA \\ V_O (\overline{Qn}) = 0.6V, I_{ref} = -2.5mA \end{cases}$	0.2V <sub>CC</sub>	—	0.55V <sub>CC</sub>	V	
Input current	I <sub>IH</sub>	V <sub>IH</sub> = 5.0V	—	—	25	μA		
	I <sub>IL</sub>	V <sub>IL</sub> = 0V	-25	—	—	μA		
Output voltage (SOUT)	V <sub>OH</sub>	I <sub>OH</sub> = -0.4mA	4.0	—	—	V		
	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA	—	—	0.5	V		
Output current 1 ( $\overline{Qn}$ )	I <sub>O1</sub>	V <sub>O</sub> ( $\overline{Qn}$ ) = 0.5V	—	—	100	mA		
Output current 2 ( $\overline{Qn}$ )	I <sub>O1</sub>	V <sub>CC</sub> = 5.0V, I <sub>ref</sub> = -12mA	83	—	117	mA		
Output current error between bits	DI <sub>O</sub>	V <sub>O</sub> ( $\overline{Qn}$ ) = 1.0V	—	—	±6	%		
Output leak current	I <sub>OLK</sub>	V <sub>O</sub> = 14V (Output OFF)	—	—	25	μA		
Supply current	I <sub>CC1</sub>	Total Driver Output V <sub>CC</sub> =5.5V	OFF	I <sub>ref</sub> = 0mA	—	—	2	mA
	I <sub>CC2</sub>			I <sub>ref</sub> = -2.5mA	—	—	20	mA
	I <sub>CC3</sub>			I <sub>ref</sub> = -2.5mA	—	—	30	mA
Clock frequency	f <sub>CLK</sub>	CLK	Input Duty 40 to 60%		—	—	20	MHz
Input pulse width	t <sub>w</sub>	CLK	V <sub>CC</sub> =5.0V R <sub>L</sub> =50Ω C <sub>L</sub> =15pF	20	—	—	ns	
		STB		20	—	—	ns	
Setting-up time	t <sub>su</sub>	SIN		20	—	—	ns	
		STB		15	—	—	ns	
Holding time	t <sub>h</sub>	SIN		20	—	—	ns	
		STB		10	—	—	ns	
Clock pulse rise time	t <sub>r</sub>		—	—	500	ns		
Clock pulse fall time	t <sub>f</sub>		—	—	500	ns		

Note) V<sub>CC</sub>= 5V unless otherwise specified.

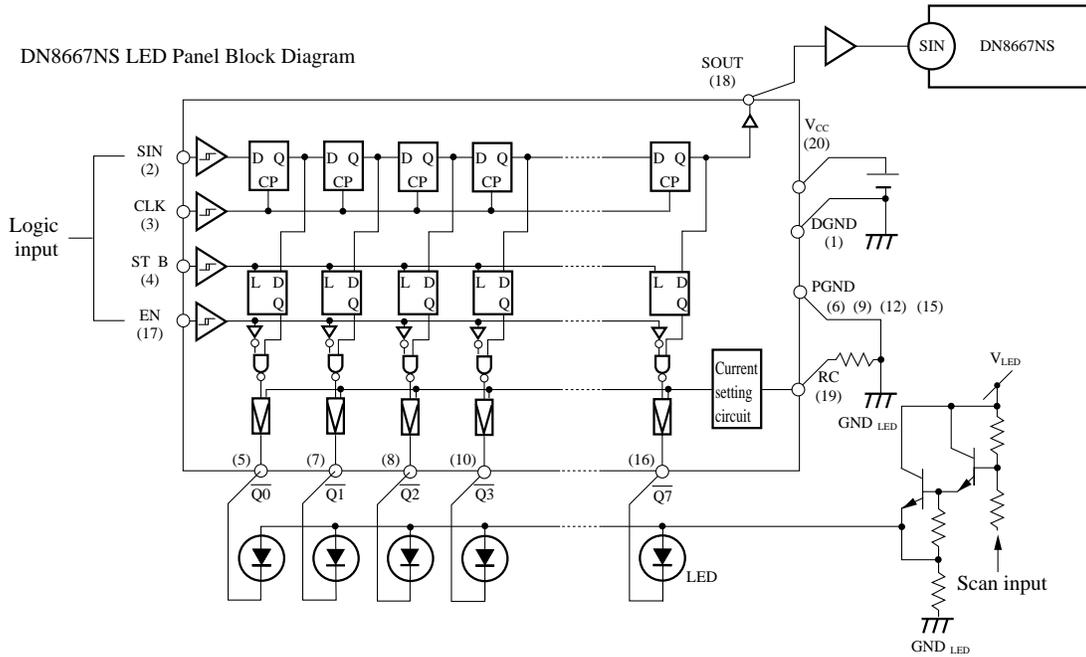
### ■ Pin Descriptions

Pin No.	Symbol	Pin name	Description
1	DGND	Digital ground	Digital ground
2	SIN	Serial data input	It is the serial data input terminal for shift register.
3	CLK	Clock input	The value of shift register shifts at the rising edge of clock input.
4	STB	Strobe input	Setting the STB input to "H" forwards the data of shift register to the latch. When the STB input is set to "L", even if the value of shift register changes, the value of latch is not changed.
5 7,8 10,11 13,14 16	$\overline{Qn}$	Driver output	It outputs signals by using the polarity opposite to that of data taken into the latch. For example, when the value of serial input is "H", the output becomes "L" level and the output is turned on. The output takes open collector form of NPN transistor.
6 9,12 15	PGND	Output ground	Output ground
17	EN	Enabling input	When the EN input is set to "H", all the outputs are turned off, independent of condition of shift register or latch driver.
18	SOUT	Serial data output	It is the terminal which performs the serial-output of data inputted from the SIN.
19	RC	Constant current setting input	It connects the external resistor between RC and GND and sets the current of output block. * Output current calculation : $I_{O(\overline{Qn})} \approx \frac{20 \times V_{CC} (V)}{R_{RC} (\Omega) + 90}$ ** RC terminal setting calculation : $I_{RC} \approx \frac{V_{CC} (V)}{2 \times R_{RC} (\Omega) + 180}$ or $R_{RC} (\Omega) \approx \frac{1}{2} \left( \frac{V_{CC} (V)}{I_{RC} (A)} - 180 \right)$
20	V <sub>CC</sub>	V <sub>CC</sub>	Supply terminal

\* Calculation example  $V_{CC} = 5V$   $R_{RC} = 910\Omega$   $I_{O(\overline{Qn})} \approx \frac{20 \times 5}{910 + 90}$   $I_{O(\overline{Qn})} = 100mA$

\*\* Calculation example  $V_{CC} = 5V$   $I_{RC} = 0.0025A$   $R_{RC} \approx \frac{1}{2} \left( \frac{5}{0.0025} - 180 \right)$   $R_{RC} \approx 910 (\Omega)$

Application Circuit

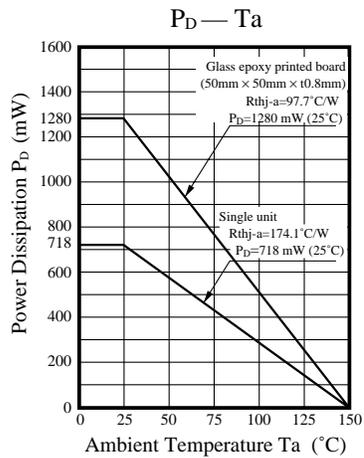


Function Table (Note)

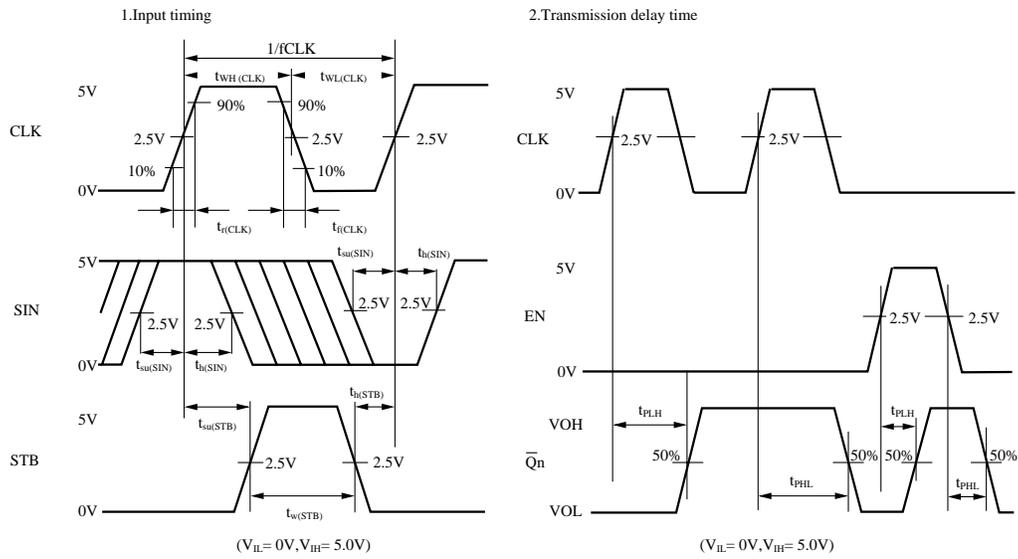
Input				Output			
CLK	STB	EN	SIN	$\overline{Q_0}$	$\overline{Q_m}$	$\overline{Q_7}$	SOUT
↑	H	L	$Q_n$	$\overline{Q_n}$	$\overline{Q_{m-1}}$	$\overline{Q_6}$	$Q_6$
↑	L	L	$Q_n$	nc	nc	nc	$Q_6$
↑	×	H	$Q_n$	H	H	H	$Q_6$
↓	×	×	$Q_n$	nc	nc	nc	nc

(Note)  
 H : High level,  
 L : Low level,  
 × : H or L  
 $Q_m, Q_n$  : H or L.  
 However, for  $\overline{Q_n}$ , "H"= OFF, "L"= ON.  
 ↑ : Shift from L to H,  
 ↓ : Shift from H to L  
 nc : No change

Characteristics Curve



■ Timing Chart



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