National Semiconductor

DP2460/DP2461, μA2460/μA2461 Servo Control Chips

General Description

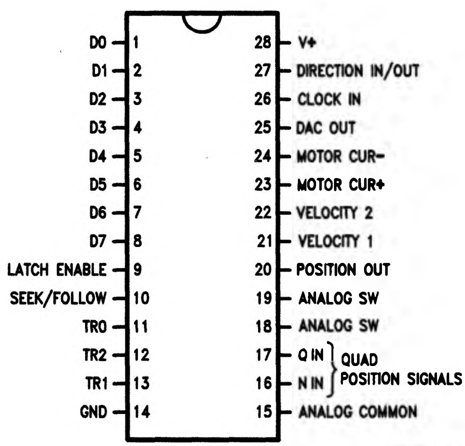
The DP2460 and DP2461 provide the analog signal processing required between a drive resident microprocessor and the servo power amplifier for Winchester disk closed loop head positioning. The DP2460 and DP2461 receive quadrature position signals from the servo channel; and from these, derive actual head seek velocity as well as position-mode off-track error. In the seek mode, the Digital to Analog Converter (DAC) is used to command velocity, while actual velocity is obtained by differentiating the quadrature position signals provided at V1 for external processing. The velocity signal (V2), obtained by integrating the motor current, is also available for extra damping, if desired. Further, the DAC may be used for detenting the head off-track for any purpose such as thermal compensation or soft-error retries.

Features

- Microprocessor compatible interface
- Quadrature di-bit compatible
- On board DAC
- Velocity V1 derived from position signal
- Velocity V2 derived from motor current
- Quarter-Track-Crossing signal outputs
- Minimal external components
- Compatible with DP2470 demodulator

Connection Diagrams

28-Lead Ceramic DIP



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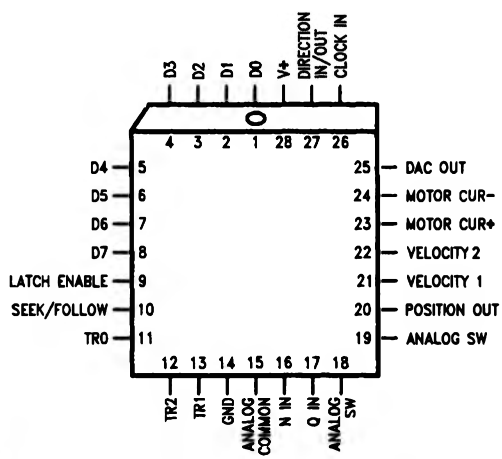
Top View

†Order Number μA2460DC or μA2461DC
††See NS Package Number J28A

28-Lead PLCC



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Top View

†Order Number μA2460QC or μA2461QC
††See NS Package Number V28A

†For most current order information, contact your local sales office.
††For most current package information, contact product marketing.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
PLCC	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
PLCC (Soldering, 10 sec.)	265°C

Internal Power Dissipation (Notes 1 and 2)	
28L—Ceramic DIP	2.50W
28L—PLCC	1.39W
Supply Voltage	15V Max
Analog Common Voltage	8.0V Max
All Inputs	V_{supply} Max

Note 1: T_J max = 150°C for the PLCC, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L—Ceramic DIP at 16.7 mW/°C, and the 28L—PLCC at 11.2 mW/°C.

Electrical Characteristics

T_A = 0°C to 70°C, V_{CC} = 12V, f_{CLK} = 2.0 MHz, Analog Common = 5.0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital I/O	Input Voltage LOW				0.8	V
	Input Voltage HIGH		2.0			
	Output Voltage LOW	I_{OL} = 2.5 mA			0.45	
	Output Voltage HIGH	I_{OH} = 40 μA	2.4			
	Input Load Current	V_I = 0V to V_{CC}			0.2	mA
Clock Input	Input Comparator Reference Level		2.0	2.5	3.0	V
	Input Impedance		15	20		kΩ
DAC	Linearity (Note 1)		−1		1	LSB
	Resolution			8.0		bits
	Differential Nonlinearity		Monotonicity Guaranteed			
	Full Scale Output Voltage	Direction in High	7.25	7.35	7.45	V
		Direction in Low	2.55	2.65	2.75	
	Zero Scale Voltage			5.0		
	Output Offset Voltage				±10	mV
	Settling Time (Notes 2, 4)	To ½ LSB All bits ON or OFF				μs
Position Inputs	Input Voltage Range		1.0		9.0	V
	Input Impedance		15	20		kΩ
Analog Switch	On Resistance	V_{CM} = 0V to 12V		100	200	Ω
	Off Leakage (Note 3)			2.0	100	nA
Position Output	Output Voltage Swing	R_L = 15k Follow Mode	1.0		9.0	V
	Voltage Gain		0.9		1.1	—
	Output Offset Voltage				±20	mV
Velocity Outputs	Output Voltage Swing	R_L = 15k	1.0		9.0	V
	Output Offset Voltage V2				±20	mV
	V1				15	
I_{CC}	Positive Supply	V_{CC} = 13.2V		10	15	mA
I_{SS}	Negative Supply	V_{CC} = 13.2V	−15	−10		mA
I_{AC}	Analog Common I		−2.0	0	2.0	mA
V1—Differentiator	Linearity	f_{CLK} = 1.0 MHz to 4.0 MHz; $f_{N/Q}$ ≤ 10 kHz		0.25		%
V2—Integrator	Linearity	f_{CLK} = 1.0 MHz to 4.0 MHz		1.0		%

Note 1: DAC Linearity is a function of the Clock frequency; Linearity at 1.0 MHz is typically ±½ LSB.

Note 2: DAC Settling Time is approx. 5.0 μs, plus a delay of maximum 32 × Clock period i.e., 5 + 32 μs at Clock = 1.0 MHz Minimum could be 5.0 μs.

Note 3: Equivalent to 50 MΩ.

Note 4: Guaranteed, but not tested in production.

Pin Description

Pin No.	Name	Function
INPUTS		
1–8	DAC Input Word (D_0–D_7)	Programs DAC output, 00000000 = Analog Command Lead 1 = LSB Lead 8 = MSB
9	Latch Enable	Allows present DAC input word to be latched.
10	Seek/Follow Mode	Configures the feedback loop for either seeking or track-following. (High = Seek, Low = Follow)
14	Ground	
15	Analog Common	Analog signal reference input level (5.0V)
16	N	Normal position input signal.
17	Q	Quadrature position input signal.
23	Motor Current +	Motor current sense input to motor current integrator.
24	Motor Current −	
26	Clock	4.0 MHz (maximum) input square wave.
27	Direction In/Out	Changes the polarity of DAC output from positive to negative consistent with the desired direction of head motion.
28	V+	12V supply

Pin No.	Name	Function
OUTPUTS		
11	Track 2^0 (TR0)	TTL signal whose frequency is 8 times N (or Q).
12	Track 2^2 (TR2)	TTL signal indicating N > Q (for DP2460). TTL signal whose frequency is 2 times N (or Q) (for DP2461).
13	Track 2^1 (TR1)	TTL signal indicating $\overline{N}$ > Q (for DP2460). TTL signal whose frequency is 4 times N (or Q) (for DP2461).
18	Analog Switch	Analog switch to be used externally for changing from seek to follow.
19	Analog Switch	
20	Position Output	Analog signal representing sensed off track amplitude.
21	Velocity 1	Analog output representing velocity processed from position signals N and Q.
22	Velocity 2	Analog output representing the integral of motor current.
25	DAC Output	Used to command velocity and position.

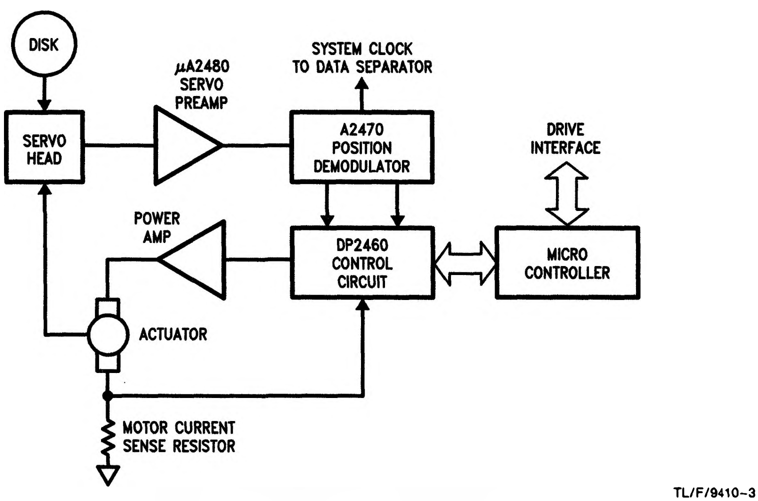

FIGURE 1. Head Actuator Control System

Functional Description

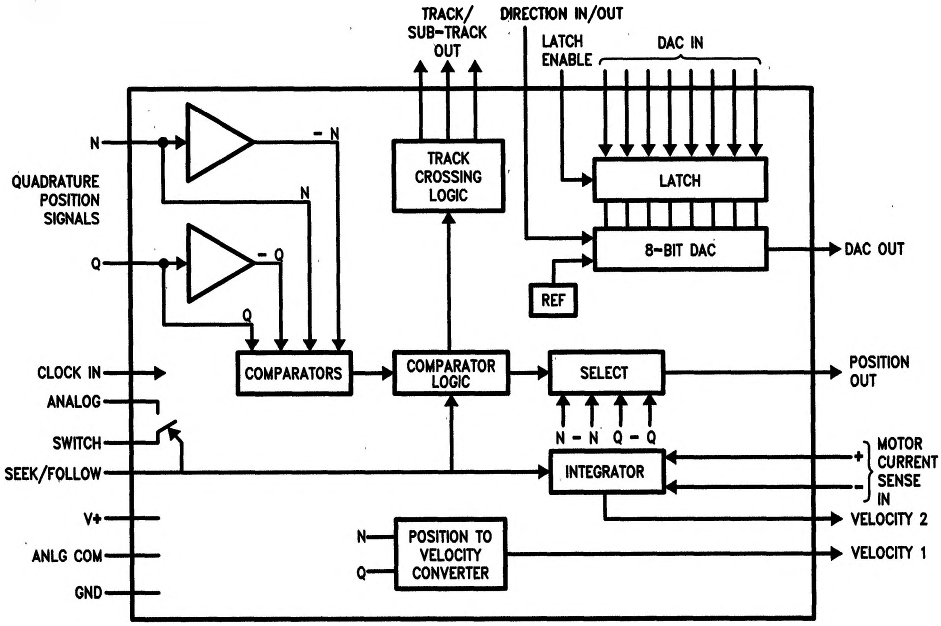

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FIGURE 2. Block Diagram

Figure 2 shows a block diagram of the DP2460/DP2461 Servo Controller.

POWER SUPPLY AND REFERENCE REQUIREMENTS

The DP2460/DP2461 is designed to operate from a single supply of 10V to 12V. Also required is a reference voltage of 5.0V called Analog Common which serves two functions; all analog signals will be referenced to this voltage and in addition the internal DAC will use it to set full scale.

A clock signal must be provided as a reference for the internal switched capacitor position differentiator and motor current integrator. The clock signal should be a sine or square wave between Analog Common and ground at a maximum frequency of 4.0 MHz.

All digital inputs and outputs are TTL compatible levels referenced to ground.

INPUT SIGNALS AND TRACK CROSSING OUTPUTS

The input format selected for position feedback is consistent with a large class of sensors that generate two cyclical output signals displaced in space phase by 90 degrees (quadrature signal pairs). These sensors include resolvers, inducto-syns, optical encoders, and most importantly, servo demodulators designed for rigid disk head position sensing.

The input signals N and Q are quadrature quasi triangular waveforms with amplitudes of $\pm 2.5V$ nominal referenced to Analog Common. The periods of the input signals are subdivided by internal comparators and logic and sent to the Track Crossing outputs T_0, T_1, and T_2. The relationship of these outputs to the inputs N and Q is shown in *Figure 3a* (for DP2460) and *Figure 3b* (for DP2461).

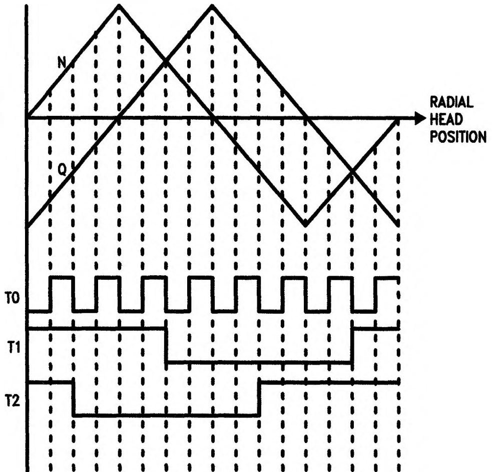
Note that different servo patterns may yield different numbers of track centerlines for each period of the quadrature signal pair. The relationship of T_0, T_1, and T_2 to N and Q is independent of track centerlines, leaving the correct interpretations to the microcontroller.

DAC

The DAC is an 8-bit, buffered input, voltage output digital to analog converter. The output voltage with an input code of all zeros is equal to Analog Common. Full scale is equal to Analog Common $\pm 2.35V$. The polarity depends on the Direction In Signal; Direction In High will result in a positive DAC output.

The DAC enable line when high will cause the DAC's input buffer to become transparent, i.e. input data will affect the output voltage immediately. When DAC enable is brought

Functional Description (Continued)



T0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
T1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1
T2	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1

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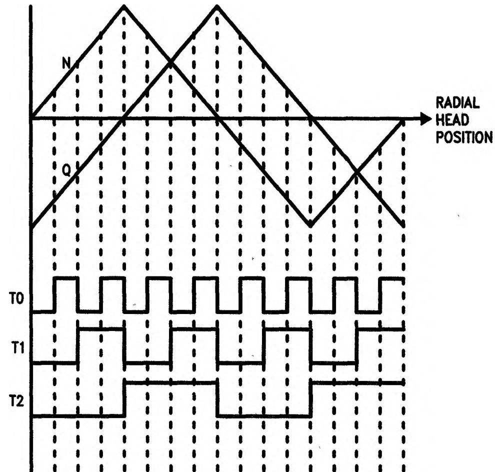
FIGURE 3a. Track Crossing Outputs (for DP2460)



T0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
T1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
T2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

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FIGURE 3b. Track Crossing Outputs (for DP2461)

low the data present on the input lines will be latched and any further changes to the input data will not change the output voltage. The DAC functions in both Seek and Follow Mode. During Seek Mode the DAC output is used as a velocity reference. In Follow Mode the DAC output can be summed into the position reference signal to offset the heads from track center.

ANALOG SWITCH

An uncommitted single pole single throw analog switch with an ON resistance of approximately 100Ω is provided. This switch is ON during Follow Mode.

MODE SELECT

The two major intended operating modes for the DP2460 are controlled by the microcontroller via the SEEK/FOLLOW input. Mode Select input high enables Seek Mode, low enables Track Follow Mode.

SEEK, when asserted by the microcontroller along with DIRECTION and a non-zero VELOCITY value as inputs, causes the actuator system to accelerate in the requested direction. During the ensuing motion, the actuator system will come under velocity feedback control. The velocity feedback signal is created by differentiation of the quadrature position signals and, additionally, by integration of motor current.

FOLLOW, the negation of SEEK, changes the feedback loop to a track-following or position mode. Position servos are typically second order systems and without loop compensation are potentially unstable. External components are used, along with the DP2460, to achieve stable track following performance. Velocity information (V1) is made available as an output in this mode to aid in stabilizing certain loops. If non-zero data is supplied to the velocity latches in this mode, it will result in a track offset in the direction indicated by DIRECTION IN/OUT. *Figure 4* shows typical seek operation.

POSITION OUTPUT

When the DP2460/DP2461 is set to Seek Mode the signal from Position Output lead is shown in *Figure 5*. This signal is made by switching the position inputs, (N and Q) through an inverter if required, ($\overline{N}$ and $\overline{Q}$) to the output using the track crossing signals. It can be used, if desired, to interpolate between DAC steps by attenuating it and summing it with the DAC output.

Track Follow Mode is entered when the heads are near the end of a seek, usually within one half to one track away from the target track centerline. The final setting to the track center is done by the position loop.

When the device is switched to Follow Mode, the position input signal (N, $\overline{N}$, Q or $\overline{Q}$) that is currently selected to the output is latched and the Position Out signal follows the selected position input signal until the device is switched back to Seek Mode. This implies that the switch to Follow Mode must not be made until the signal that will be the correct Position error signal for the target track is present at the output. If track centers are defined as the zero crossings of both N and Q this means that the switch to Follow Mode must be made less than one-half track away from the target track. (This is with respect to the convention of 4 tracks per encoder cycle, so switching must be done within 90° of the period of N or Q.)

Functional Description (Continued)

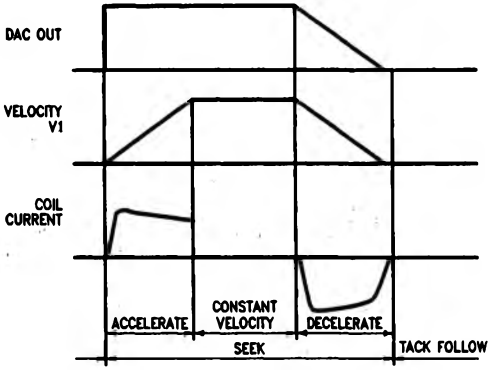

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FIGURE 4. Typical Seek

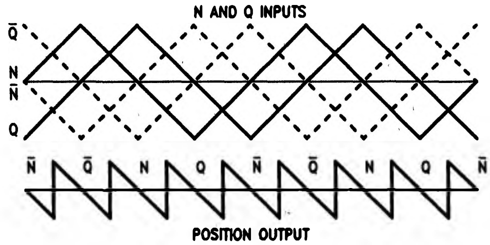

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FIGURE 5. Position Output during Seek Mode

VELOCITY OUTPUTS

There are two analog signal outputs representing velocity. The first (V1) is derived by differentiating the position input signals. The entire differentiator is on-chip, using switched capacitor techniques and requires no external components.

The transfer function of the differentiator is:

$$V_O = dv/dt\ (\text{input}) \times 14.3/f\ (\text{clock})\ \text{Hz}$$

As an example; a 10 kHz triangular signal pair into N and Q of 6.0V peak-to-peak amplitude (dv/dt = 120 kV/s) would result in a velocity voltage output of 1.716V referenced to Analog Common with a clock of 1.0 MHz. The polarity will be positive if N is leading Q by 90 degrees and negative if Q is leading N. This block functions during both Seek and Follow modes.

The second velocity output is obtained by integrating a voltage proportional to the current in the motor using the following function:

$$dv/dt\ (\text{out}) = V\,(+I_{in} - -I_{in}) \times 2 \times 10^{-4}\, f\ (\text{clock})\ \text{Hz}.$$

The motor current integrator output is clamped to Analog Common during Follow Mode and is released at the initiation of a seek.

Figure 6 shows a typical application setup for the Servo Control chip.

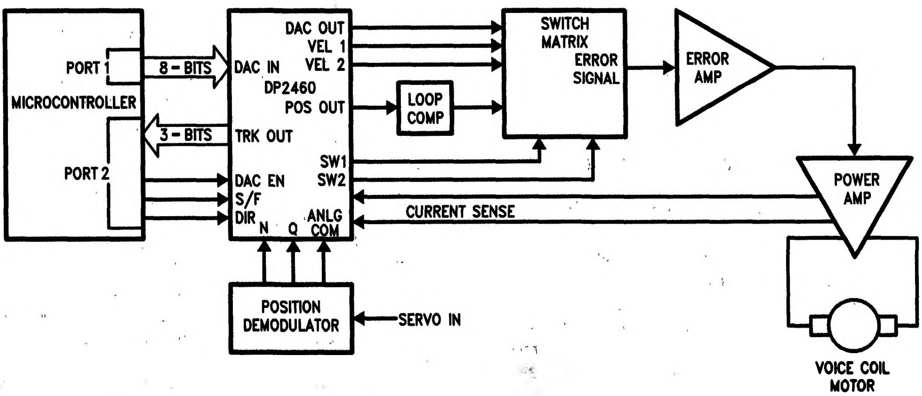

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FIGURE 6. Typical Application Setup