National Semiconductor

DP501X/DP501XR/μA501X/μA501XR Series 6 or 8 Channel Read/Write Circuit

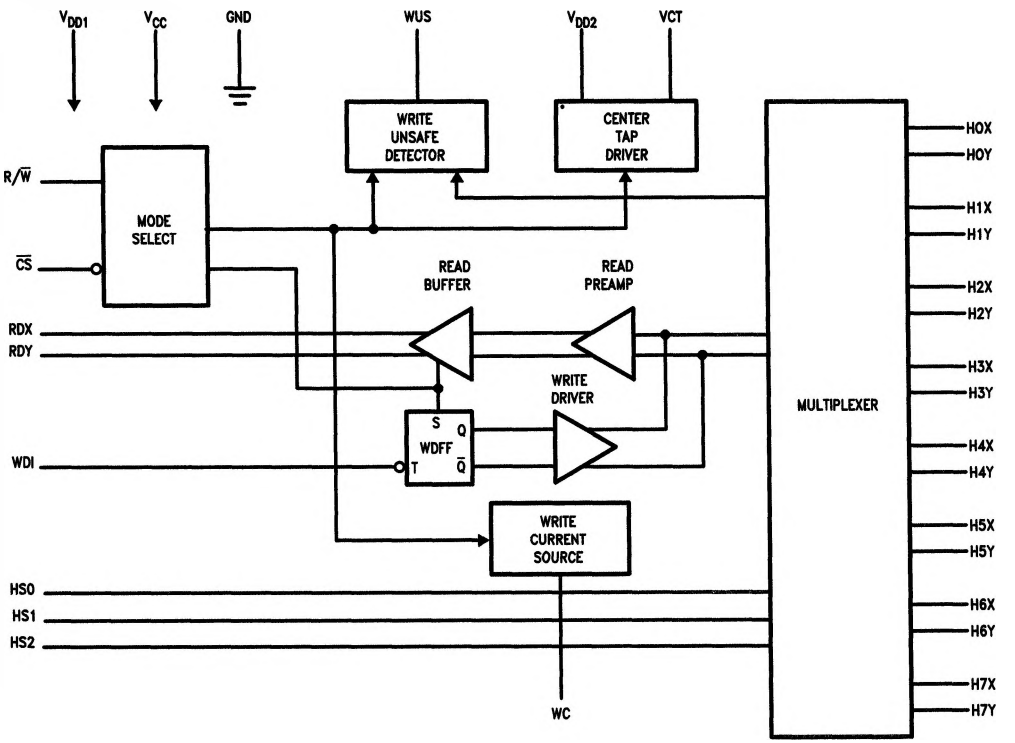
General Description

The μA501X/μA501XR devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for eight channels. The μA501X/μA501XR requires +5.0V and +12V power supplies and is available in a variety of packages. The μA501XR differs from the μA501X by having internal damping resistors.

Features

- +5.0V, +12V power supplies
- Single- or multi-platter Winchester drives
- Designed for center-tapped ferrite heads
- Programmable write current source
- Easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals

Block Diagram



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Note: Caution: Use handling procedures necessary for a static sensitive component.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP and Flatpak	−65°C to +175°C
Molded DIP and PLCC	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP and Flatpak (Soldering, 60 seconds)	300°C
Molded DIP and PLCC (Soldering, 10 seconds)	265°C
Internal Power Dissipation (Notes 2 & 3)	
28L-Ceramic DIP	2.50W
28L-Plastic DIP	1.92W
32L-Brazed Flatpak	1.88W
40L-Ceramic DIP	2.65W
40L-Plastic DIP	2.5W
28L-Plastic LCC	1.39W
44L-Plastic LCC	1.92W
DC Supply Voltage	
V_{DD1} and V_{DD2}	−0.3V to +14V
V_{CC}	−0.3V to +6.0V
Digital Input Voltage Range	−0.3V to V_{CC} + 0.3V
Head Port Voltage Range	−0.3V to V_{DD} + 0.3V
WUS Port Voltage Range	−0.3V to +14V
1 Write Current	60 mA
Output Current	
RDX and RDY	−10 mA
VCT	−60 mA
WUS	+12 mA

Note 1: All voltages referenced to GND.

Note 2: $T_{J\ MAX}$ = 150°C for the Plastic, and 175°C for the Ceramic.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L-Ceramic DIP at 16.7 mW/°C, the 28L-Plastic DIP at 15.3 mW/°C, the 32L-Brazed Flatpak at 12.5 mW/°C, the 40L-Ceramic DIP at 20.1 mW/°C, the 40L-Plastic DIP at 20 mW/°C, the 28L-Plastic LCC at 11.2 mW/°C, and the 44L-Plastic LCC at 15.3 mW/°C.

Recommended Operating Conditions

DC Supply Voltage	
V_{DD1}	12V ±10%
V_{CC}	5V ±10%
Head Inductance (Lh)	5.0 μH to 15 μH
Damping Resistor (External)	
RD (DP501X Only)	500Ω to 2000Ω
RCT Resistor	90Ω ±5.0% (½W)
Write Current (I_W)	25 mA to 50 mA

DC Electrical Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ +70°C, unless otherwise specified

Symbol	Parameter		Conditions		Min	Max	Units
I_{CC}	Supply Current		Read/Idle Mode			25	mA
			Write Mode			25	
I_{DD}	Supply Current		Idle Mode			20	mA
			Read Mode			40	
			Write Mode			20 + I_W	
P_C	Power Consumption		25°C ≤ T_J ≤ 135°C	Idle Mode		400	mW
				Read Mode		650	
				Write Mode, I_W = 50 mA, RCT = 90Ω		880	
				Write Mode, I_W = 50 mA, RCT = 0Ω		1060	
V_{IL}	Digital Inputs:	Input Voltage LOW			−0.3	0.8	V
V_{IH}		Input Voltage HIGH			2.0	V_{CC} + 0.3	V
I_{IL}		Input Current LOW	V_{IL} = 0.8V		−0.4		mA
I_{IH}		Input Current HIGH	V_{IH} = 2.0V			100	μA
V_{OL}	WUS Output		I_{OL} = 8.0 mA			0.5	V
I_{OH}			V_{OH} = 5.0V			100	μA
V_{CT}	Center Tap Voltage		Read Mode		4.0 (typ)		V
			Write Mode		6.0 (typ)		V

Write Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ +70°C, I_W = 45 mA, Lh = 10 μH, Rd = 750Ω (DP501X only), f(Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, unless otherwise specified

Parameter	Conditions	Min	Max	Units
Write Current Range		10	50	mA
Write Current Constant "K"		129	151	V
Differential Head Voltage Swing		7.5		V (pk)
Unselected Head Transient Current	5.0 μH ≤ Lh ≤ 9.5 μH		2.0	mA (pk)
Differential Output Capacitance			15	pF
Differential Output Resistance	Without Internal Resistors	10k		Ω
	With Internal Resistors	560	940	
WDI Transition Frequency	WUS = LOW	250		kHz
Head Current Gain to I_{WC} $\left(\frac{I_W}{I_{WC}}\right)$		20 (typ)		mA/mA
Unselected Head Leakage	Sum of X and Y Side Current		85	μA

Read Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, I_W = 45 mA, CL (RDX, RDY) ≤ 20 pF, (V_{IN} is referenced to V_{CT}), 0°C ≤ T_A ≤ + 70°C, Lh = 10 μH, Rd = 750Ω, f(Data) = 5.0 MHz unless otherwise specified

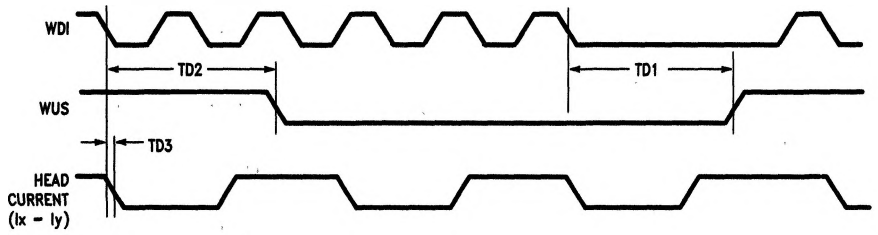
Characteristic	Condition		Min	Max	Unit
Differential Voltage Gain	V_{IN} = 1.0 mV_{PP} at 300 kHz RL (RDX), RL (RDY) = 1.0 kΩ (AC coupled)		80	120	V/V
Dynamic Range	Input Voltage, V_I, where Gain Falls by 10% V_{IN} = V_I + 0.5 mV_{PP} at 300 kHz		−3.0	3.0	mV
Bandwidth (−3 dB)	|Zs| < 5.0Ω, V_{IN} = 1.0 mV_{PP}		30		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5.0 MHz			23	pF
Differential Input Resistance	f = 5.0 MHz, V_{IN} ≤ 6 mV_{PP}	Without Internal Resistors	2k		Ω
		With Internal Resistors	530	790	
Input Bias Current (per Side)				100	μA
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100 mV_{PP} at 5.0 MHz		50		dB
Power Supply Rejection Ratio	100 mV_{PP} at 5.0 MHz on V_{DD1}, V_{DD2}, or V_{CC}		45		dB
Channel Separation	Unselected Channels: V_{IN} = 100 mV_{PP} at 5.0 MHz and Selected Channel: V_{IN} = 0 mV_{PP}		45		dB
Output Offset Voltage			−480	480	mV
Common Mode Output Voltage		Read Mode	5.0	7.0	V
		Write/Idle Mode	4.3 (typ)		
Single Ended Output Resistance	f = 5.0 MHz			30	Ω
External Resistive Load (AC Coupled to Output)	Per Side to GND		100		Ω
Leakage Current (RDX, RDY)	5.0 < RDX, RDY < 8.0V Write or Idle Mode		−50	50	μA
Center Tap Output Impedance	0 ≤ f ≤ 5.0 MHz			150	Ω
Output Current	AC Coupled Load RDX to RDY		2.0		mA

Switching Characteristics

V_{DD1} = 12V ±10%, V_{CC} = 5.0V ±10%, 0°C ≤ T_A ≤ +70°C, I_W = 45 mA, Lh = 10 μH, Rd = 750Ω, f(Data) = 5.0 MHz, unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
R/$\overline{W}$	R/$\overline{W}$ to Write	Delay to 90% of Write Current		600	ns
	R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% Decay of Write Current		600	
$\overline{CS}$	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope		600	ns
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		600	
HS0 HS1 HS2	to Any Head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope		600	ns
WUS	Safe to Unsafe—TD1	I_W = 50 mA	1.6	8.0	μs
	Unsafe to Safe—TD2	I_W = 20 mA		1.0	
Head Current	Propagation Delay—TD3	Lh = 0 μH, Rh = 0Ω from 50% Points		30	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time		2	
	Rise/Fall Time	10%–90% Points		20	

Write Mode Timing Diagram



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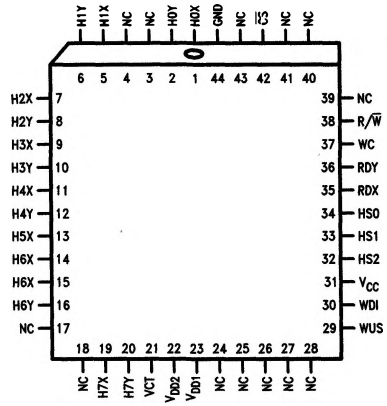
Connection Diagrams

44-Lead PLCC



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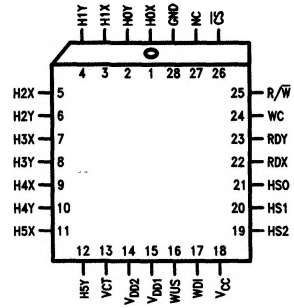
Top View

Order Number μA5018QC or μA5018RQC
See NS Package Number V44A

28-Lead PLCC



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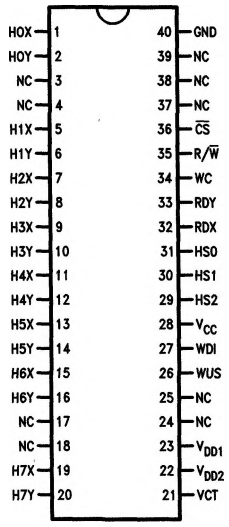
Top View

Order Number μA5016QC or μA5016RQC
See NS Package Number V28A

40-Lead DIP



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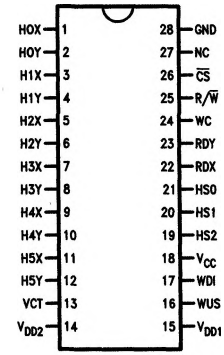
Top View

Ceramic DIP
***Order Number μA5018DC or μA5018RDC**
****See NS Package Number J40A**

Molded DIP
***Order Number μA5018PC or μA5018RPC**
****See NS Package Number N40A**

28-Lead DIP



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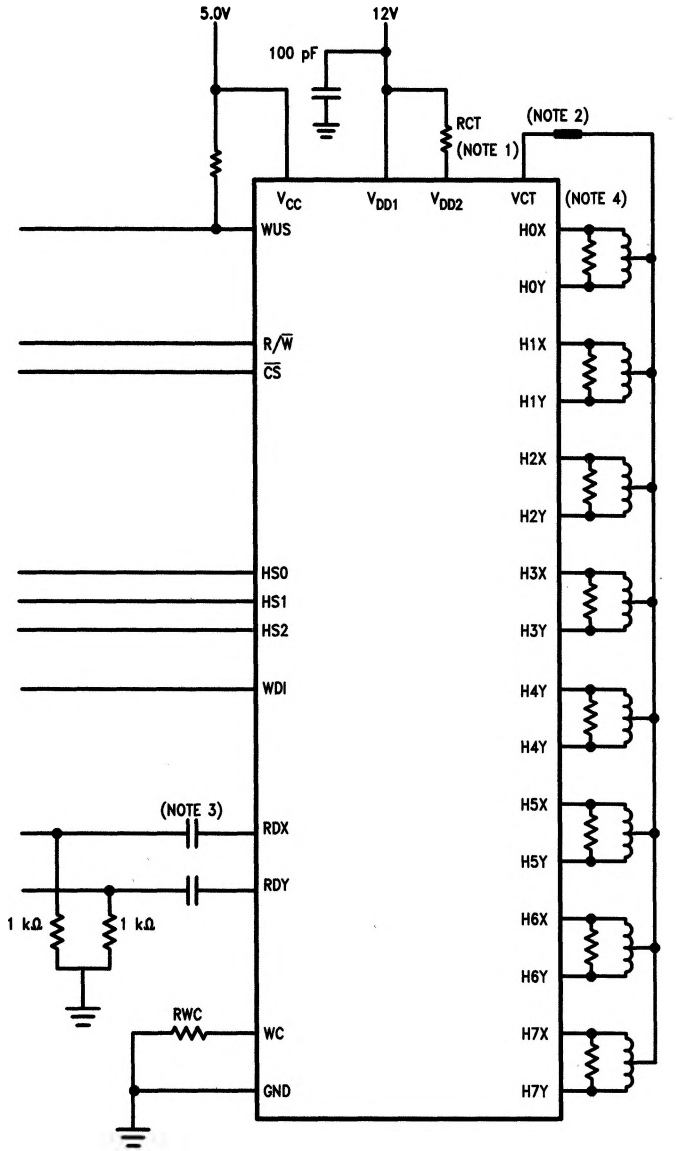
Top View

Order Number μA5016DC or μA5016RDC
See NS Package Number J28A

Order Number μA5016PC or μA5016RPC
See NS Package Number N28B

*For most current order information, contact your local sales office.
**For current package information, contact product marketing.

Application Information



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Note 1: An external ½W resistor, RCT, given by RCT = 90 (50/I_W)Ω, where I_W is in mA can be used to limit internal power dissipation. Otherwise connect V_{DD2} to V_{DD1}.

Note 2: A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics.

Note 3: Limit DC current from RDX and RDY to 100 μA and load capacitance to 20 pF.

Note 4: Damping resistors required on DP501X only.

Pin Descriptions

TABLE I. Description of Lead Functions

Name	Functions
HS0–HS2	Head Select
$\overline{CS}$	Chip Select: a low level enables device.
R/$\overline{W}$	Read/$\overline{Write}$: a high level selects read mode.
WUS	Write Unsafe: a high level indicates an unsafe writing position.
WDI	Write Data In: a negative transition toggles the direction of the head current.
H0X–H7X H0Y–H7Y	X, Y Head Connections
RDX, RDY	X,Y Read Data: differential read signal out.
WC	Write Current: used to set the magnitude of the write current.
VCT	Voltage Center Tap: voltage source for head center tap.
V_{CC}	+5.0V
V_{DD1}	+12V
V_{DD2}	Positive power supply for the center tap voltage source.
GND	Ground

Circuit Operation

The μA510X/μA501XR functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables II and III. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the μA510X/μA501XR as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

I_W = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from lead WC to GND.

TABLE II. Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	X	Idle

TABLE III. Head Select

HS2	HS1	HS0	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low Level

1 = High Level

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

READ MODE

In the Read mode the μA510X/μA501XR is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the chip deselect mode. This eliminates the need for external gating of the write current source.