National Semiconductor

DP83223A
TWISTER™ High Speed Networking Transceiver Device

General Description

The DP83223A Twisted Pair Transceiver is an integrated circuit capable of driving and receiving either binary or MLT-3 encoded datastreams. The DP83223A Transceiver is designed to interface directly with standards compliant FDDI and 100BASE-TX chip sets allowing low cost data links over copper based media. The DP83223A allows links of up to 100 meters over both Shielded Twisted Pair (STP) and datagrade Unshielded Twisted Pair (UTP) or equivalent. The electrical performance of the DP83223A meets or exceeds all performance parameters specified in the ANSI X3T12 TP-PMD draft standard and the IEEE 802.3 100BASE-TX Fast Ethernet Specification. The DP83223A also provides important features such as baseline restoration, TRI-STATE® capable transmit outputs, and controlled transmit output edge rates.

Features

- Compliant with ANSI X3T12 TP-PMD draft standard
- Compliant with IEEE 802.3 100BASE-TX Ethernet draft standard
- Integrated baseline restoration circuit
- Integrated transmitter and receiver with adaptive equalization circuit
- Programmable binary or MLT-3 operation
- Isolated TX and RX power supplies for minimum noise coupling
- Controlled transmit output edge rates for reduced EMI
- Tri-State capable current transmit outputs
- Loopback feature for board diagnostics
- Programmable transmit voltage amplitude

Block Diagram

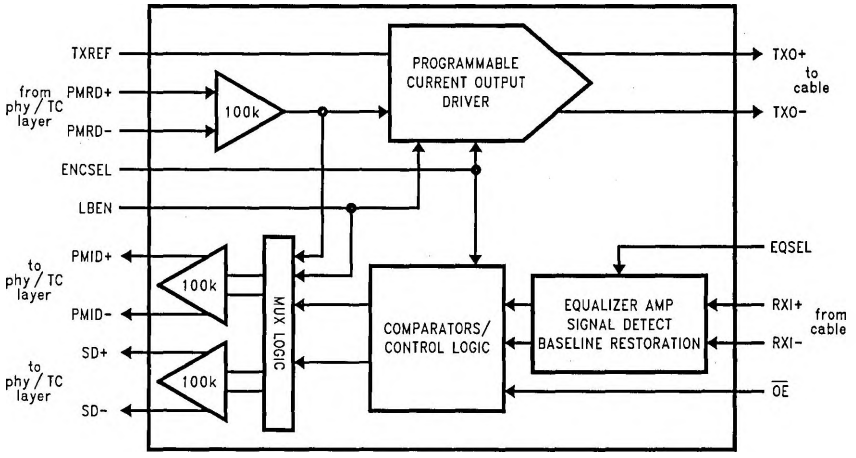

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FIGURE 1. DP83223A Transceiver Block Diagram

1.0 Functional Description

OVERVIEW

The DP83223A TWISTER is an enhanced version of the DP83223 transceiver device. The new DP83223A device has been designed to be backward compatible with the existing DP82223 device such that current PMD designs based on the DP83223 will accept, without modification, the new DP83223A device.

The DP83223A consists of seven major functional blocks as shown in *Figure 1*. The Transmit section consists of a 100K ECL input buffer for PMRD± and the Programmable Current Output Driver. The Programmable Current Output Driver can be configured to convert the incoming binary (NRZ or NRZI) datastream to a current sourced MLT-3 encoded datastream or current sourced binary datastream depending on the state of the ENCSEL input pin.

The Receive section consists of the following functional blocks: a differential input Equalization Amplifier with Signal Detect and baseline restoration circuitry, signal Comparators with Control Logic, Loopback Multiplexer Logic, and differential 100K ECL output drivers for PMID and Signal Detect.

In adaptive or full equalization mode, as selected by the EQSEL input pin, the receive data is first equalized and then amplified for signal detection. If the receive equalizer is turned off, the data is then only amplified for signal detection. In either case, the average baseline of the incoming signal is continuously monitored and restored given any baseline wander that may occur.

The Comparator/Control Logic block performs several functions. Primarily, the comparators either quantize and decode incoming MLT-3 into binary or simply quantize the incoming binary signal depending on the state of the ENCSEL input. The control logic receives input from $\overline{OE}$ and ENCSEL enabling final signal detect indication and control of data regeneration.

The Loopback Multiplexer logic performs the function of routing the transmit data at the PMRD± inputs to either the PMID± pins (loopback enabled) or to the TXO± current outputs (normal operation).

Finally, 100K ECL output drivers are used to drive both PMID± receive data and SD± Signal Detect data to the appropriate clock recovery circuit.

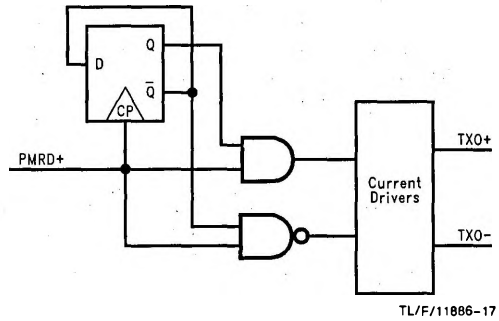
1.1 ENCODE/DECODE

The PMRD± inputs of the DP83223A TWISTER will accept either NRZ or NRZI PECL binary up to 155 Mbps. With the ENCSEL (Encode Select) input pin forced low, binary data is asynchronously encoded to a current sourced MLT-3 data stream for transmission. For twisted pair FDDI or 100BASE-TX implementations, NRZI data (as provided by the Physical Layer) is required.

With ENCSEL forced high, incoming binary data is not encoded but is directly converted to a current sourced binary datastream.

The receiver function of the DP83223A TWISTER is also determined by the state of the ENCSEL pin. With ENCSEL forced low, the receiver will decode the incoming MLT-3 data stream to the original binary version. This decoded binary signal is converted to PECL levels and then routed to the PMID± outputs. With ENCSEL forced high, the incoming binary data is regenerated, converted to PECL levels and routed to the PMID± outputs.

The process of encoding binary to MLT-3 and decoding MLT-3 back to binary is illustrated in the simplified logic circuits and associated bit patterns given in *Figures 2* and *3*.



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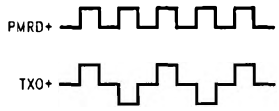

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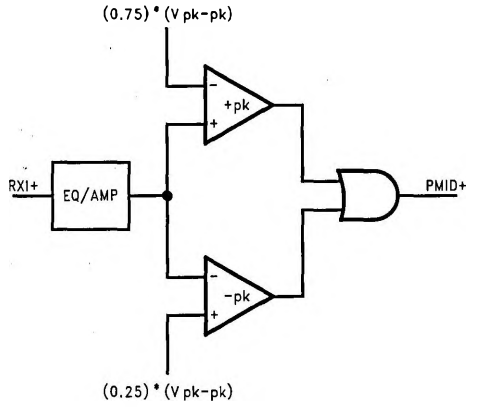
FIGURE 2. Binary to MLT-3 Encoding



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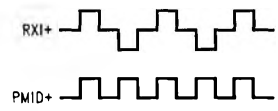

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FIGURE 3. MLT-3 to Binary Decoding

1.0 Functional Description (Continued)

1.2 BASELINE RESTORATION

The DP83223A TWISTER has been designed to correct for baseline wander as defined in the ANSI FDDI TP-PMD specification. Baseline wander can generally be defined as the change in the average DC content, over time, of an AC coupled digital transmission over a given transmission medium. (i.e., copper wire)

Baseline wander results from the interaction between the low frequency components of a bit stream being transmitted and the frequency response of the AC coupling component(s) within the transmission system. If the low frequency content of the digital bit stream goes below the low frequency pole of the AC coupling transformers then the droop characteristics of the transformers will dominate resulting in potentially serious baseline wander.

The digital oscilloscope plot provided in *Figure 4* illustrates the severity of the baseline wander event generated by the frame specified in the ANSI FDDI TP-PMD standard. This event consists of a DC offset of approximately 750 mV with a period of approximately 360 μs. Left uncompensated, this event would cause many bit errors which could potentially isolate the receiving node from the FDDI network.

It is interesting to note that the probability of a baseline wander event serious enough to corrupt data is very low. In fact, it is reasonable to virtually bound the occurrence of a baseline wander event serious enough to cause bit errors to a legal but premeditated, artificially constructed bit sequence loaded into the original MAC frame. Several studies have been conducted to evaluate the probability of various baseline wander events for FDDI transmission over copper. Contact the X3T12 ANSI group for further information.

1.3 TRANSMIT AMPLITUDE CONTROL

The transmit amplitude of the signal presented at the TXO output pins can be controlled by varying the value of resistance between TXREF and TXGND. This TXREF resister, R_{REF}, sets up a reference current which determines the final output current at TXO±. The DP83223A TWISTER will also automatically set the TXREF scaling factor to provide the correct transmit amplitude based on the selected mode of operation (MLT-3 or binary) without having to change the value of the TXREF resistor.

For 100Ω Category-5 UTP cable implementations, the value of the TXREF resister (R_{REF}) is currently set at 510Ω. This will yield either a 2 $V_{pk\text{-}pk}$ differential transmit amplitude for MLT-3 or a 1 $V_{pk\text{-}pk}$ differential transmit amplitude for binary. The following equations are useful for calculating R_{REF}:

$$R_{REF} = \frac{10.24 * Z_{CABLE}}{V_{OUT}\,(\text{MLT-3})} \quad \text{or} \quad R_{REF} = \frac{5.12 * Z_{CABLE}}{V_{OUT}\,(\text{binary})}$$

where:

- R_{REF} is the TX amplitude reference resistor in Ohms (Ω)
- Z_{CABLE} is the characteristic differential impedance of the desired twisted pair cable (Ω)
- V_{OUT} is the differential peak-peak output voltage in Volts (V)
- 10.24 and 5.12 are related to the reference scaling factors

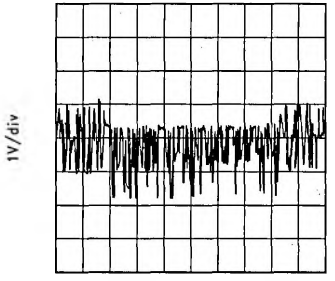

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FIGURE 4. Baseline Wander Event

1.0 Functional Description (Continued)

1.4 TRANSITION TIME CONTROL

The transition times of the TXO± output signals are digitally synthesized resulting in closely matched and controlled rise and fall times. As with the previous TWISTER, the new DP83223A TWISTER incorporates this unique feature which significantly reduces the need for external filtering of the transmitted signal. The combination of these controlled edge rates and inexpensive magnetics (without additional filtering) generates clean rise and fall times compliant with the ANSI X3T12 TP-PMD draft standard and the IEEE 802.3 100BASE-TX Fast Ethernet Specification. In addition, control of the transmitter transition times reduces the EMI related board layout sensitivities. This offers a distinct advantage over transceivers dependent on external filtering for transition time control.

Figure 5 compares the power spectrum of two transmitters each driving a 1V binary scrambled HALT bitstream into a 100Ω load through a typical 350 μH 1:1 transformer. The power spectrum curve exhibiting lower relative power is from the DP83223A TWISTER transmitter with contolled output transition times. The curve exhibiting the higher relative power is from a transmitter which does not contol the output transition time and therefore, would require additional external filtering to limit bandwidth and radiated emmisions. The curves in *Figure 6* make the same comparison for 2V MLT-3 transmission where the DP83223A TWISTER again exhibits lower relative power, eliminating the need for additional external transmit filtering.

1.5 ADAPTIVE EQUALIZATION

When transmitting data at high speeds over copper twisted pair cable, frequency dependent attenuation becomes a concern. In high speed twisted pair signalling the frequency content of the transmitted signal can vary greatly during normal operation based primarily on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the transmission.

In order to ensure quality transmission when employing MLT-3 encoding, (and to a lesser extent, binary) the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will over-compensate for shorter, less attenuating lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal regardless of the of the installed media.

In order to implement receiver adaptive equalization, a known relationship between transmit output amplitude and a receive input reference must be specified and controlled. Given these two parameters, the adaptive equalizer can determine the approximate cable length via signal attenuation at certain frequencies and actively compensate for cable variations.

The curves given in *Figure 7* provide insight to the actual attenuation at certain frequencies for given cable lengths. This is derived from the worst case frequency vs. attenuation figures as specified in the EIA/TIA Bulletin TSB-36. These curves indicate the significant variations in signal attenuation that must be compensated for by the receive adaptive equalization circuit.

As a measure of operation, *Figures 8* through *13* indicate the performance and function of the adaptive equalizer in terms of jitter for a 2 V_{pk-pk} differential MLT-3 signal.

Figure 8 represents a scrambled HALT, transmitted over 0 Meters of Category-5 cable as measured at the AII (Active Input Interface) of the receiver. *Figure 9* represents the jitter of the recovered PECL data as measured differentially at the PMID± outputs. *Figures 10* and *11* represent the performance over 50 Meters of Category-5 Cable and *Figures 12* and *13* represent performance over 100 Meters of Category-5 cable.

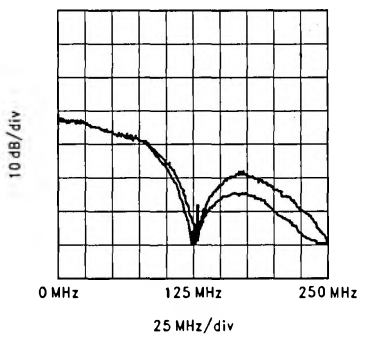

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FIGURE 5. 1V Binary Power Spectrum with and without Edge Rate Control

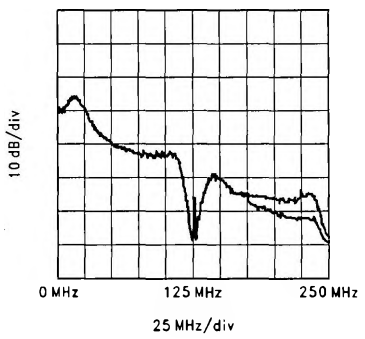

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FIGURE 6. 2V MLT-3 Power Spectrum with and without Edge Rate Control

1.0 Functional Description (Continued)

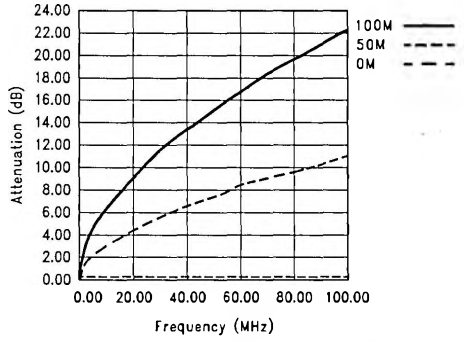

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FIGURE 7. EIA/TIA Attenuation vs Frequency for 0, 50 and 100 Meters of CAT-5 Cable

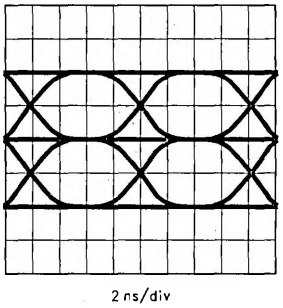

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FIGURE 8. MLT-3 Signal Measured at All after 0M of CAT-5 Cable

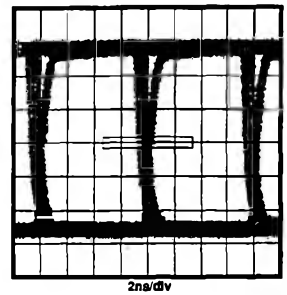

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FIGURE 9. Recovered ECL Peak Total Jitter for 0M of CAT-5 Cable (MLT-3) 660 ps

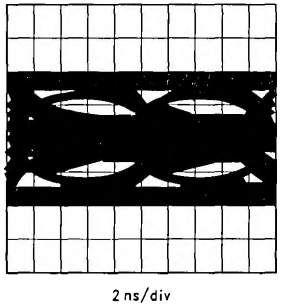

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FIGURE 10. MLT-3 Signal Measured at All after 50M of CAT-5 Cable

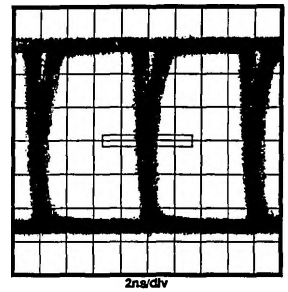

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FIGURE 11. Recovered ECL Peak Total Jitter for 50M of CAT-5 Cable (MLT-3) 1.0 ns

1.0 Functional Description (Continued)

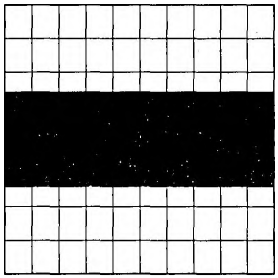

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FIGURE 12. MLT-3 Signal Measured at All after 100M of CAT-5 Cable

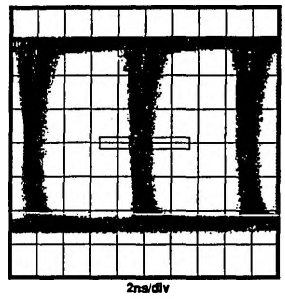

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FIGURE 13. Recovered ECL Peak Total Jitter for 100M of CAT-5 Cable (MLT-3) 1.08 ns

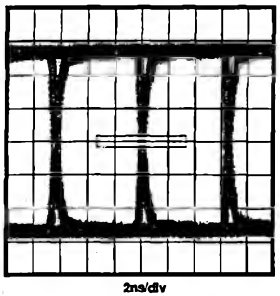

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FIGURE 14. Recovered ECL Peak Total Jitter for 0M of CAT-5 Cable (binary) 340 ps

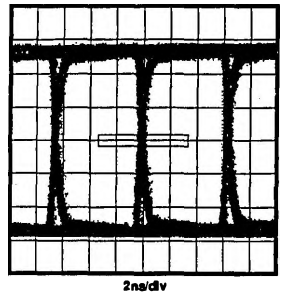

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FIGURE 15. Recovered ECL Peak Total Jitter for 50M of CAT-5 Cable (binary) 480 ps

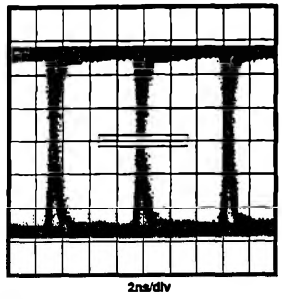

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FIGURE 16. Recovered ECL Peak Total Jitter for 100M of CAT-5 Cable (binary) 520 ps

1.0 Functional Description (Continued)

1.6 JITTER PERFORMANCE

This section provides additional jitter performance measured using the DP83223A TWISTER transceiver. The TWISTER was configured to transmit a scrambled HALT data stream over various lengths of cable in both MLT-3 and binary modes of operation. The 0, 50 and 100 Meter plots provided in *Figures 9, 11* and *13* represent the MLT-3 mode total jitter performance.

Figures 14, 15 and *16* indicate the jitter performance in the binary mode of operation also over 0, 50 and 100 Meter Category-5 cable lengths. All of these jitter results are given as the peak total jitter resulting from the combination of the transmitter, cable, and receiver.

1.7 SIGNAL DETECT

The signal detect function of the DP83223A TWISTER is incorporated to meet the specifications mandated by the ANSI FDDI TP-PMD Standard as well as the IEEE 802.3 100BASE-TX Standard.

The signal detect turn-on and turn-off thresholds for the TWISTER for both binary and MLT-3 modes of operation are illustrated in *Figure 17*. It is important to note that the signal detect function occurs after adaptive equalization and amplification of the received signal.

1.8 OUTPUT ENABLE

The DP83223A TWISTER provides an output enable/disable function which is pin selectable via the Output Enable bar pin ($\overline{OE}$). This pin was formerly labeled Cable Detect bar ($\overline{CDET}$) on the previous DP83223 TWISTER. With $\overline{OE}$ set to a logic high level, the TXO± current outputs are both turned off. This causes the TXO outputs to effectively TRI-STATE regardless of the selected mode of operation (MLT-3 or Binary). Additionally, the PMID± PECL outputs are forced to a steady state and the Signal Detect (SD+) output is forced to a logic low (SD+ = 0 and SD− = 1). With OE set to a logic low level, the TWISTER functions normally.

1.9 EQUALIZATION SELECT

The DP83223A TWISTER provides the added flexibility of controlling the type of receive equalization required for a given implementation. While adaptive equalization is the preferred method of cable compensation for TP-PMD FDDI and 100BASE-TX, the ability to switch the equalizer completely off or to a fixed maximum is provided.

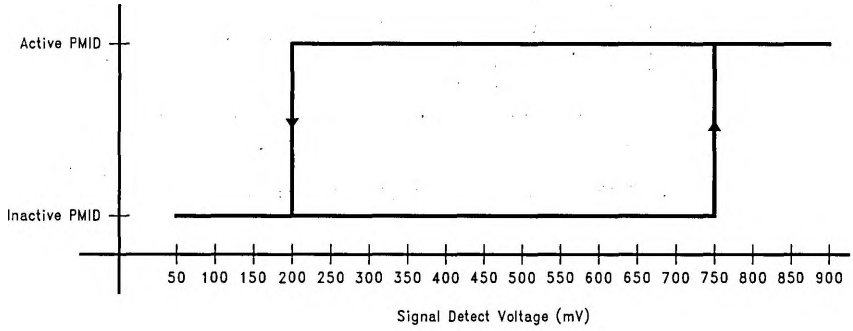

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FIGURE 17. Signal Detect

1.0 Functional Description (Continued)

1.10 LOOPBACK OPERATION

As with the previous TWISTER, the Loopback function of the DP83223A TWISTER (LBEN = 1) routes the signal at the PMRD inputs directly to the PMID outputs and forces SD+ high. However, the new TWISTER also forces the TXO± outputs to a true Quiet line state. This is accomplished by forcing the TXO± outputs to a balanced state where each output sources ½ the peak current required for the selected mode of operation (MLT-3 or Binary).

Figure 18 illustrates the normal and true Quiet line signalling for normal and loopback functions while in the MLT-3 mode of operation. *Figure 19* illustrates normal and loopback signalling for binary operation. Both figures are based on implementations using 100Ω Cat-5 UTP cable.

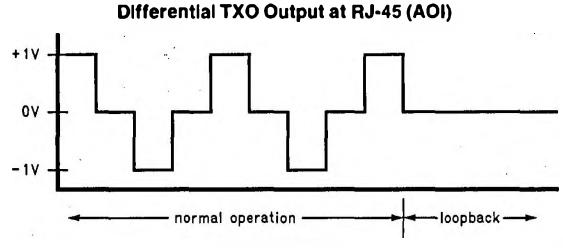

FIGURE 18. TXO True Quiet during Loopback (MLT-3 Mode)

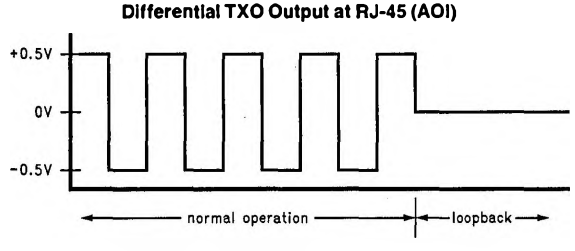

FIGURE 19. TXO True Quiet during Loopback (Binary Mode)

2.0 System Connection Diagrams

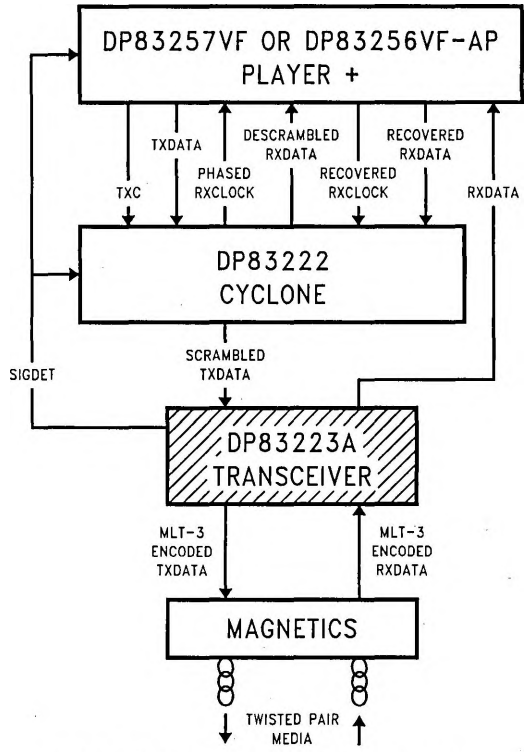

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FIGURE 20. Typical TP-FDDI System Connection

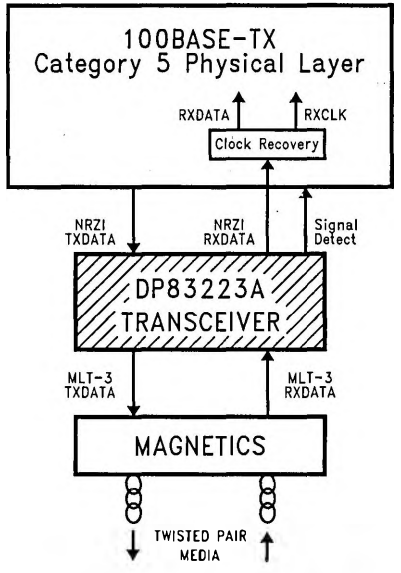

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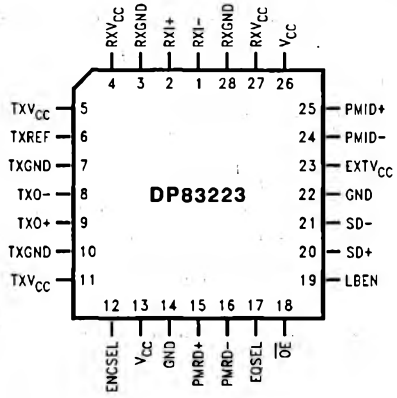
FIGURE 21. Typical 100BASE-TX System Connection

3.0 Pinout Information



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28-Pin PLCC
FIGURE 23. Pin Configuration

3.1 PINOUT SUMMARY

Signal	Pin No.	Description	Type
V_{CC}	13, 26	V_{CC}	Supply
GND	14, 22	GND	Supply
RXV_{CC}	4, 27	Receive V_{CC}	Supply
RXGND	3, 28	Receive GND	Supply
TXV_{CC}	5, 11	Transmit V_{CC}	Supply
TXGND	7, 10	Transmit GND	Supply
$EXTV_{CC}$	23	External V_{CC}	Supply
RXI ±	2, 1	Receive Data Inputs	Differential Voltage In
PMID ±	25, 24	Physical Media Indicate Data	ECL Out
PMRD ±	15, 16	Physical Media Request Data	ECL In
TXO ±	9, 8	Transmit Data Outputs	Differential Current Out
SD ±	20, 21	Signal Detect Outputs	ECL Out
TXREF	6	Transmit Amplitude Reference	Current Out
ENCSEL	12	Encode Select Input	CMOS In
LBEN	19	Loopback Enable	CMOS In
EQSEL	17	Equalization Select	3-Level Select
$\overline{OE}$	18	Output Enable Bar	CMOS Schmitt Trig In

3.0 Pinout Information (Continued)

3.2 PIN DEFINITIONS

V_{CC} (13, 26): Positive power supply for the 100K ECL compatible circuitry. The Transceiver operates from a single +5 VDC power supply.

GND (14, 22): Return path for the 100K ECL compatible circuitry power supply.

RXV_{CC} (4, 27): Positive power supply for the small signal receive circuitry. This power supply is intentionally separated from others to eliminate receive errors due to coupled supply noise.

RXGND (3, 28): Return path for the receive power supply circuitry. This power supply return is intentionally separated from others to eliminate receive errors due to coupled supply noise.

TXV_{CC} (5, 11): Positive power supply required by the analog portion of the transmit circuitry. This power supply is intentionally separated from the others to prevent supply noise from coupling to the transmit outputs.

TXGND (7, 10): Return path for the analog transmit power supply circuitry. This supply return is intentionally separated from others to prevent supply noise from being coupled to the transmit outputs.

$EXTV_{CC}$ (23): Positive power supply for 100K ECL output circuitry.

RXI± (2, 1): Balanced differential line receiver inputs. These inputs are capable of receiving either binary or MLT-3 encoded data.

PMID± (25, 24): Differential 100K ECL compatible outputs which source the recovered receive-data to the appropriate clock recovery circuit.

PMRD± (15, 16): Differential 100K ECL compatible inputs which accept transmit-data from the appropriate Physical Layer device

TXO± (9, 8): Differential current driver outputs which drive either binary or MLT-3 encoded data over either 100Ω or 150Ω twisted pair cable. These outputs provide controlled rise and fall times designed to filter the transmitters output, reducing any associated EMI.

SD± (20, 21): Differential 100K ECL compatible Signal Detect outputs which indicate that either a valid signal is present at the RXI± inputs or that Loopback mode has been selected.

TXREF (6): Reference current pin allowing adjustment of TXO± transmit amplitude. By placing a resistor between this pin and TXGND, a reference current is setup which results in a given transmit amplitude for a given application. Refer to section 1.3 of the Functional Description for reference current equations.

ENCSEL (12): The TTL compatible CMOS Encode Select input controls the encoded state of the signal at the TXO± outputs. A logic high level at this input causes the TXO± pins to output binary code and configures the receiver to receive binary. A logic low level causes the TXO outputs to source MLT-3 encoded data and configures the receiver to accept MLT-3 encoded data.

LBEN (19): TTL compatible CMOS Loopback Enable input pin selects the internal loopback path which routes the PMRD± data to the PMID± differential outputs and forces Signal Detect true. During loopback operation (LBEN = 1) the TXO± outputs source a true QUITE onto the cable. Normal operation occurs when LBEN forced low.

EQSEL (17): This three level Equalization Select input controls the mode of receiver equalization. Forcing a median voltage level, accomplished by allowing EQSEL to float, selects the adaptive equalization mode which automatically regulates the equalization effects based on signal degradation caused by the media. Forcing a voltage less than ⅓ of V_{CC}, selects full equalization which provides fixed equalization for a maximum length of cable. Forcing a voltage greater than ⅔ of V_{CC} turns the receive equalizer off.

$\overline{OE}$ (18): The Schmitt Trigger Output Enable bar input is provided to support the option of true transmit disable. With $\overline{OE}$ high, the signal detect output is forced low (SD+ = 0) which inhibits data reception by the PHY and the PMID outputs are forced to 100K ECL static levels (PMID+ = 0, PMID− = 1). The exception is in the case of Loopback when the Signal Detect output is forced high (SD+ = 1) regardless of all other conditions. With $\overline{OE}$ low, the transceiver functions normally.

4.0 Functional Truth Tables

4.1 OUTPUT ENABLE

Output Enable

$\overline{OE}$	TXO Outputs	PMID+/PMID−	SD+/SD−
0	Normal Function	Normal Function	Normal Function
1	TRI-STATE	0/1	0/1

4.2 EQUALIZATION SELECT

Equalization Select

EQSEL	Mode
< 1.5V	Full EQ
Float	Adaptive EQ
> 3.0V	EQ Off

4.3 ENCODE SELECT

Encode Select

ENCSEL	Mode
0	MLT-3 (TP-FDDI/100BASE-TX)
1	Binary

4.4 LOOPBACK SELECT

Loopback Select

LBEN	TXO Outputs	PMID Outputs	SD+/SD−
0	Normal Function	Normal Function	Normal Function
1	True Quiet	follow PMRD	1/0

The Loopback Function is intended for board diagnostics. In Loopback mode, the ECL signal applied to the PMRD inputs will appear at the PMID outputs regardless of the signal present at the RXI inputs.

5.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Logic Power	Referenced to GND	−0.5		7.0	V
RXV_{CC}	Received Power	Referenced to RXGND	−0.5		7.0	V
TXV_{CC}	Transmit Power	Referenced to TXGND	−0.5		7.0	V
$EXTV_{CC}$	ECL Output Power	Referenced to GND	−0.5		7.0	V
I_{ECL}	DC Output Current (High)				−50	mA
ESD					2	KV
$T_{storage}$	Storage Temperature		−65		+150	°C

5.1 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.50	5.0	5.50	V
T_A	Operating Temperature		0	25	70	°C
PD	Device Power Dissipation			700		mW

5.2 DC ELECTRICAL CHARACTERISTICS $T_A = 25°C, V_{CC} = 5.0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IHt}	TTL High Level Input				10	μA
I_{ILt}	TTL Low Level Input				−10	μA
$I_{IHschmitt}$	Schmitt High Level Input				10	μA
$I_{ILschmitt}$	Schmitt Low Level Input				−10	μA
$I_{IHeqsel}$	EQSEL High Level Input	*Figure 24a*			1000	μA
$I_{ILeqsel}$	EQSEL Low Level Input	*Figure 24a*			−1000	μA
I_{IHe}	ECL High Level Input				50	μA
I_{ILe}	ECL Low Level Input				1.0	μA
V_{IHt}	TTL High Level Input		2.0			V
V_{ILt}	TTL Low Level Input				0.8	V
$V_{IHschmitt}$	Schmitt High Level Input			$3*V_{CC}/4$		V
$V_{ILschmitt}$	Schmitt Low Level Input			$V_{CC}/4$		V
$V_{IHeqsel}$	EQSEL High Level Input			$2*V_{CC}/3$		V
$V_{ILeqsel}$	EQSEL Low Level Input			$V_{CC}/3$		V
$V_{IMeqsel}$	EQSEL Mid Level Input			$V_{CC}/2$		V
V_{IHe}	ECL High Level Input		$V_{CC} - 1165$		$V_{CC} - 880$	mV
V_{ILe}	ECL Low Level Input		$V_{CC} - 1810$		$V_{CC} - 1475$	mV
V_{OHe}	ECL High Level Output	*Figure 24c*	$V_{CC} - 1025$		$V_{CC} - 880$	mV
V_{OLe}	ECL Low Level Output	*Figure 24c*	$V_{CC} - 1810$		$V_{CC} - 1620$	mV
I_{CCext}	External Supply Current	*Figure 24c*		55		mA
I_{CCint1}	Internal Supply Current	ENCSEL = 1, $\overline{OE}$ = 0, *Figure 24c*		115		mA
I_{CCint2}	Internal Supply Current	ENCSEL = 0, $\overline{OE}$ = 0, *Figure 24c*		135		mA
$I_{CCtotal1}$	Total Supply Current	ENCSEL = 1, $\overline{OE}$ = 0, *Figure 24c*		170		mA
$I_{CCtotal2}$	Total Supply Current	ENCSEL = 0, $\overline{OE}$ = 0, *Figure 24c*		190		mA

5.0 Electrical Characteristics (Continued)

5.2 DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$ (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{TXOmatch1}$	Transmit Current Matching 1	LBEN = 1, R_{REF} = 510Ω, (Note 1)		2.5		%
$I_{TXOmatch2}$	Translmit Current Matching 2	ENCSEL = 0, LBEN = 0, R_{REF} = 510Ω PMRD+ = 0, PMRD− = 1 (Note 1)		2.5		%
$I_{TXOleak\_tri}$	TXO TRI-STATE Leakage Current	$\overline{OE}$ = 1, R_{REF} = 510Ω, V_{TXO-} = 0V, V_{TXO+} = 0V (Note 2)			10	μA
TX_{ref_mult1}	TXREF Multiplier for Binary	ENCSEL = 1, R_{REF} = 510Ω, *Figure 24b*, (Note 3)		5.12		
TX_{ref_mult2}	TXREF Multiplier for MLT-3	ENCSEL = 0, R_{REF} = 510Ω, *Figure 24b* (Note 3)		10.24		
TX_{ref_tol}	TXREF Multiplier Tolerance	ENCSEL = 1, R_{REF} = 510Ω		2.5		%
SD_{THon1}	Sig Det Turn-on Threshold 1	ENCSEL = 1, *Figure 10* (Note 4)		750		mV
SD_{THon2}	Sig Det Turn-on Threshold 2	ENCSEL = 0, *Figure 10* (Note 4)		750		mV
SD_{THoff1}	Sig Det Turn-off Threshold 1	ENCSEL = 1, *Figure 10* (Note 4)		200		mV
SD_{THoff2}	Sig Det Turn-off Threshold 2	ENCSEL = 0, *Figure 10* (Note 4)		200		mV
R_{INdiff}	RXI Differential Input Resistance			8		KΩ

Note 1: $I_{TXOmatch}$ refers to the percentage of mismatch in current between TXO+ and TXO− referenced to the total output current as defined by:

$$I_{TXOmatch} = \frac{I_{TXO+} - I_{TXO-}}{I_{TXO+} + I_{TXO-}} \times 100$$

Note 2: V_{TXO+} and V_{TXO-} refer to the voltage present at the TXO+ and TXO− output pins respectively.

Note 3: Refer to Section 1.3 for further description of the TXREF Multiplier (scaling factor).

Note 4: Signal Detect turn on and turn off thresholds are measured differentially directly across the RXI± inputs.

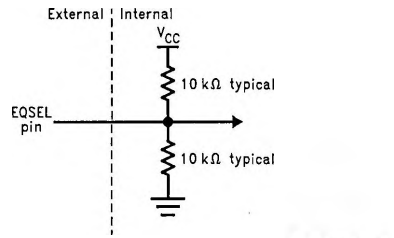

FIGURE 24a. EQSEL 3 Level Input

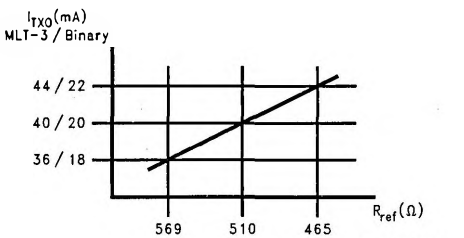

FIGURE 24b. Typical TXO Current vs R_{REF}

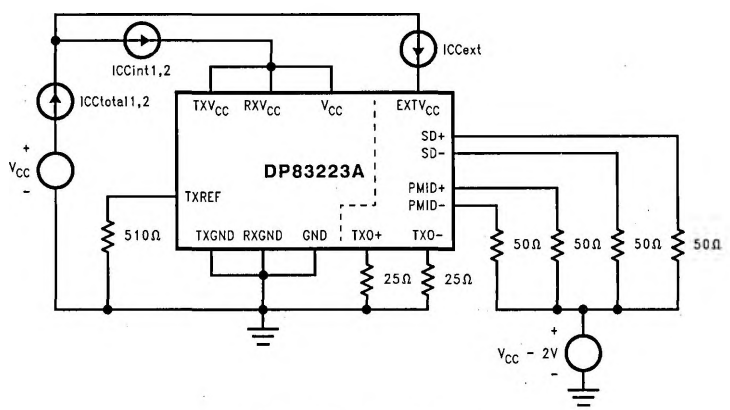

FIGURE 24c. I_{CC} Diagram

5.0 Electrical Characteristics (Continued)

5.3 AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{TXr/f\,1}$	TXO Rise/Fall (10%–90%)	ENCSEL = 1, *Figure 25*		2.2		ns
$t_{TXr/f\,2}$	TXO Rise/Fall (10%–90%)	ENCSEL = 0, *Figure 26*		2.2		ns
t_{TLH}	PMID Rise (20%–80%)	LBEN = 1, *Figure 27*		1.0		ns
t_{THL}	PMID Fall (20%–80%)	LBEN = 1, *Figure 27*		1.0		ns
t_{TXpd1}	PMRD/TXO Prop Delay	ENCSEL = 1, *Figure 25*		6.5		ns
t_{TXpd2}	PMRD/TXO Prop Delay	ENCSEL = 0, *Figure 26*		7.0		ns
t_{RXpd1}	RXI/PMID Prop Delay	ENCSEL = 1 (Note 1) *Figure 27*		4.5		ns
t_{RXpd2}	RXI/PMID Prop Delay	ENCSEL = 0 (Note 2) *Figure 28*		5.5		ns
t_{LBpd}	PMRD/PMID Prop Delay	LBEN = 1, *Figure 31*		2.0		ns
t_{LBon_pmid}	LBEN on to PMID	LBEN = 1, RXI Not Switching, *Figure 29*		20		ns
t_{LBoff_pmid}	LBEN off to PMID	LBEN = 0, RXI Not Switching, *Figure 29*		20		ns
t_{LBon_txo}	LBEN on to TXO Balance	LBEN = 1, *Figure 29*		50		ns
t_{LBoff_txo}	LBEN off to TXO Active	LBEN = 0, *Figure 29*		20		ns
t_{LBon_sd}	LBEN on to SD+ High	LBEN = 1, *Figure 29*		20		ns
t_{LBoff_sd}	LBEN off to SD+ Normal	LBEN = 0, *Figure 29*		20		ns
$t_{\overline{OE}on\_txo}$	$\overline{OE}$ on to TXO Active	*Figure 30*		40		ns
$t_{\overline{OE}off\_txo}$	$\overline{OE}$ off to TXO TRI-STATE	*Figure 30*		20		ns
$t_{SDon\,1}$	RXI Data to SD High	ENCSEL = 1 (Note 3) *Figure 32*		28		μs
$t_{SDon\,2}$	RXI Data to SD High	ENCSEL = 0 (Note 4) *Figure 33*		0.5		μs
$t_{SDoff\,1}$	RXI Quiet to SD Low	ENCSEL = 1 (Note 3) *Figure 32*		28		μs
$t_{SDoff\,2}$	RXI Quiet to SD Low	ENCSEL = 0 (Note 4) *Figure 33*		0.5		μs
t_{jTX1}	TX pk Total Jitter	ENCSEL = 1 (Note 5)		750		ps
t_{jTX2}	TX pk Total Jitter	ENCSEL = 0 (Note 5)		850		ps
t_{jRX1}	RX pk Total Jitter	ENCSEL = 1 (Note 6)		1400		ps
t_{jRX2}	RX pk Total Jitter	ENCSEL = 0 (Note 6)		1500		ps
Mbps	MLT-3 Data Rate	ENCSEL = 0		125		Mbps

Note 1: $t_{RXpd\ 1}$ RXI to PMID timing is measured by applying a 1 Vp-p 62.5 MHz square wave to the RXI ± inputs with EQSEL floating.

Note 2: $t_{RXpd\ 2}$ RXI to PMID timing is measured by applying a 1.5 Vp-p 62.5 MHz MLT-3 IDLE to the RXI ± input with EQSEL floating.

Note 3: Signal Detect turn on and turn off times are measured using an MTL-3 2 Vp-p scrambled halt bit stream over a length of Category 5 UTP cable ≤ 100 Meters with adaptive equalization enabled.

Note 4: Signal Detect turn on and turn off times are measured using a binary 1 Vp-p 2^{23} pseudo random bit stream over a length of Category 5 UTP cable ≤ 100 Meters with adaptive equalization enabled.

Note 5: TX Jitter measurements are made differentially at the TXO ± current outputs using a scrambled HALT bit stream for MLT-3 mode and PRBS 2^{23} for binary mode. All measurements are referenced to the original transmit clock.

Note 6: RX Jitter measurements are made differentially at the PMID ± PECL outputs using a scrambled HALT bit stream for MLT-3 mode and PRBS 2^{23} for binary mode. This test includes data transmission over a 100M Cat-5 cable plant comprised of 90M of horizontal wiring, two 5M lengths of vertical wiring, two 110 punchdown blocks and 2 RJ45-8 wall jacks. All measurements are referenced to the original transmit clock.

5.0 Electrical Characteristics (Continued)

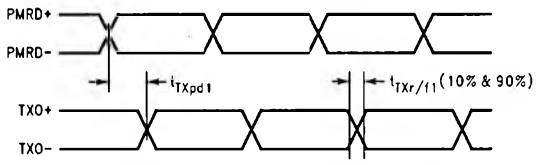

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FIGURE 25. TXO Timing (binary)

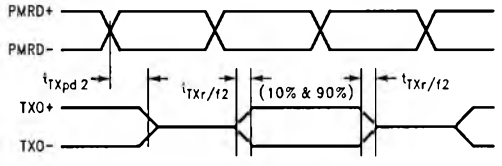

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FIGURE 26. TXO Timing (MLT-3)

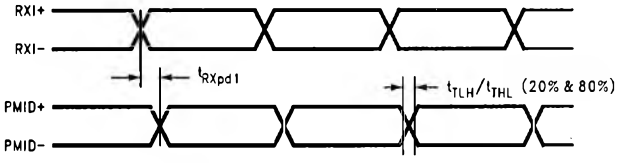

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FIGURE 27. PMID Timing (Binary RXI to PMID)

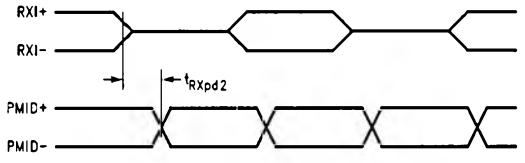

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FIGURE 28. PMID Timing (MLT-3 RXI to PMID)

5.0 Electrical Characteristics (Continued)

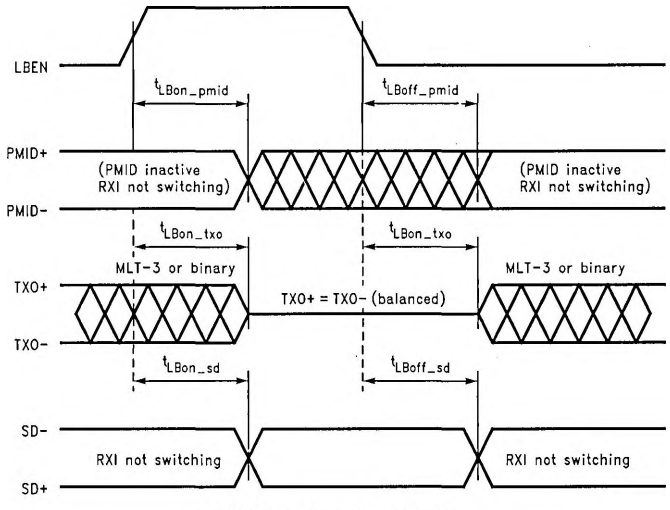

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FIGURE 29. Loopback Timing

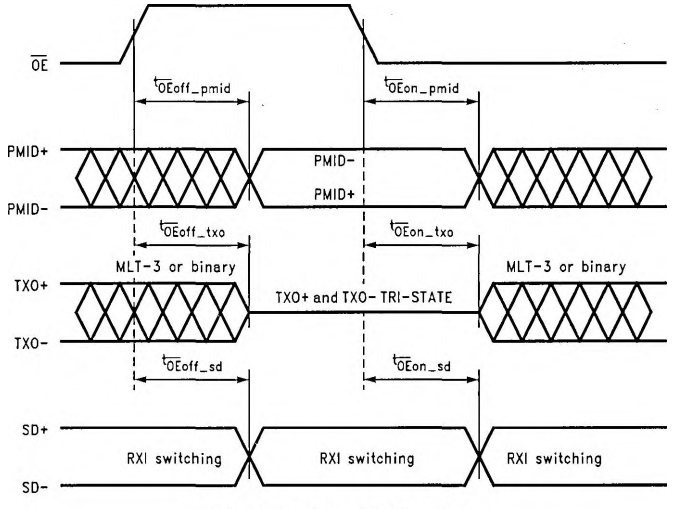

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FIGURE 30. Output Enable Timing

5.0 Electrical Characteristics (Continued)

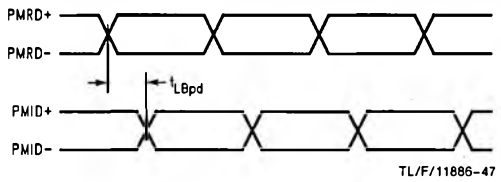


FIGURE 31. PMID Timing (Loopback)

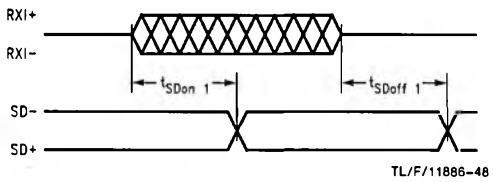


FIGURE 32. Signal Detect Timing (Binary RXI to SD)

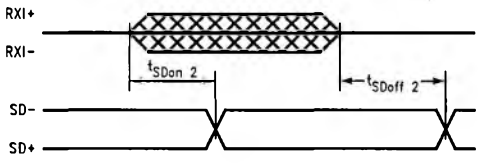
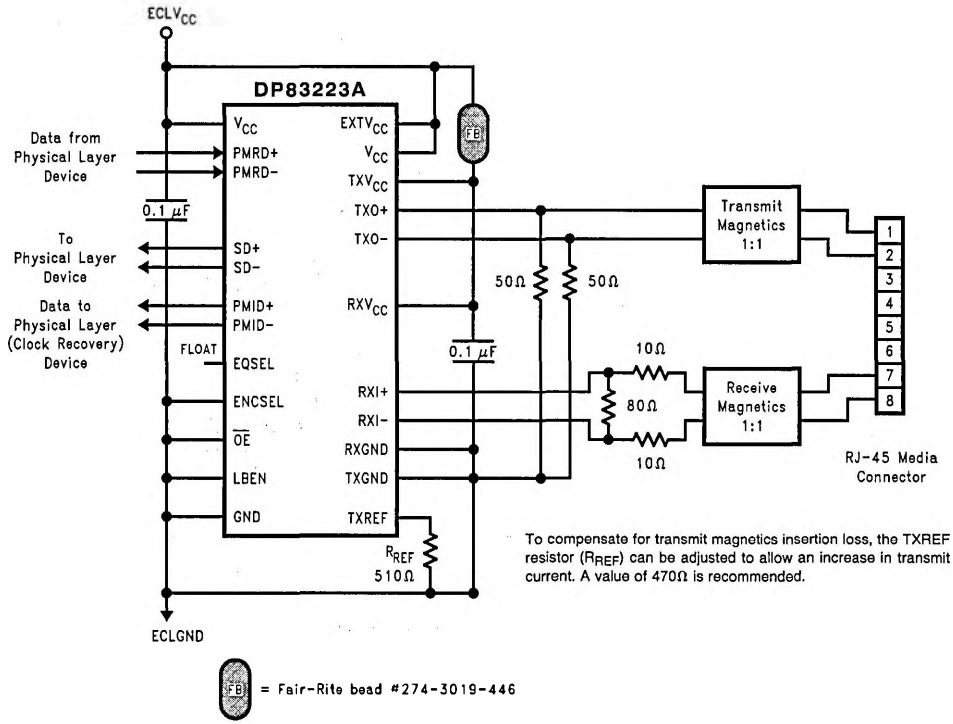


FIGURE 33. Signal Detect Timing (MLT-3 RXI to SD)



To compensate for transmit magnetics insertion loss, the TXREF resistor (R_{REF}) can be adjusted to allow an increase in transmit current. A value of 470Ω is recommended.

The PMRD, SD and PMID 100K ECL differential signal must be terminated into a standard ECL load of 50Ω to V_{CC} minus 2.0V or equivalent: i.e., Thevenin of 130Ω to GND accompanied by 82Ω to V_{CC}.

FIGURE 34. Typical Schematic for MTL-3 Signalling over Cat-5 UTP 100Ω Cable