National Semiconductor

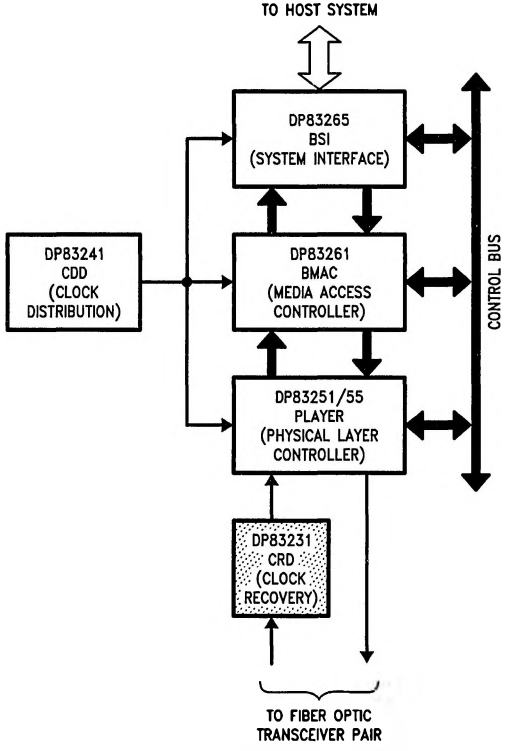
DP83231 CRD™ Device (FDDI Clock Recovery Device)

General Description

The DP83231 CRD device is a clock recovery device that has been designed for use in 100 Mbps FDDI (Fiber Distributed Data Interface) networks. The device receives serial data from a Fiber Optic Receiver in differential ECL NRZI 4B/5B group code format and outputs resynchronized NRZI received data and a 125 MHz received clock in differential ECL format for use by the DP83251/55 PLAYER™ device.

Features

- Clock recovery at 100 Mbps data rate
- Internal 250 MHz VCO
  - 0.1% VCO operating range
  - Crystal controlled
- Precision window centering delay line
- Single +5V supply
- 28-pin PLCC package
- BiCMOS processing



TL/F/10384–1

FIGURE 1-1. FDDI Chip Set Block Diagram

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1.0 FDDI Chip Set Overview

National Semiconductor's FDDI chip set consists of five components as shown in *Figure 1-1.* For more information about the other devices in the chip set, consult the appropriate data sheets and application notes.

DP83231 CRD™ Device Clock Recovery Device

The Clock Recovery Device extracts a 125 MHz clock from the incoming bit stream.

Features

- PHY Layer loopback test
- Crystal controlled
- Clock locks in less than 85 μs

DP83241 CDD™ Device Clock Distribution Device

From a 12.5 MHz reference, the Clock Distribution Device synthesizes the 125 MHz, 25 MHz and 12.5 MHz clocks required by the BSI, BMAC, and PLAYER devices.

DP83251/55 PLAYER™ Device Physical Layer Controller

The PLAYER device implements the Physical Layer (PHY) protocol as defined by the ANSI FDDI PHY X3T9.5 Standard.

Features

- 4B/5B encoders and decoders
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Link error detector
- Configuration switch
- Full duplex operation
- Separate management port that is used to configure and control operation.

In addition, the DP83255 contains an additional PHY_Data.request and PHY_Data.indicate port required for concentrators and dual attach stations.

DP83261 BMAC™ Device Media Access Controller

The BMAC device implements the Timed Token Media Access Control protocol defined by the ANSI FDDI X3T9.5 MAC Standard.

Features

- All of the standard defined ring service options
- Full duplex operation with through parity
- Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long, and External Addressing
- Generates Beacon, Claim, and Void frames internally
- Extensive ring and station statistics gathering
- Extensions for MAC level bridging
- Separate management port that is used to configure and control operation
- Multi-frame streaming interface

DP83265 BSI™ Device System Interface

The BSI Device implements an interface between the National FDDI BMAC device and a host system.

Features

- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Interfaces to low-cost DRAMs or directly to system bus
- Provides 2 Output and 3 Input Channels
- Supports Header/Info splitting
- Efficient data structures
- Programmable Big or Little Endian alignment
- Full Duplex data path allows transmission to self
- Comfirmation status batching services
- Receive frame filtering services
- Operates from 12.5 MHz to 25 MHz synchronously with host system

2.0 Functional Description

The DP83231 uses two phase locked loops (PLL's) to perform the clock recovery function. The function of the first PLL is to establish a 250 MHz Voltage Controlled Oscillator (VCO) with a narrow frequency range which can be pulled by the second PLL. The function of the second PLL is to force this same VCO to track the incoming data so that a Receive Clock output and a data synchronizing flip-flop can be driven from it. Operation of the VCO at 250 MHz ensures that the received clock output operating at half of the VCO frequency has a 50% duty cycle waveform independent of any VCO waveform dissymmetry.

The first PLL uses a 10.41666 MHz crystal as a pullable frequency reference to generate the 250 MHz VCO. The limited frequency pulling range of the crystal ensures that the capture range of the 250 MHz VCO is limited to less than 0.1% of the specified data transition rate, thus eliminating the possibility of fractional or harmonic lock up modes. The output of the VCO is divided by twenty four and applied to the feedback input of the phase detector in the first PLL. The phase detector compares the phase of the VCO divided by twenty four signal against the phase of the crystal to maintain VCO lock at 250 MHz. If the phase transition of the signal derived from the VCO arrives at the phase detector before that of the crystal, the charge pump circuitry will apply a negative current pulse to the VCO FLTR node who's width is proportional to the phase error. The charge pulled out of the filter capacitors will drive the voltage applied to the VCO downward. This reduction in the VCO's control voltage will slow down the frequency of the VCO and will appear during successive cycles to reduce the VCO's phase and frequency error. As the frequency of the crystal varies, in response to the second PLL, the frequency of the 250 MHz VCO will change in an attempt to remain 24 times the crystal's frequency.

The second PLL delays the phase transitions of the selected incoming stream of data (DATA± or LBD±), and then compares them against the phase transitions of a gated 125 MHz signal derived from the 250 MHz VCO. The delayed incoming data is applied to the reference input of a phase detector and the gated VCO signal is applied to it's feedback input. If the positive and negative phase transitions of the incoming data do not line up with the phase transitions of the gate VCO signal, the charge pump circuitry associated with that phase detector will apply current pulses to the OSC FLTR± nodes which are proportional to the phase error. The change in the charge on the filter capacitors will modify the reverse bias on the varactors in the crystal's tank circuit thus causing the frequency of the 10.41666 MHz crystal (and consequently the VCO) to shift in the direction which will reduce their phase error. When the phase of the VCO and the incoming data are aligned, a VCO divided by two signal can be used as the Receive Clock output. Because the two PLL's share a common VCO feedback path, the cutoff frequency of the loop filters associated with the second PLL are specified to be approximately 10 times lower than the cutoff frequency of the first PLL to prevent instability between the two loops.

The delay line associated with the second PLL precisely centers the data transitions within the data window. The delay line remains accurate independent of temperature, power supply, IC process variation or external components. The design also ensures that the charge pump up and down circuits both produce an active pulse at each zero phase crossing when in lock to guarantee a linear phase detector gain characteristic.

The CRD continually monitors the data frequency at the selected data inputs. If this input frequency drops below ½ the minimum allowed frequency (about 3 MHz) the CRD resets itself by internally deasserting CRD-EN. This centers the crystal frequency, and restarts the internal VCO.

The CRD EN pin is provided to initialize the CLK DET circuitry and enable the crystal to track incoming data. The part is enabled when this pin is active High. Deassertion of this pin will cause the CLK DET circuitry and the OSC FLTR ± pins to be disabled in a manner similar to when legitimate data is not being received. Deassertion of the CRD EN pin also momentarily causes (1 μs) the VCO FLTR pin to be pulled to ground and stops the VCO and RXC ± outputs. After this time, the VCO will be restarted and its output frequency will climb quickly to approximately 250 MHz.

The device is capable of locking on to a stream of Halt or Master line states in less than 100 μs when using a 10.41666 MHz crystal to govern the 250 MHz VCO. Lock on time for a stream of Idle line states is less than 10 μs once Halt or Master line status is obtained. During quiet line conditions the chip will output a continual stream of Received Clock whose frequency will be within less than 0.1% of the upstream station's data rate. The Received Data outputs are always active. Prior to the CLK DET output transitioning active High, the Received Data outputs may issue invalid data (see Typical Waveforms). When the device is locked, Received Data is presented on the falling edge of the Receive Clock output insuring sufficient setup and hold margin for the receiving device.

An ECL to TTL translator is provided on the chip to convert the FORX's ECL signal detect output level to TTL for use by the PLAYER device.

2.0 Functional Description (Continued)

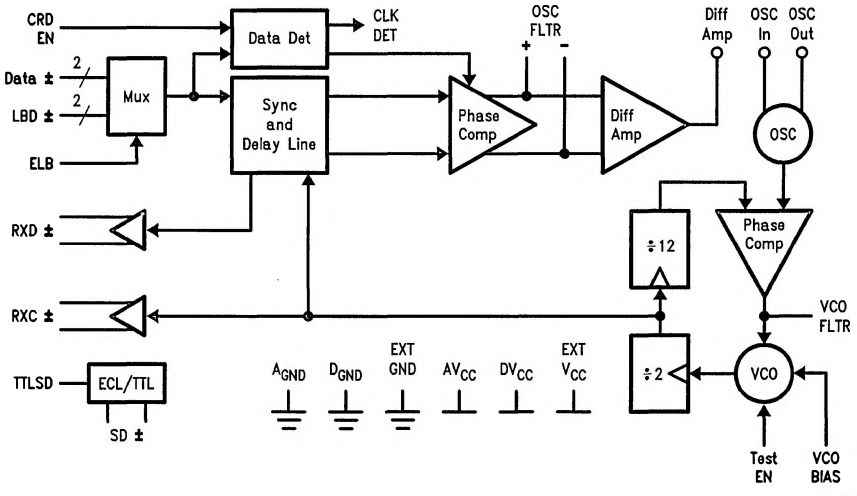
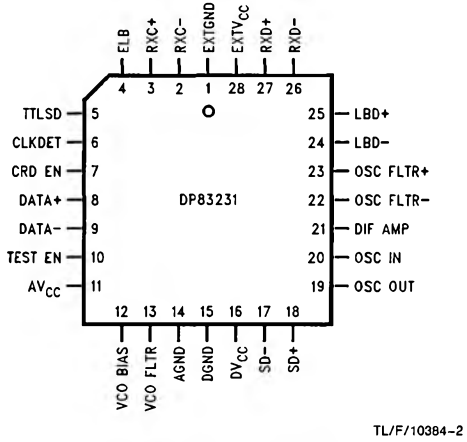


FIGURE 2-1. DP83231 Block Diagram

28-Pin PLCC Package



Order Number DP83231AV
See NS Package Number V28A

FIGURE 2-2. DP83231 Pinout

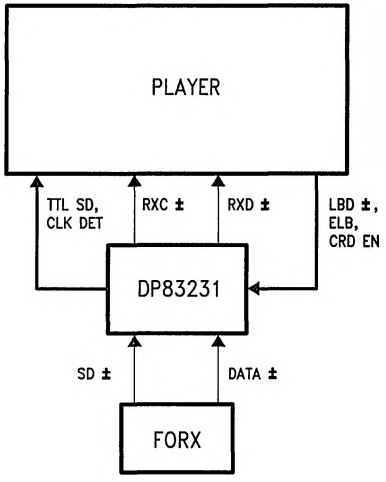


FIGURE 2-3. System Connection Diagram

3.0 Pin Descriptions

Symbol	Pin No.	I/O	Description
DATA+, DATA−	8, 9	I	**DATA ±:** 4B/5B serial NRZI data inputs originating from a fiber optic receiver and presented for the purpose of resynchronization and clock recovery. These differential 100k ECL compatible inputs are selected when the ELB input is at a logic Low level.
LBD+, LBD−	25, 24	I	**Loopback Data ±:** 4B/5B serial NRZI data inputs originating from a local PLAYER device and presented for the purpose of station diagnostics. These differential 100k ECL compatible inputs are selected when the ELB input is at a logic High level.
ELB	4	I	**Enable Loopback:** TTL compatible input which selects between the DATA ± inputs or the LBD ± inputs. The LBD inputs are selected when the ELB pin is at a logic High level and the DATA inputs when at a logic Low level.
CLK DET	6	O	**Clock Detect:** CMOS output used to indicate that the chip has detected the presence of a continuous data frequency greater than 3.0 MHz. A logic High level on the output will indicate that valid input data has been detected.
CRD EN	7	I	**CRD Enable:** TTL compatible input which directs the differential charge pump outputs to either operate the crystal oscillator at the center of its operating range or to track out the VCO phase errors in the second PLL. The CRD EN input will reset the CLK DET function and will force the oscillator to the center of its operating range when at a logic LOW level and will allow normal PLL tracking operation when at a logic High level. Deassertion of the CRD EN input will momentarily stop the VCO.
OSC FLTR+, OSC FLTR−	23, 22	O	**Oscillator Filter ±:** The differential charge pump up and down outputs which are part of the second PLL. A three element filter should be connected to each of these pins which consists of one capacitor in parallel with a resistor and another capacitor to ground. These outputs are driven to their maximum upper operating level when the CRD EN pin is at a logic LOW level or when valid data frequencies are not recognized at the data inputs.
DIF AMP OUT	21	O	**Differential Amplifier Output:** The differential amplifier output associated with the second PLL which is used to adjust the frequency of the external crystal.
OSC_IN, OSC_OUT	20, 19	I	**Oscillator Input and Output:** The terminals for the crystal oscillator which require connection of the crystal tank circuit, varactors, and capacitors.
RXC+, RXC−	3, 2	O	**Receive Clock:** Differential 100K ECL receive clock outputs which operate at 125 MHz synchronized to the selected inputs (NRZI DATA ± or LBD ±) when valid line state data is present. When valid line state data is not present these outputs continue to operate at a nominal frequency of 125 MHz ± 12 kHz. These outputs should be terminated externally with a conventional ECL 50Ω equivalent load.
RXD+, RXD−	27, 26	O	**Receive Data:** Differential 100K ECL received data outputs which provide a resynchronized equivalent of the selected NRZI DATA or LBD inputs. The received data output transitions occur concurrent with the falling edge of the RXC ± output. These outputs should be terminated externally with a conventional ECL 50Ω equivalent load.
VCO FLTR	13	O	**VCO Filter:** Low pass filter associated with the first PLL. A three element filter should be connected to this pin which consists of one capacitor in parallel with a resistor and another capacitor to ground.
SD+, SD−	18, 17	I	**Signal Detect:** Differential inputs to a 100K ECL to TTL translator intended for conversion of the fiber optic receiver's ECL signal detect to TTL for a player device. The inputs are used in the test modes as inputs for single stepping and gating the VCO.
TTLSD	5	O	**TTL Signal Detect:** Intended to be a signal detect output in TTL format for use by the PLAYER chip.
TEST EN	10	I	**Test Enable:** CMOS input which enables the test functions. This input must be at a logic low level in normal operation.
DV_{CC}	16		**Digital V_{CC}:** Positive power supply for most of the internal logic circuitry intended for +5V operation ±5% relative to ground. Bypass capacitors should be placed as close as possible across the DV_{CC} and DGND pins. DV_{CC}, AV_{CC} and $EXTV_{CC}$ should be tied together through chokes.

3.0 Pin Descriptions (Continued)

Symbol	Pin No.	I/O	Description
$EXTV_{CC}$	28		**External V_{CC}:** Positive power supply for all the input and output buffers intended for +5V operation ±10% relative to ground. Bypass capacitors should be placed as close as possible across the $EXTV_{CC}$ and EXTGND pins. DV_{CC}, AV_{CC} and $EXTV_{CC}$ should be tied together at the device pins through chokes.
DGND	15		**Digital Ground:** Power supply return for the internal circuitry. DGND, AGND and EXT GND pins should be tied together.
EXTGND	1		**External Ground:** Power supply return for the input and output buffers. DGND, AGND and EXT GND pins should be tied together.
AV_{CC}	11		**Analog V_{CC}:** Positive power supply for the critical analog circuitry intended for +5V operation ±5% relative to ground. Bypass capacitors should be placed as close as possible across the AV_{CC} and A_{GND} pins. DV_{CC}, $EXTV_{CC}$ and AV_{CC} should be tied together through chokes.
AGND	14		**Analog Ground:** Power supply return for the critical analog circuitry. DGND, EXTGND and AGND pins should be tied together.
VCO BIAS	12	I	**VCO Bias:** TTL compatible input that sets the nominal frequency for the VCO by the selection of the resistor value between this input and AV_{CC}. A 30 kΩ value for this resistor will provide nominally 125 MHz on the RXC outputs.

4.0 Electrical Characteristics

4.1 ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature −65°C to +150°C

TTL Signals
- Inputs 5.5V
- Outputs 5.5V

ECL Signals
- Output Current −20 mA

Supplies
- $EXTV_{CC}$ to EXTGND −0.5V to +7V
- DV_{CC} to DGND −0.5V to +7V
- AV_{CC} to AGND −0.5V to +7V

ESD Susceptibility 2000V

4.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Units
V_{CC} to GND	Power Supply		4.75	5	5.25	V
V_{IH}	High Level Input Voltage	TTL	2.0			V
		ECL	V_{CC} − 1.165		V_{CC} − 0.880	
V_{IL}	Low Level Input Voltage	TTL			0.8	V
		ECL	V_{CC} − 1.810		V_{CC} − 1.475	
I_{OH}	High Level Output Current	TTL Outputs (Note 1)			−0.4	mA
I_{OL}	Low Level Output Current	TTL Outputs (Note 1)			4.0	mA
FVCO	VCO Frequency			250		MHz
FXTL	Crystal Frequency			10.416667		MHz
TA	Operating Temperature		0	25	70	°C

Note 1: TTL outputs include CLK DET and TTLSD.
ECL outputs include RXC± and RXD±.

4.0 Electrical Characteristics (Continued)

4.3 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
V_{IC}	Input Clamp Voltage	I_{IN} = 18 mA		−1.5	V
V_{OH}	High Level Output Voltage	TTL Outputs: I_{OH} = −400 μA	V_{CC} − 2		V
		ECL Outputs: 50Ω Load to V_{CC} − 2V	V_{CC} − 1025	V_{CC} − 880	mV
V_{OL}	Low Level Output Voltage	TTL Outputs: I_{OL} = 4 mA		0.5	V
		ECL Outputs: 50Ω Load to V_{CC} − 2V	V_{CC} − 1810	V_{CC} − 1620	mV
I_I	Max High Level Input Current	TTL Inputs: V_{IN} = 7V		100	μA
I_{IH}	High Level Input Current	TTL Inputs: V_{IN} = 2.7V	−20	20	μA
I_{IL}	Low Level Input Current	TTL Inputs: V_{IN} = 0.4V	−20	20	μA
I_{filter}	Charge Pump Current	Source	−0.3	−0.7	mA
		Sink	0.3	0.7	mA
		TRI-STATE®	−500	500	nA
I_{CC}	Supply Current			180*	mA

*Includes 60 mA due to external ECL termination of two differential signals.

For 100k ECL output buffers, output levels are specified as:

$V_{OH\_max} = V_{CC} - 0.88V$

$V_{OL\_max} = V_{CC} - 1.62V$

Since the outputs are differential, the average output level is V_{CC} − 1.25V. The test load per output is 50Ω at V_{CC} − 2V. The external load current through this 50Ω resistor is thus:

$I\_load = [(V_{CC} - 1.25) - (V_{CC} - 2)]/50A$

$= 0.015A$

$= 15$ mA

There are 2 pairs of differential ECL signals, so the total ECL current is 60 mA.

4.4 AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
T1	Phase Difference		−2	2	ns
T2	RXC Pos. Pulse Width	(Note 1)	3	5	ns
T3	CLK DET Time	CRD EN Neg. Pulse Width = 1 μs (Valid DATA ± Present)		100	μs
T4	Valid Data Time	CRD EN = High		100	μs

Note 1: These parameters are not tested, but are assured by correlation with characterization data.

4.0 Electrical Characteristics (Continued)

TYPICAL WAVEFORMS

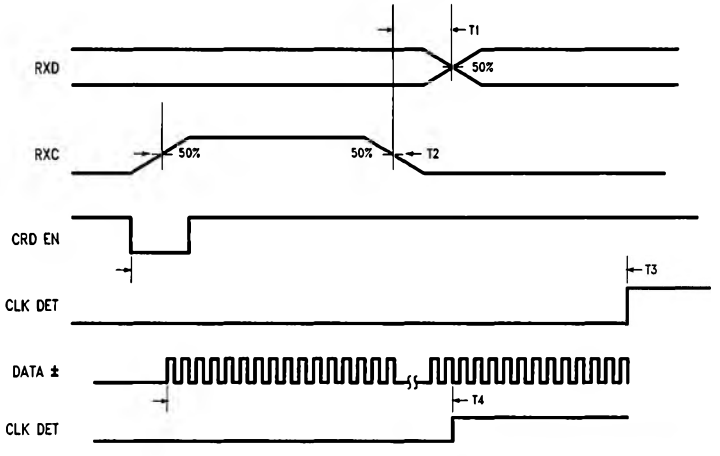


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FIGURE 4-1. DP83231 Timing Waveforms

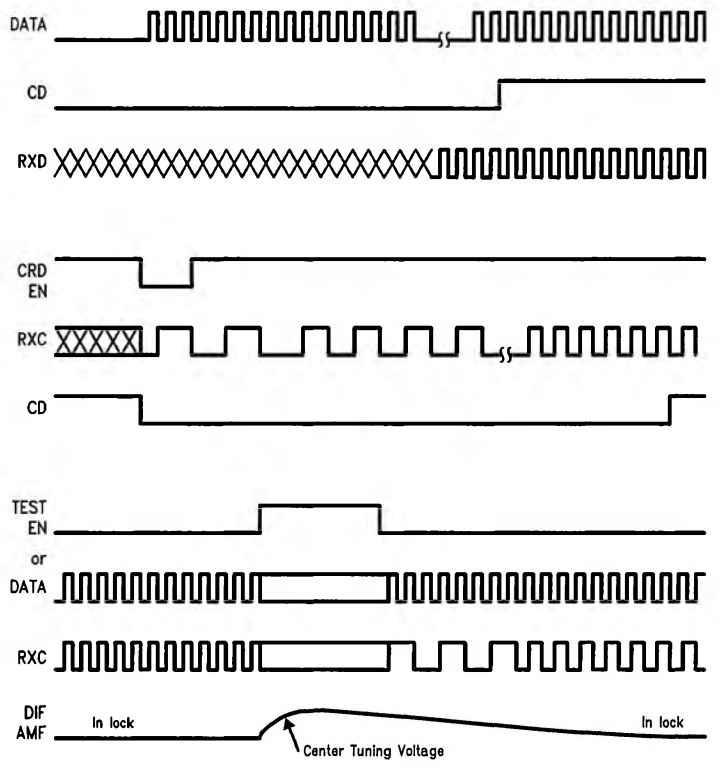

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FIGURE 4-2. Typical Waveforms

4.0 Electrical Characteristics (Continued)

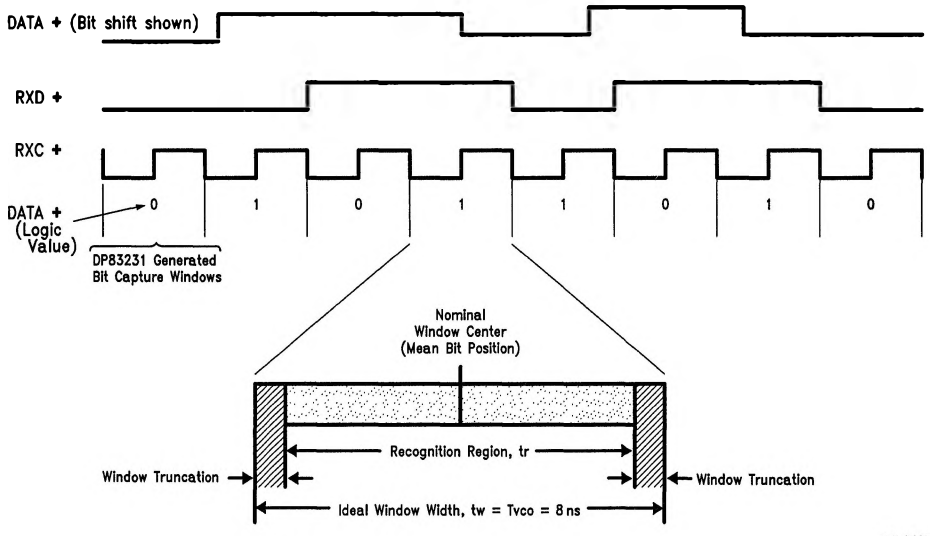

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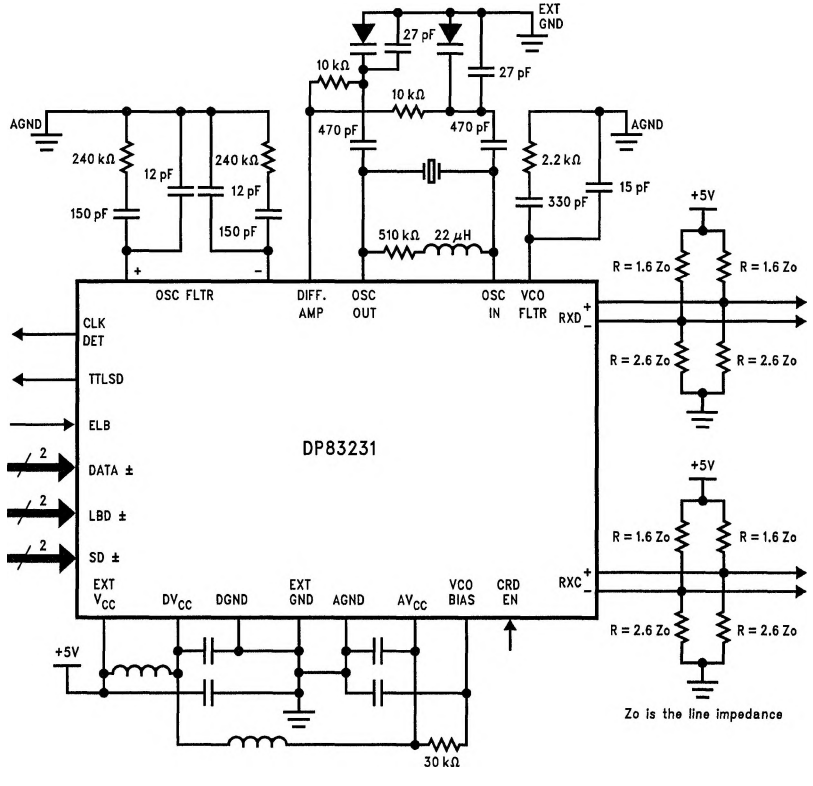
FIGURE 4-3. Synchronization Window



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All component values ±5%.

FIGURE 4-4. General Wiring Diagram

5.0 Detailed Information

5.1 SPECIAL EXTERNAL COMPONENTS

Crystals

- Manufacturer: Nel Frequency Controls (414) 763-3591
  Part#: C5400N
- Manufacturer: Standard Crystal Corporation
  (818) 443-2121
  Part#: 800R-A-10.41667-32

Key Specifications:

Center Frequency: 10.41667 MHz
Load Capacitance, C_L: 32 pF
Frequency Calibration: ±20 PPM
Frequency Stability (0°C–70°C): ±20 PPM
Aging: < ±10 PPM
Pullability: either a motional capacitance of ≥0.021

or

a change of at least 100 PPM when the C_L is changed from 32 pF to 18 pF and a change of −100 PPM when the C_L is changed from 32 pF to 50 pF.

Varactors

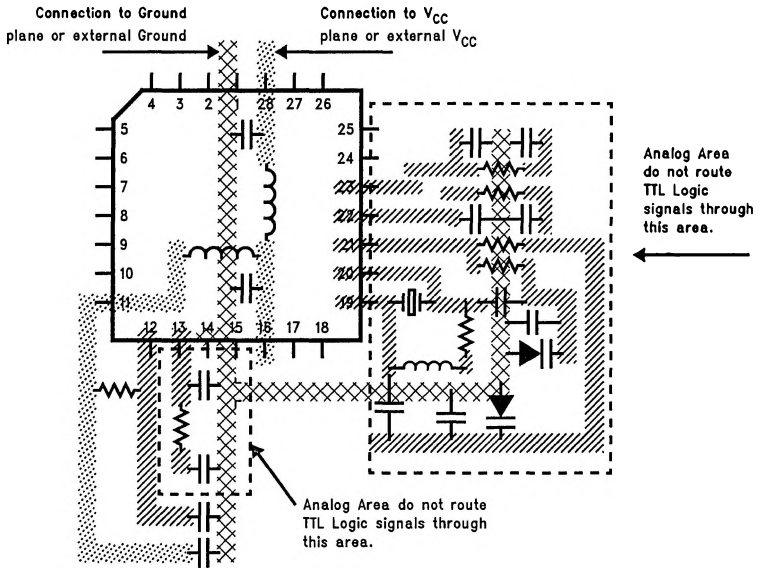
- Manufacturer: Alpha Industries (617) 935-5150
  Part#: DKV6510-71

Key Specifications:

Capacitance: @ V_r = 1V: C > 85 pF
@ V_r = 4V: 15 pF < C < 30 pF

5.2 LAYOUT RECOMMENDATIONS

- The part should be bypassed between the $EXTV_{CC}$ and EXTGND as close to the chip as possible (preferably under the chip using chip caps). The part should also be bypassed between the DV_{CC} and DGND and the AV_{CC} and AGND as close to the chip as possible.
- No TTL logic lines should pass through the crystal OSC FLTRs or VCO FLTR circuitry areas to avoid the possibility of noise due to crosstalk.
- The crystal, OSC FLTRs and the VCO FLTR circuitries should be connected to Ground on isolated branches off of the DGND pin. If using a multilayered board with dedicated V_{CC} and Ground planes ensure that for the ground plane that the ceramic resonator, OSC FLTRs and the VCO FLTR circuitries have their own small isolated islands that are connected to the DGND and AGND pins as described above.
- The DV_{CC} and AV_{CC} pins should be connected to V_{CC} on an isolated branches off of the $EXTV_{CC}$ pin, preferably being connected through a ferrite bead or a small inductor.
- The DGND and AGND pins should be connected to GND on an isolated branches off of the EXTGND pin. Connection to the ground plane should be made only at the EXTGND pin.



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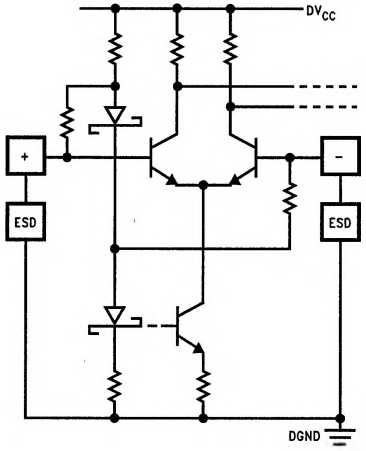
This drawing was done with convenience in mind.

FIGURE 5-1. Recommended Layout

5.0 Detailed Information (Continued)

5.3 INPUT AND OUTPUT SCHEMATICS

SD ±



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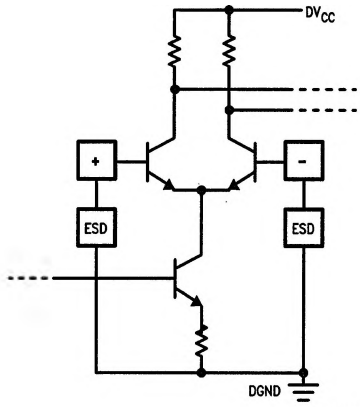
DATA ±, LBD ±



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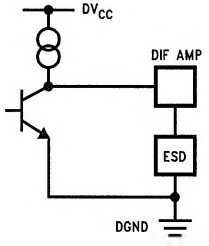
DIF AMP



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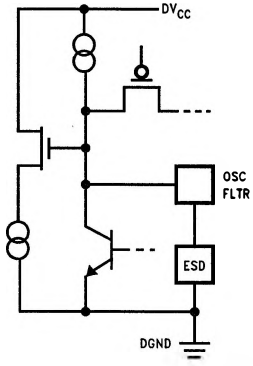
OSC FLTR



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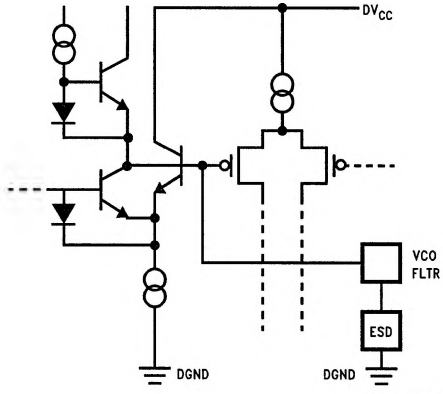
VCO FLTR



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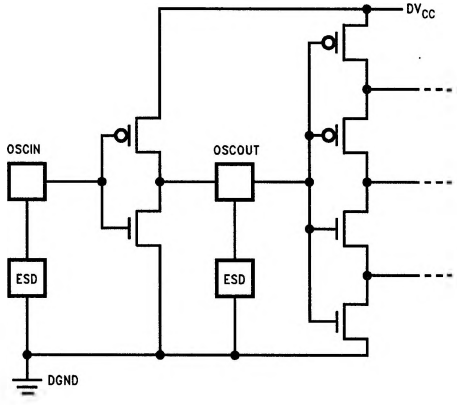
OSCIN, OSCOUT



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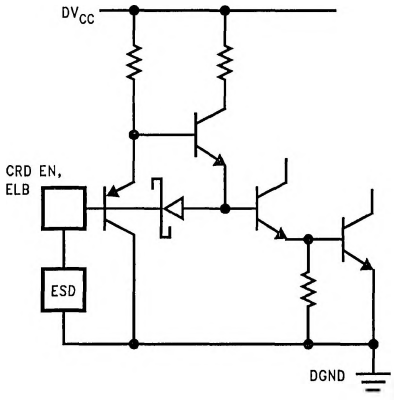
5.0 Detailed Information (Continued)

5.3 INPUT AND OUTPUT SCHEMATICS (Continued)

CRD EN, ELB



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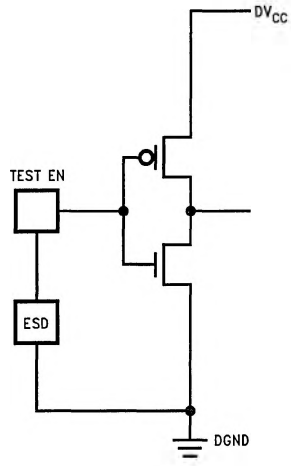
TEST EN



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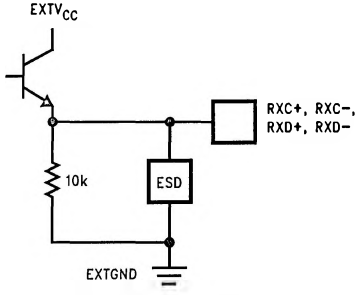
RXC±, RXD±



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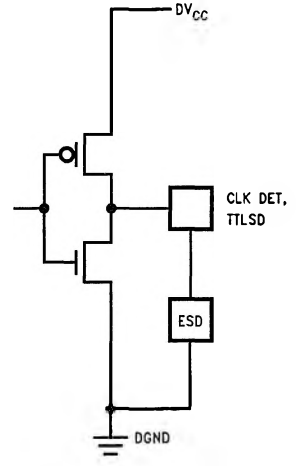
CLK DET, TTLSD



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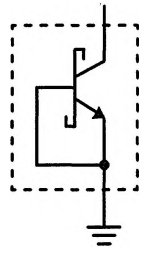
Typical ESD Structure



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5.0 Detailed Information (Continued)

5.4 DEBUG PROCEDURE

Evaluation of the DP83231 should begin by tying the CRD EN and TEST EN pins low and confirming that the SD± pins are above 2V. This will disable the differential phase comparator allowing the crystal resonator to run at its center frequency and will keep the part out of a test mode. The first PLL (see *Figure 5-2*) should be evaluated. The variable capacitor in the crystal resonator circuitry should be tuned so that the crystal resonator oscillates at 10.41666 MHz. If the oscillator circuit fails to oscillate the voltage levels of the OSC IN and OSC OUT pins should be examined. The DC voltage on these pins should be equal to approximately $V_{CC} \div 2$ (with or without the crystal present). The capacitors which form the oscillator tank circuit should be returned to the isolated ground branch in close proximity. After checking the crystal frequency, examine the RXC± output and verify that this frequency is twelve times the crystal frequency. If this is not true then the VCO FLTR output should be examined for possible PC board shorts, opens or filter instability. The VCO FLTR pin should be stable at approximately a 1.5V DC level in operation.

If the VCO FLTR pin is oscillating then the loop filter components for this pin were either chosen inappropriately or were placed in the incorrect position.

Once it is known that the first PLL is working, force CRD EN high and input a constant 62.5 MHz ±50 ppm (1T pattern) data stream to the DATA± inputs (see *Figure 5-3*). To see how well the second loop is working examine the DIF AMP pin. If the incoming data rate is exactly 62.5 MHz and the crystal resonator was accurately adjusted as described above, then the DIF AMP pin voltage should be stable at approximately 2.25V. The voltage at this pin will vary from the nominal value dependent on temperature and data rate frequency error. If this pin is oscillating then the OSC FLTR pins are unstable and the filters should be examined for possible PC board shorts, opens or instability. If the DIF AMP pin is near ground then check to see if the ELB input is selecting the correct data input. If the DIF AMP pin continues to be near ground or V_{CC}, then the accuracy of the 62.5 MHz source should be examined to verify it is within the ±3 KHz (50 PPM) FDDI system data rate specification.

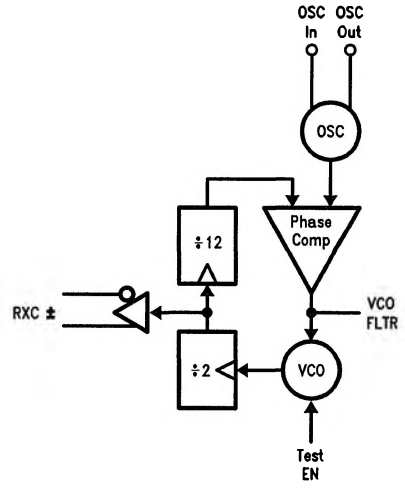

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FIGURE 5-2. 1st PLL

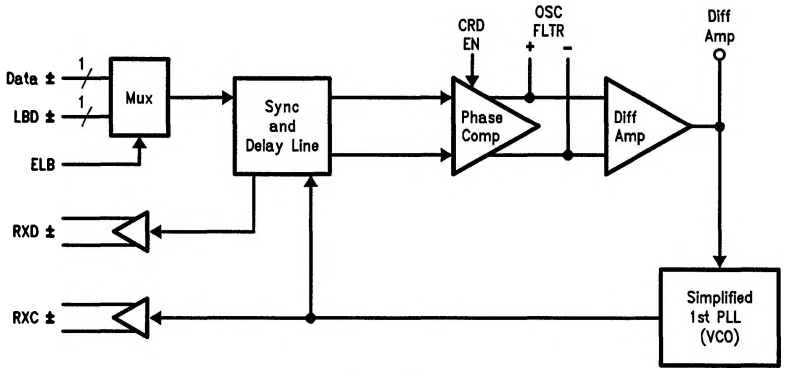

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FIGURE 5-3. 2nd PLL

5.0 Detailed Information (Continued)

5.5 AC TEST CIRCUITS

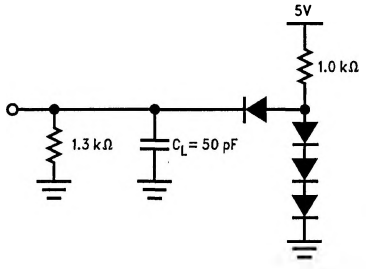

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FIGURE 5-4. Switching Test Circuit for All TTL Output Signals

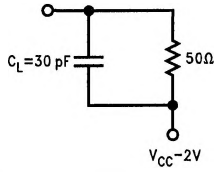

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FIGURE 5-5. Switching Test Circuit for All ECL Input and Output Signals