National Semiconductor

PRELIMINARY

DP83856
100 Mb/s Repeater Information Base

General Description

The DP83856 100 Mb/s Repeater Information Base is designed specifically to meet the management demands of today's high speed Ethernet networking systems.

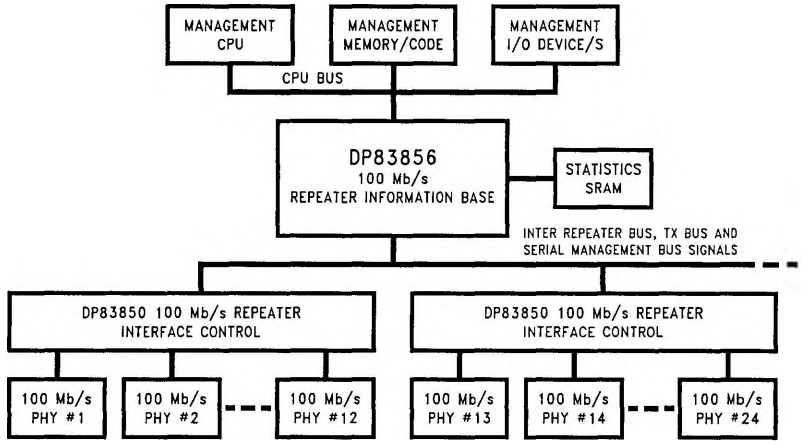
The DP83856 simplifies design of managed multiport repeaters. Used in conjunction with up to 16 DP83850s it enables a repeater system to become a single managed entity that is fully compatible with the IEEE 802.3u clause 30 management requirements.

The DP83856 device incorporates all the necessary functions and counters for collecting network statistics. Information is gathered on a per-packet, per-port basis: the port which is receiving the packet is the active port for statistics collection.

Features

- Supports up to 16 DP83850 Repeater Interface Controllers (192, 100 Mb/s ports on one segment)
- Fully IEEE 802.3u clause 30 compatible
- Network management statistics processed on a per activity (per packet) basis
- Programmed I/O interface for statistics reporting
- Uses external SRAM to maintain per port network management statistics counters
- Single interrupt acknowledgement provides report on all per port SRAM based and DP83856 based statistics
- Parallel register interface to CPU (16-bit)
- Allows indirect access to the DP83850 Repeater Interface Controller and DP83840 Physical Layer Device serial registers through a parallel register interface
- 132-pin PQFP

System Diagram



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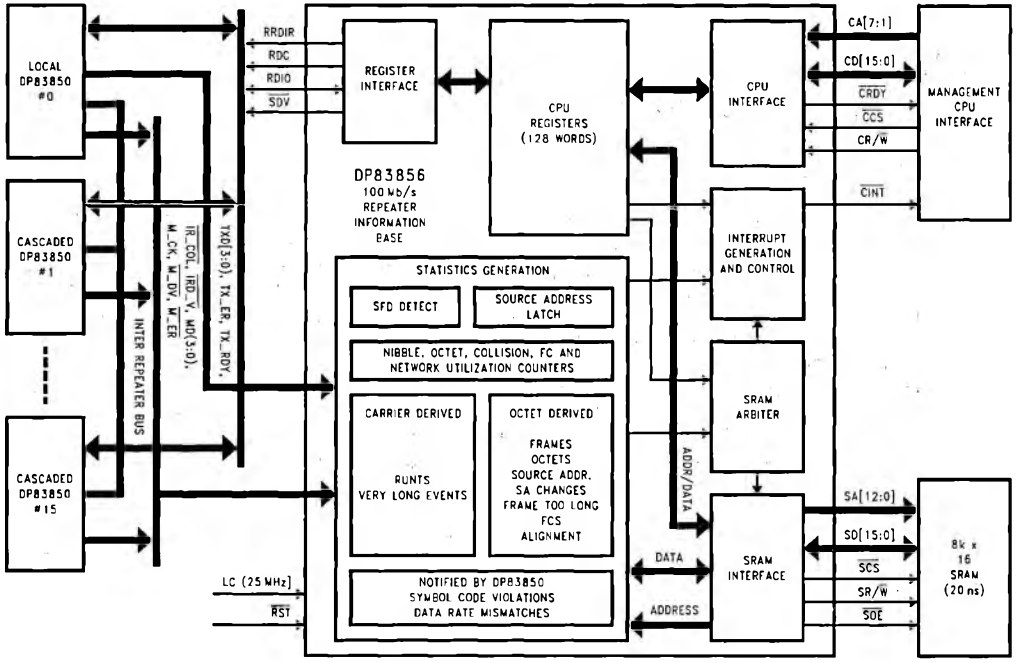
Block Diagram



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1.0 Pin Connection Diagram

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2.0 Pin Description

2.1 CPU INTERFACE

The CPU interface pins are a set of generic interface signals designed to accommodate many different CPU types with minimal external logic. The data interface is 16-bits wide and does not provide any steering capabilities. Furthermore, all accesses must be aligned on 16-bit boundaries, as indicated in the CPU Register Map Section 4.

Signal Name	Type	Active	Description
$\overline{\text{CINT}}$	O/Z, L	Low	**CPU INTERRUPT:** Indicates that the DP83856 has at least one interrupt pending. The $\overline{\text{CINT}}$ signal will remain active until the CPU reads the Interrupt Register. It is software's responsibility to keep track of multiple interrupts pending, and service all of the interrupts.
$\overline{\text{CRDY}}$	O/Z, L	Low	**CPU READY:** Indicates that the DP83856 is ready to terminate the current cycle. The DP83856 asserts $\overline{\text{CRDY}}$ on writes once it has strobed the data into its write data holding register. The DP83856 asserts $\overline{\text{CRDY}}$ on reads once it has strobed data into its read data output register.
$\overline{\text{CCS}}$	I	Low	**CPU CHIP SELECT:** Chip select for internal DP83856 registers. Generated by external logic as an address decode of the DP83856 register space. $\overline{\text{CCS}}$ must remain valid for the entire cycle.
CR/$\overline{\text{W}}$	I		**CPU READ-WRITE:** Read/Write strobe for DP83856 internal registers. Read = 1, Write = 0.
CA[7:1]	I		**CPU ADDRESS [7:1]:** Address bus for DP83856 register accesses. The DP83856 latches the address for internal use within 45 ns of $\overline{\text{CCS}}$ being asserted.
CD[15:0]	I/O/Z, M		**CPU DATA [15:0]:** 16-bit data bus for DP83856 register accesses. CD[15:0] correspond to the low 16-bits of data on the CPU. The DP83856 implements **Big Endian** convention for data storage. All CPU register accesses should be 16-bit accesses aligned on 16-bit boundaries.

2.2 SRAM INTERFACE

The SRAM interface pins are used to connect the DP83856 to a fast (20 ns) external SRAM. The DP83856 supports up to an 8k x 16-bit SRAM configuration. This configuration provides a maximum of 16, 32-bit statistics values per port.

Signal Name	Type	Active	Description
SA[12:0]	O/Z, L		**SRAM ADDRESS [12:0]:** The SRAM address bus should be directly connected to the fast external SRAM's address inputs.
SD[15:0]	I/O/Z/P, L		**SRAM DATA [15:0]:** The SRAM data bus, should be directly connected to the fast external SRAM's data pins.
SR/$\overline{\text{W}}$	O/Z, L		**SRAM READ-WRITE:** Should be directly connected to the fast external SRAM's write enable pin. Read = 1, Write = 0.
$\overline{\text{SCS}}$	O/Z, L	Low	**SRAM CHIP SELECT:** Should be directly connected to the fast external SRAM's active low chip select pin.
$\overline{\text{SOE}}$	O/Z, L	Low	**SRAM OUTPUT ENABLE:** Should be directly connected to the fast external SRAM's (active low) output enable pin.

2.0 Pin Description (Continued)

2.3 TRANSMIT BUS AND MANAGEMENT BUS

Signal Name	Type	Active	Description
TXD[3:0]	I		**TRANSMIT DATA [3:0]:** Transfers data from a local DP83850 to the DP83856. TXD[3:0] is synchronous to the local clock signal LC, and is framed by the transmit ready signal TX__RDY.
TX__RDY	I	High	**TRANSMIT DATA READY:** Asserted by a local DP83850 when non-idle symbols are repeated on any of the DP83850's output ports. The DP83856 uses this signal as a framing signal for transmit data, transmit error, management data, management error, collision, data valid, and as an enable for carrier and network utilization timing.
TX__ER	I	High	**TRANSMIT DATA ERROR:** Asserted by a local DP83850 when a transmit error occurs. The DP83856 monitors this signal to determine if the current reception was a Symbol Code violation error. TX__ER is synchronous to the local clock signal LC.
$\overline{\text{IR\_\_COL}}$	I	Low	**INTER REPEATER COLLISION:** Asserted by any (all) DP83850s in the system which are currently experiencing a collision. The DP83856 monitors this signal during TX__RDY valid, and uses the information in statistics processing and collision counting.
$\overline{\text{IRD\_\_V}}$	I	Low	**INTER REPEATER DATA VALID:** Asserted by any DP83850 in the system which has won the Inter Repeater Bus arbitration and is transmitting valid data symbols. The DP83856 monitors this line at the beginning of the frame to establish whether the frame is a false carrier event. If TX__RDY is valid and $\overline{\text{IR\_\_DV}}$ is invalid when the DP83856 samples the $\overline{\text{IR\_\_DV}}$ line, then a false carrier event is counted.
MD[3:0]	I		**MANAGEMENT DATA [3:0]:** Data which is sourced by any DP83850 in the system that has won the Inter Repeater Bus arbitration. This data is synchronous to the management clock M__CK, and is framed by the transmit ready signal TX__RDY. The DP83856 uses this data to determine the source of the current data stream (DP83850 RID number and Port number).
$\overline{\text{M\_\_DV}}$	I	Low	**MANAGEMENT DATA VALID:** Asserted by any DP83850 in the system which has won the Inter Repeater Bus arbitration when it places valid data on MD[3:0]. The DP83856 monitors this line when TX__RDY is valid to determine when to latch the DP83850 RID number and port number for the current reception. $\overline{\text{M\_\_DV}}$ is synchronous to M__CK.
M__CK	I		**MANAGEMENT CLOCK:** All data transfers on the management bus are synchronized to the rising edge of this clock. M__CK is a reference 25 MHz clock used to latch the active DP83850, port, and elasticity buffer errors for the current packet reception. M__CK is sourced by any DP83850 in the system which has won the Inter Repeater Bus arbitration.
$\overline{\text{M\_\_ER}}$	I	Low	**MANAGEMENT ERROR:** Asserted by any DP83850 in the system which has won the Inter Repeater Bus arbitration when a data rate mismatch error occurs (elasticity buffer over/underrun). The DP83856 monitors this line during TX__RDY valid to determine if the current frame contains a data rate management error. $\overline{\text{M\_\_ER}}$ is synchronous to M__CK. Note that on data rate mismatch errors, $\overline{\text{M\_\_ER}}$ will not be asserted until after the DP83850 number and port number have been sent to the DP83856 from the DP83850, but will be sent prior to the end of the frame (before TX__RDY is de-asserted).

2.4 MII INTERFACE

Signal Name	Type	Active	Description
RDC	O/Z, L		**REGISTER DATA CLOCK:** A 2.5 MHz clock which is continuously output from the DP83856. Used to synchronize data transfers on the serial MII register bus.
RDIO	I/O/Z, L		**REGISTER DATA I/O:** Serial MII register data signal. Used to transfer data to and from the DP83856 on MII register accesses. This signal should be buffered onto the backplane, using the RRDIR signal as a direction control for the buffer. The buffer does not require a tri-state enable.
RRDIR	O/Z, L	High	**RIB REGISTER DIRECTION:** Serial MII Register Direction pin to drive an external buffer. The buffer should default to READ, and toggle to WRITE only when the DP83856 is initiating an MII register access. 0 = MII Slave (DP83850 or PHY) drives RDIO 1 = DP83856 drives RDIO
$\overline{\text{SDV}}$	O/Z, L	Low	**SERIAL DATA VALID:** Indicates that a valid MII access is in progress. It is asserted one half clock prior to the start of the cycle and remains valid for one half clock after the cycle is complete.

2.0 Pin Description (Continued)

2.5 TEST INTERFACE

Signal Name	Type	Active	Description
$\overline{\text{TSTATE}}$	I/P	Low	**TRI-STATE®:** Pulling this pin low puts the DP83856 into a test mode that tri-states all outputs except $\overline{\text{NAND\_E}}$ and $\overline{\text{NAND\_O}}$.This allows an external tester to drive all the outputs of the DP83856.
$\overline{\text{TEST\_EN}}$	I/P	Low	**TEST MODE ENABLE HIGH/LOW OUTPUT TEST:** Forces the DP83856's outputs to the High or Low state as defined by the $\overline{\text{TEST\_H\_L}}$ pin. This allows automatic test machines to check for outputs stuck at High or Low.
$\overline{\text{TEST\_H\_L}}$	I/P	Low	**TEST MODE OUTPUT HIGH/LOW:** When $\overline{\text{TEST\_EN}}$ is taken Low, the DP83856's output pins (in two groups) are forced into the High or Low state as defined below: $\overline{\text{TEST\_H\_L}}$ Group 1 Outputs Group 2 Outputs 0 1 0 1 0 1 Group 1 output pin numbers are: 21, 23, 27, 31, 35, 37, 39, 43, 61, 64, 68, 70, 72, 74, 78, 80, 82, 87, 89, 90, 92, 96, 98, 100, 104, 108, 113, 115. Group 2 output pin numbers are: 20, 22, 24, 30, 34, 36, 38, 42, 44, 65, 69, 71, 73, 75, 79, 81, 83, 88, 91, 93, 97, 99, 103, 105, 114, 116.
$\overline{\text{NAND\_E}}$	O, L	Low	**NAND TREE EVEN INPUTS OUTPUT:** The logical NAND of all of the even numbered inputs (except the test input $\overline{\text{TEST\_EN}}$) and $\overline{\text{RST}}$. If all of the inputs are High, the output will go Low. If any of the inputs are Low, the output will remain High.
$\overline{\text{NAND\_O}}$	O, L	Low	**NAND TREE ODD INPUTS OUTPUT:** The logical NAND of all of the odd numbered inputs (except the test inputs $\overline{\text{TSTATE}}$, $\overline{\text{TEST\_H\_L}}$ and LC). If all of the inputs are High, the output will go Low. If any of the inputs are Low, the output will remain High.

2.6 MISCELLANEOUS PINS

Signal Name	Type	Active	Description
LC	I		**LOCAL CLOCK:** Primary clock for DP83856 device. All DP83856 internal state machines run off LC. This clock must be the same local clock used to drive the local DP83850 because the TX signals (to which the DP83856 must be sychronized) are all synchronous to the local clock. Must be a 25.000 MHz, 40/60 duty cycle, 50 ppm.
$\overline{\text{RST}}$	I	Low	**RESET:** The DP83856 is reset when this signal is asserted low. Asserting this signal will cause all DP83856 state machines and registers to enter their reset state. The statistics SRAM is not cleared by $\overline{\text{RST}}$, it must be cleared/preset by software.
RES1	O		**RESERVED OUTPUT 1:** No Connect.
RES2	O		**RESERVED OUTPUT 2:** No Connect.

2.7 PIN TYPE DESIGNATION

Type	Description
I	Input buffer.
I/P	Input buffer with internal pull-up resistor.
O, L	Output buffer, low drive (4 mA).
O/Z, L	Output buffer with high impedance capability, low drive (4 mA).
I/O/Z, L	Bi-directional buffer with high impedance capability, low drive (4 mA).
I/O/Z, M	Bi-directional buffer with high impedance capability, medium drive (12 mA).
I/O/Z/P, L	Bi-directional buffer with high impedance capability and pull-up resistor, low drive (4 mA).

3.0 Functional Description

The following sections describe the different functional blocks of the DP83856 100 Mb/s Repeater Information Base. Referring to the block diagram on page 2 of this datasheet, the DP83856 is used in conjuction with a number of DP83850s, a management CPU and a fast (20 ns) 8k x 16 bit SRAM. The DP83856 collects and maintains network management statistics from the connected DP83850s and makes them available to the management CPU.

3.1 STATISTICS GENERATION

Inputs to the DP83856 Statistic Generation block include the Inter Repeater Bus signals, Management Bus signals and TX bus signals. These signals provide the data streams necessary to create all the statistics collected by the DP83856. The DP83856 uses the fast external SRAM to hold statistics for the current packet reception. Statistics for the current receive packet are collected as follows:

3.1.1 Octet Derived

The majority of the statistics are a function of the octet count. Statistics based on octet counts imply that a valid SFD has been detected and an accurate count of the number of data bytes in the packet are available.

The DP83856 Statistic Generation module has an SFD detect block, which indicates that a valid SFD has been detected so that the octet counter can be enabled. The Source Address latch is used to store the source address of the current packet, so that a comparison to the previous source address can be made at the end of the packet reception. Octet derived statistics include:

Frames
Octets
FCS Errors
Alignment Errors
Frames Too Long
Source Address
Source Address Changes

3.1.2 Carrier Derived

Other statistics are a function of carrier. Carrier derived statistics have a high probability of occurring on activity bursts which do not include a valid SFD. To ensure accurate statistic gathering a carrier based detection scheme is implemented. A nibble counter is used to calculate the length of the carrier, which is used to create the carrier derived statistics.

The DP83856 employs 32-bit counters for network utilization, false carrier events, and collisions. All of these counters monitor events for all ports, i.e. they are an aggregate of the total repeater events.

Carrier derived statistics gathered by the DP83856 include:

Runts
Very Long Events (jabber)
Network Utilization
Repeater False Carrier Events
Repeater Collisions (per port collision map obtained from DP83850s)

3.1.3 DP83850 Notified

For a few of the required statistics the DP83856 has no way of determining the occurrence of that event. These statistics are obtained by notification from the connected DP83850s. DP83850 notified statistics include:

Data Rate Mismatches
Symbol Code Violations

3.1.4 Collision Counter

The DP83856 has a 32-bit counter which is incremented any time the repeater experiences a collision. This counter is used to keep track of total number of collisions happening on the repeater.

3.1.5 Network Utilization Counter

The Network Utilization counter is a 32-bit counter that counts nibbles when TX_RDY is active. The network utilization counter will count all nibbles relative to any packet activity. This includes any short events, runts, and even noise on the segment. The network utilization counter is used to measure the packet activity relative to the overall network bandwidth. Since the nibbles occurs at a 25 MHz rate, during a one second update there could be up to a maximum of 25 million nibbles that could be recorded.

As an example, software can do a one second read update on the 32-bit network utilization counter, and read a 10 million value count. The network utilization can be calculated as 10 mil./25 mil. (max. total) = 0.4 or 40 per cent of the network bandwidth is utilized on that segment.

3.1.6 False Carrier Counter

The DP83856 has a 32-bit counter which is incremented any time the repeater experiences a false carrier event. This counter is used to keep track of the total number of false carrier events occurring on the segment.

3.2 SRAM INTERFACE

The SRAM interface provides the logic required to communicate with the fast external SRAM.

The interface between the DP83856 and the fast external SRAM is very straightforward. The fast external SRAM is a dedicated block of memory directly accessed only by the DP83856. The DP83856 provides the address capability for 8k x 16 bits of SRAM. In this configuration the DP83856 can store up to sixteen 32-bit statistics per port.

Figure 1 shows a memory map for the 8k x 16 configuration. For each port there are 11 statistics defined which are stored in SRAM. Ten of these statistics are 32-bit values, and one is a 48-bit value (Last Source Address).

Last Source Address is stored as two 32-bit values for simplicity of hardware implementation. All statistics are stored in big endian mode.

The DP83856 can be directly connected to the SRAM; there is no need for buffering between the DP83856 and the SRAM. The DP83856 requires fast SRAM with a maximum access time of 20 ns.

The SRAM interface block contains the address and data multiplexers to select between CPU and Statistic Update accesses. Data is multiplexed under control of the SRAM arbiter.

3.3 SRAM ARBITER

The SRAM arbiter controls the SRAM data multiplexers depending on what type of access is being performed and creates all of the control signals for the SRAM, ensuring the timing is correct. There are three events that result in SRAM arbitration:

— End of packet request_Runt (Statistic Update State Machine)
— End of packet request_Legal Length or greater (Statistic Update State Machine)
— CPU request (read or write)

3.0 Functional Description (Continued)

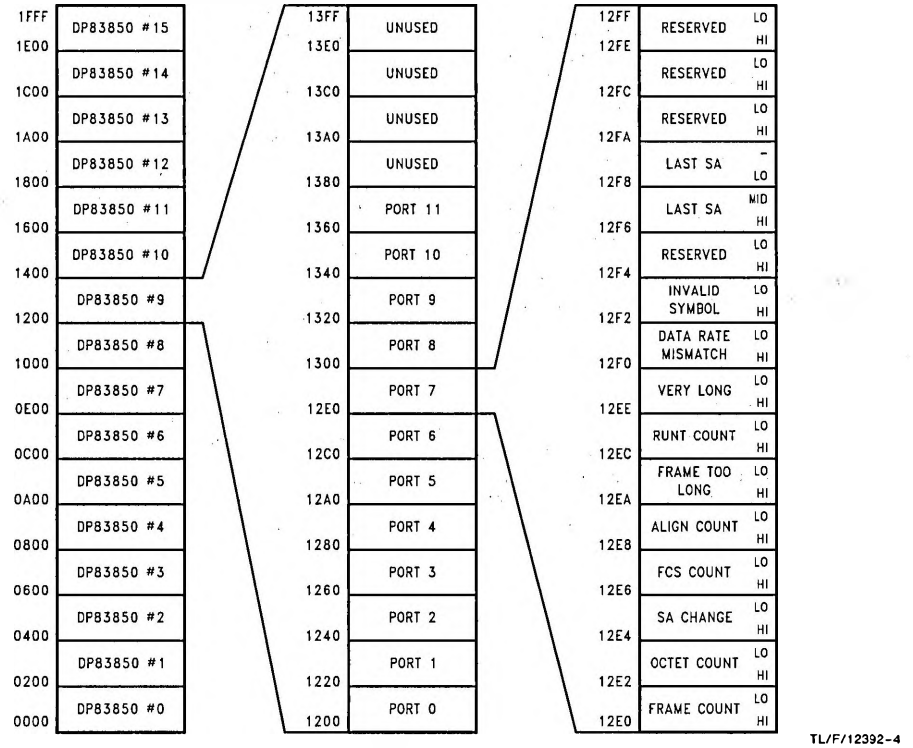

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FIGURE 1. Memory Map for the DP83856 Statistics SRAM

The arbiter assigns highest priority to EOP-runts and lowest priority to CPU requests. For single statistic reads, the arbiter produces two 16-bit locked read cycles on the SRAM to form the 32-bit value. For block reads the SRAM arbiter re-arbitrates after each 32-bit SRAM read (two 16-bit locked reads) to allow any higher priority event access to the SRAM. Writes to the SRAM must always be word (16-bit) accesses: byte writes are not supported.

3.4 INTERRUPT GENERATION AND CONTROL

There are four events that can generate an interrupt:

— SRAM access complete

— MII register access complete

— Invalid MII register read

— DP83856 error

The DP83856 provides one interrupt line ($\overline{\text{CINT}}$) that is shared for all interrupts. The interrupt is an active low, level sensitive signal. Interrupts are generated based on a valid event occuring with the appropriate mask bit set and global interrupt bit set. Interrupts are cleared by reading the interrupt register.

The "SRAM access complete" interrupt signifies that the current SRAM request has been serviced and the data is in the SRAM Read Data Register(s) (10h–40h).

The "MII register access complete" interrupt signifies that the current MII register request has been serviced and the data is in the MII Read Data Register(s) (A0h–ACh).

The "Invalid MII register read" interrupt is generated based on the DP83856 detecting an error while performing an MII read access. Per the MII register protocol in IEEE 802.3u/D5, Clause 22, the DP83856 looks for a leading 0 on reads; if it does not see a leading 0, it flags the read as invalid and generates the interrupt.

The "DP83856 error" interrupt signifies that the device has dropped management data due to invalid inter-frame gap (IFG) spacing between packets. The minimum IFG specified in the IEEE 802.3u/D5, Clause 21A.3 is 0.96 μs. The DP83856 may drop management data if the IFG drops below 0.64 μs. This event is not expected to happen on well formed 100 Mb/s networks.

3.5 MII REGISTER INTERFACE

The MII register interface block is a state machine that performs accesses to DP83850 and Physical Layer Device registers (read and write) based on requests from the CPU.

This interface uses the IEEE 802.3u clause 22 MII compliant serial interface protocol.

The MII Register Interface eliminates the need for the CPU to talk directly to the DP83850 and Physical Layer Device registers. The amount of spare management CPU processing bandwidth is therefore increased.

3.0 Functional Description (Continued)

The CPU provides the opcode, type of access (read or write), register address, and device ID to the MII Interface Register, and then asserts a start command by writing a 1 to bit 0 (MII_ACC) of the Configuration Register.

MII protocol for performing reads and writes are as follows:

READ

<01> <10> <AAAAA> <RRRRR> <line turn-around> <0> <xxxx xxxx xxxx xxxx>

where <01> is a start bit sequence, <10> is a read opcode, <AAAAA> is the device address (up to 32 devices), <RRRRR> is the register address (up to 32 registers), <line turn-around> is a clock cycle allowed for turn-around of the data bus, <0> is a leading 0, and <xx ... xx> is 16 bits of data.

WRITE

<01> <01> <AAAAA> <RRRRR> <10> <xxxx xxxx xxxx xxxx>

where <01> is a start bit sequence, <01> is a write opcode, <AAAAA> is the device address (up to 32 devices), <RRRRR> is the register address (up to 32 registers), <10> is a leading 10, and <xx ... xx> is 16 bits of data.

Refer to the IEEE 802.3u D5 draft document for more details on the MII interface, its function and timing.

3.6 CPU REGISTER BLOCK

The CPU register block provides the system management CPU access to all of the data in the DP83856, SRAM, connected DP83850s and Physical Layer Devices.

3.7 MANAGEMENT DATA INTERFACE

For every network event, the DP83850 device with port N will send information required by the DP83856 to perform statistics gathering.

The information required by the DP83856 is transferred on the Management Data Interface, which consists of a nibble wide data bus with synchronous clock (MD[3:0] and M_CK), plus a framing signal ($\overline{\text{M\_DV}}$) and an error flag ($\overline{\text{M\_ER}}$).

Data is transferred in 3 nibbles (per network event). The first data nibble contains the lowest significant 4 bits of the DP83850 RID Number, the second contains the most significant bit of the DP83850 RID number and the third contains the number of the receiving port (port N). The $\overline{\text{M\_ER}}$ signal indicates elasticity buffer errors (due to under-run or over-run) in the DP83850.

4.0 Registers

All the DP83856 registers are directly addressable by the system management CPU. Although some bits in the Configuration Register have been allocated to a register paging scheme, these are not currently used (available for future expansion) and should always be set to zero.

All register accesses are word (16-bit) wide: byte access is not supported. The addresses given in the tables below assume that the user has connected the DP83856 to a management CPU in the normal 16-bit manner with address bits A1–A7 from the CPU connected to bits CA1–CA7 on the DP83856. The addresses are thus the offset from the base address at which the DP83856 is located in the system.

To be consistent with normal address bus labeling practice, since the DP83956 only supports 16-bit accesses, no pin A0 is supplied.

4.1 REGISTER MEMORY MAP

Address	Register	Access
00h	Configuration Register	R/W
02h	Interrupt	R/W
04h	Reserved	
06h	SRAM Interface	R/W
08h	MII Management Interface	R/W
0Ah	SRAM Write Data	R/W
0Ch	MII Write Data	R/W
0Eh	Device ID	R only
10h	Frame Count High Read	R/W
12h	Frame Count Low Read	R/W
14h	Octet Count High Read	R/W
16h	Octet Count Low Read	R/W
18h	Source Address Change Count High Read	R/W
1Ah	Source Address Change Count Low Read	R/W
1Ch	FCS Error Count High Read	R/W
1Eh	FCS Error Count Low Read	R/W
20h	Alignment Error Count High Read	R/W
22h	Alignment Error Count Low Read	R/W
24h	Frame Too Long Count High Read	R/W
26h	Frame Too Long Count Low Read	R/W
28h	Runt Count High Read	R/W
2Ah	Runt Count Low Read	R/W
2Ch	Very Long Event Count High Read	R/W
2Eh	Very Long Event Count Low Read	R/W
30h	Data Rate Mismatch Count High Read	R/W
32h	Data Rate Mismatch Count Low Read	R/W
34h	Invalid Symbol Count High Read	R/W
36h	Invalid Symbol Count Low Read	R/W
38h	Reserved	
3Ah	Reserved	
3Ch	Source Address High Read	R/W
3Eh	Source Address Mid Read	R/W
40h	Source Address Low Read	R/W
42h	Reserved	
44h–7Eh	Reserved	

4.0 Registers (Continued)

4.1 REGISTER MEMORY MAP (Continued)

Address	Register	Access
80h	Carrier Count Register	R/W
82h	Oct_Nib Count Register	R/W
84h–8Eh	Reserved	
90h	Repeater Collisions High Read	R/W
92h	Repeater Collisions Low Read	R/W
94h	Network Utilization High Read	R/W
96h	Network Utilization Low Read	R/W
98h	False Carrier High Read	R/W
9Ah	False Carrier Low Read	R/W
9Ch–9Eh	Reserved	
A0h	Mil Read Data / Port 0-11 Short Event High Block Read Data	R only
A2h	DP83850 Port 0-11 Short Event Low Block Read Data	R only
A4h	DP83850 Port 0-11 Late Event High Block Read Data	R only
A6h	DP83850 Port 0-11 Late Event Low Block Read Data	R only
A8h	DP83850 Port 0-11 Collision High Block Read Data	R only
AAh	DP83850 Port 0-11 Collision Low Block Read Data	R only
ACh	DP83850 Port 0-11 Auto-Partitions Block Read Data	R only
AEh	Reserved	
B0h–1FEh	Reserved	

4.2 CONFIGURATION REGISTER

Address: 00h

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D0	MII_ACC	R/W	0: DP83856 writes 0 after register access completes 1: CPU initiates register access by writing 1 This bit indicates when the current DP83850 or Physical Layer device register access is complete.
D1	SR_ACC	R/W	0: DP83856 writes 0 after SRAM access completes 1: CPU initiates SRAM access by writing 1 This bit indicates when the current SRAM access is complete.
D2	SR_ACC_TYPE	R/W	0: Perform Single Access 1: Perform Block Access (Reads Only) All SRAM based statistics will be loaded into SRAM (CPU Addr. 10h–40h)
D3	MEN	R/W	0: Statistics gathering disabled 1: Statistics gathering enabled This bit enables managment statistics gathering. Note that subsequent read accesses should use read-modify-write instructions so that the MEN bit is left undisturbed.
D(4:7)	PAGE_SEL	R/W	These bits define which page of the register map the CPU is pointing to. Allows for 16 pages x 256 word registers. Always write 0 for compatibility with later versions of DP83856. Note: The Page bits are not implemented in current version.
D(8:15)	Reserved	R/W	Write: 0 Read: Undefined

4.0 Registers (Continued)

4.3 INTERRUPT REGISTER

Address: 02h

Reset: All bits cleared to zero.

Note: Mask bits must be set to enable valid status on corresponding status bits.

Bit	Bit Name	Access	Description
D0	MII_INT_STS	R	0: MII access complete Interrupt not asserted. 1: MII access complete Interrupt asserted. Cleared by read of register. Writes ignored.
D1	SR_ACC_STS	R	0: SRAM access complete Interrupt not asserted. 1: SRAM access complete Interrupt asserted. Cleared by read of register. Writes ignored.
D2	RIBERR_STS	R	0: DP83856 error Interrupt not asserted. 0: Mil access complete Interrupt not asserted. 1: DP83856 error Interrupt asserted. Cleared by read of register. Writes ignored.
D3	MII_RD_ERR_STS	R	0: MII register read error Interrupt not asserted. 1: MII register read error Interrupt asserted. Cleared by read of register. Writes ignored.
D4	MII_INT_MSK	R/W	0: Mask MII access complete Interrupt. 1: Enable MII access complete Interrupt.
D5	SR_ACC_MSK	R/W	0: Mask SRAM access complete Interrupt. 1: Enable SRAM access complete Interrupt.
D6	RIBERR_MSK	R/W	0: Mask DP83856 error Interrupt. 1: Enable DP83856 error Interrupt.
D7	MII_RD_ERR_MSK	R/W	0: Mask MII Register Error Interrupt. 1: Enable MII Register Error Interrupt.
D8	INT_EN	R/W	0: Disable $\overline{\text{CINT}}$ signal. 1: Enable $\overline{\text{CINT}}$ signal. This bit is a global enable for the $\overline{\text{CINT}}$signal. It has NO effect on the status bits.
D(9:15)	Reserved	R/W	Write: 0 Read: Undefined.

4.0 Registers (Continued)

4.4 SRAM INTERFACE REGISTER

Address: 06h

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:4)	STAT_ACC#	R/W	These bits set which STATISTIC the SRAM access is destined for. Values are: **00h:** Frame Count **02h:** Octet Count **04h:** SA Change Count **06h:** FCS Error Count **08h:** Alignment Error Count **0Ah:** Frame Too Long Count **0Ch:** Runt Count **0Eh:** Very Long Event Count **10h:** Data Rate Mismatch Count **12h:** Invalid Symbol Count **14h:** Reserved **16h:** Source Address High **18h:** Source Address Low **1Ah–1Eh:** Reserved
D(5:6)	Reserved	R/W	Always Write 0
D7	R/W_SRAM	R/W	0: SRAM Write 1: SRAM Read This bit defines whether the current CPU SRAM access is a read or a write.
D(8:11)	PORT_ACC#	R/W	These bits set which PORT number the access is destined for. Valid values are 0h–Bh (12 ports)
D(12:15)	RIC_ACC#	R/W	These bits set which DP83850 the access Is destined for. Valid values are 0h–Fh (16, DP83850s)

Note: This register should NOT be accessed while an SRAM access is in progress (If bit D1 of Configuration Register is 1, then do not access this register).

4.5 MII MANAGEMENT INTERFACE REGISTER

Address: 08h

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:4)	REG_ADDR	R/W	These bits set which register the access is destined for.
D(5:9)	DEV_ID	R/W	These bits set which DEVICE_ID the access is destined for.
D(10:11)	OPCODE	R/W	**OPCODE VALUE:** Corresponds to the opcodes defined in the MII specification. 01: Extended Addressed Mode Write, 16-bit payload. 10: Extended Addressed Mode Read, 16-bit payload.
D12	MII_ACC_TYP	R/W	**MII ACCESS TYPE:** Sets the access type to single or block read. 0: Perform Single Access (All Physical Layer device accesses and all DP83850 accesses except DP83850 counters). 1: Perform Block Read (DP83850 reads only). All DP83850 based counters will be loaded into registers (Address A0h–ACh). The OPCODE field is 10 for block reads. REG_ADDR is set to register address corresponding to the Port_ShortEvent Counter for the desired port.
D(13:15)	Reserved	R/W	Write: 0 Read: Undefined.

4.0 Registers (Continued)

4.6 SRAM WRITE DATA REGISTER

Address: 0Ah

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	WR_DATA	R/W	This register contains the data to be written on an SRAM write access. SRAM writes should only be performed during DP83856 initialization.

4.7 MII WRITE DATA REGISTER

Address: 0Ch

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	WR_DATA	R/W	This register contains the data to be written on an MII register write access.

4.8 DEVICE ID REGISTER

Address: 0Eh

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:3)	REV_LEVEL	R	These bits are the Revision level of the device and are embedded into the DP83856 silicon. Reads 0h for initial revision.
D(4:7)	DEVICE ID	R	These bits are a vendor specific code embedded in the DP83856. Reads 0h for initial revision.
D(8:15)	Reserved	R/W	Write: 0 Read: Undefined.

4.9 SRAM READ DATA REGISTERS

Addresses: 10h–40h

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	SRAM Read Data	R	Contains data corresponding to the SRAM location selected.

4.0 Registers (Continued)

4.10 CARRIER COUNT REGISTER

Address: 80h

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:13)	Carrier Count	R/W	Contains data which is used to preset the carrier counter FOR TEST PURPOSES ONLY. This register can only be written when the MEN bit in the CONFIG register is 0.
D(14:15)	Unused	R/W	Write: 0 Read: Undefined.

4.11 OCT_NIB COUNT REGISTER

Address: 82h

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:11)	Oct_Nib Count	R/W	Contains data which is used to preset the Octet-Nibble counter FOR TEST PURPOSES ONLY. This register can only be written when the MEN bit in the CONFIG register is 0.
D(12:15)	Unused	R/W	Write: 0 Read: Undefined.

4.12 NETWORK COUNTERS

Addresses: 90h–9Ah

Reset: All bits cleared to zero.

Bit	Bit Name	Access	Description
D(0:15)	Counter Data	R/W	Contains data corresponding to the selected counter. Disable the Management function by writing 0 to the MEN, bit D3 in the Config register prior to writing to these counters.

4.13 MII READ DATA REGISTERS

Addresses: A0h–ACh

Reset: Bit value at reset is indeterminate. Will probably read FFh due to bus pull-up.

Bit	Bit Name	Access	Description
D(15:0)	MII Data	R	Contains read data corresponding to the MII register selected.

For single Physical Layer Management register read accesses and single statistic read accesses to connected DP83850s, the read data appears in data register address A0h. When the DP83856 is instructed to do a block statistics read from a connected DP83850, the block of 7 read values is placed in the registers A0h–ACh. The register designations are given in the memory map in Section 4.1.

5.0 DP83856 Initialization

5.1 SRAM TEST AND INITIALIZATION

System vendors will often desire to test the SRAM as part of power-up initialization prior to enabling management. SRAM accesses are performed as follows:

SRAM Writes:

1. Program the SRAM Interface Register (06h) with the desired information.
2. Program the SRAM Write Data Register (0Ah) with the desired data.
3. Program the Configuration Register (00h) to disable management (D3 = 0), perform a single SRAM access (D2 = 0), and initiate the cycle (D1 = 1). (Note block access to SRAM is not allowed for Writes.)
4. Poll the Configuration Register (00h) for SRAM access complete (D1 = 0).
5. Repeat for next write.

SRAM Reads:

1. Program the SRAM Interface Register (06h) with the desired information.
2. Program the Configuration Register (00h) to enable management (D3 = 1), perform a single SRAM access (D2 = 0), and initiate the cycle (D1 = 1).
3. Poll the Configuration Register (00h) for SRAM access complete (D1 = 0).
4. Read the appropriate SRAM Read Data Register (10b–40h) to obtain data.
5. Repeat for next read.

Note that there are "holes" in the SRAM space, i.e., locations which are not accessible due to the statistic update implementation. The DP83856 implementation uses 8k x 16 of SRAM. Assuming the base address of the SRAM is 0000h, then the locations (word addresses) which are inaccessible are given in Table I below.

TABLE I. Unaccessible SRAM Locations (8k x 16 Map, word addressing, in hex)

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
0	0014	001A	001C	001E
0	0034	003A	003C	003E
0	0054	005A	005C	005E
0	0074	007A	007C	007E
0	0094	009A	009C	009E
0	00B4	00BA	00BC	00BE
0	00D4	00DA	00DC	00DE
0	00F4	00FA	00FC	00FE
0	0114	011A	011C	011E
0	0134	013A	013C	013E
0	0154	015A	015C	015E
0	0174	017A	017C	017E
0	0194	019A	019C	019E
0	01B4	01BA	01BC	01BE
0	01D4	01DA	01DC	01DE
0	01F4	01FA	01FC	01FE
1	0214	021A	021C	021E
1	0234	023A	023C	023E
1	0254	025A	025C	025E
1	0274	027A	027C	027E
1	0294	029A	029C	029E
1	02B4	02BA	02BC	02BE
1	02D4	02DA	02DC	02DE
1	02F4	02FA	02FC	02FE
1	0314	031A	031C	031E
1	0334	033A	033C	033E
1	0354	035A	035C	035E
1	0374	037A	037C	037E
1	0394	039A	039C	039E
1	03B4	03BA	03BC	03BE
1	03D4	03DA	03DC	03DE
1	03F4	03FA	03FC	03FE

5.0 DP83856 Initialization (Continued)

TABLE I. Unaccessible SRAM Locations (8k x 16 Map, word addressing, in hex) (Continued)

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
2	0414	041A	041C	041E
2	0434	043A	043C	043E
2	0454	045A	045C	045E
2	0474	047A	047C	047E
2	0494	049A	049C	049E
2	04B4	04BA	04BC	04BE
2	04D4	04DA	04DC	04DE
2	04F4	04FA	04FC	04FE
2	0514	051A	051C	051E
2	0534	053A	053C	053E
2	0554	055A	055C	055E
2	0574	057A	057C	057E
2	0594	059A	059C	059E
2	05B4	05BA	05BC	05BE
2	05D4	05DA	05DC	05DE
2	05F4	05FA	05FC	05FE
3	0614	061A	061C	061E
3	0634	063A	063C	063E
3	0654	065A	065C	065E
3	0674	067A	067C	067E
3	0694	069A	069C	069E
3	06B4	06BA	06BC	06BE
3	06D4	06DA	06DC	06DE
3	06F4	06FA	06FC	06FE
3	0714	071A	071C	071E
3	0734	073A	073C	073E
3	0754	075A	075C	075E
3	0774	077A	077C	077E
3	0794	079A	079C	079E
3	07B4	07BA	07BC	07BE
3	07D4	07DA	07DC	07DE
3	07F4	07FA	07FC	07FE

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
4	0814	081A	081C	081E
4	0834	083A	083C	083E
4	0854	085A	085C	085E
4	0874	087A	087C	087E
4	0894	089A	089C	089E
4	08B4	08BA	08BC	08BE
4	08D4	08DA	08DC	08DE
4	08F4	08FA	08FC	08FE
4	0914	091A	091C	091E
4	0934	093A	093C	093E
4	0954	095A	095C	O95E
4	0974	097A	097C	097E
4	0994	099A	099C	099E
4	09B4	09BA	09BC	09BE
4	09D4	09DA	09DC	09DE
4	09F4	09FA	09FC	09FE
5	0A14	0A1A	0A1C	0A1E
5	0A34	0A3A	0A3C	0A3E
5	0A54	0A5A	0A5C	0A5E
5	0A74	0A7A	0A7C	0A7E
5	0A94	0A9A	0A9C	0A9E
5	0AB4	0ABA	0ABC	0ABE
5	0AD4	0ADA	0ADC	0ADE
5	0AF4	0AFA	0AFC	0AFE
5	0B14	0B1A	0B1C	0B1E
5	0B34	0B3A	0B3C	0B3E
5	0B54	0B5A	0B5C	0B5E
5	0B74	0B7A	0B7C	0B7E
5	0B94	0B9A	0B9C	0B9E
5	0BB4	0BBA	0BBC	0BBE
5	0BD4	0BDA	0BDC	0BDE
5	0BF4	0BFA	0BFC	0BFE

5.0 DP83856 Initialization (Continued)

TABLE I. Unaccessible SRAM Locations (8k x 16 Map, word addressing, in hex) (Continued)

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
6	0C14	0C1A	0C1C	0C1E
6	0C34	0C3A	0C3C	0C3E
6	0C54	0C5A	0C5C	0C5E
6	0C74	0C7A	0C7C	0C7E
6	0C94	0C9A	0C9C	0C9E
6	0CB4	0CBA	0CBC	0CBE
6	0CD4	0CDA	0CDC	0CDE
6	0CF4	0CFA	0CFC	0CFE
6	0D14	0D1A	0D1C	0D1E
6	0D34	0D3A	0D3C	0D3E
6	0D54	0D5A	0D5C	0D5E
6	0D74	0D7A	0D7C	0D7E
6	0D94	0D9A	0D9C	0D9E
6	0DB4	0DBA	0DBC	0DBE
6	0DD4	0DDA	0DDC	0DDE
6	0DF4	0DFA	0DFC	0DFE
7	0E14	0E1A	0E1C	0E1E
7	0E34	0E3A	0E3C	0E3E
7	0E54	0E5A	0E5C	0E5E
7	0E74	0E7A	0E7C	0E7E
7	0E94	0E9A	0E9C	0E9E
7	0EB4	0EBA	0EBC	0EBE
7	0ED4	0EDA	0EDC	0EDE
7	0EF4	0EFA	0EFC	0EFE
7	0F14	0F1A	0F1C	0F1E
7	0F34	0F3A	0F3C	0F3E
7	0F54	0F5A	0F5C	0F5E
7	0F74	0F7A	0F7C	0F7E
7	0F94	0F9A	0F9C	0F9E
7	0FB4	0FBA	0FBC	0FBE
7	0FD4	0FDA	0FDC	0FDE
7	0FF4	0FFA	0FFC	0FFE

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
8	1014	101A	101C	101E
8	1034	103A	103C	103E
8	1054	105A	105C	105E
8	1074	107A	107C	107E
8	1094	109A	109C	109E
8	10B4	10BA	10BC	10BE
8	10D4	10DA	10DC	10DE
8	10F4	10FA	10FC	10FE
8	1114	111A	111C	111E
8	1134	113A	113C	113E
8	1154	115A	115C	115E
8	1174	117A	117C	117E
8	1194	119A	119C	119E
8	11B4	11BA	11BC	11BE
8	11D4	11DA	11DC	11DE
8	11F4	11FA	11FC	11FE
9	1214	121A	121C	121E
9	1234	123A	123C	123E
9	1254	125A	125C	125E
9	1274	127A	127C	127E
9	1294	129A	129C	129E
9	12B4	12BA	I2BC	12BE
9	12D4	12DA	12DC	12DE
9	12F4	12FA	12FC	12FE
9	1314	131A	131C	131E
9	1334	133A	133C	133E
9	1354	135A	135C	135E
9	1374	137A	137C	137E
9	1394	139A	139C	139E
9	13B4	13BA	13BC	13BE
9	13D4	13DA	13DC	13DE
9	13F4	13FA	13FC	13FE

5.0 DP83856 Initialization (Continued)

TABLE I. Unaccessible SRAM Locations (8k x 16 Map, word addressing, In hex) (Continued)

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
10	1414	141A	141C	141E
10	1434	143A	143C	143E
10	1454	145A	145C	145E
10	1474	147A	147C	147E
10	1494	149A	149C	149E
10	14B4	14BA	14BC	14BE
10	14D4	14DA	14DC	14DE
10	14F4	14FA	14FC	14FE
10	1514	151A	15IC	151E
10	1534	153A	153C	153E
10	1554	155A	155C	155E
10	1574	157A	157C	157E
10	1594	159A	159C	159E
10	15B4	15BA	15BC	15BE
10	15D4	15DA	15DC	15DE
10	15F4	15FA	15FC	15FE
11	1614	161A	161C	161E
11	1634	163A	163C	163E
11	1654	165A	165C	165E
11	1674	167A	167C	167E
11	1694	169A	169C	169E
11	16B4	16BA	16BC	16BE
11	16D4	16DA	16DC	16DE
11	16F4	16FA	16FC	16FE
11	1714	171A	171C	171E
11	1734	173A	173C	173E
11	1754	175A	175C	175E
11	1774	177A	177C	177E
11	1794	179A	179C	179E
11	17B4	17BA	17BC	17BE
11	17D4	17DA	17DC	17DE
11	17F4	17FA	17FC	17FE

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
12	1814	181A	181C	181E
12	1834	183A	183C	183E
12	1854	185A	185C	185E
12	1874	187A	187C	187E
12	1894	189A	189C	189E
12	18B4	18BA	18BC	18BE
12	18D4	18DA	18DC	18DE
12	18F4	18FA	18FC	18FE
12	1914	191A	191C	191E
12	1934	193A	193C	193E
12	1954	195A	195C	195E
12	1974	197A	197C	197E
12	1994	199A	199C	199E
12	19B4	19BA	19BC	19BE
12	19D4	19DA	19DC	19DE
12	19F4	19FA	19FC	19FE
13	1A14	1A1A	1A1C	1A1E
13	1A34	1A3A	1A3C	1A3E
13	1A54	1A5A	1A5C	1A5E
13	1A74	1A7A	1A7C	1A7E
13	1A94	1A9A	1A9C	1A9E
13	1AB4	1ABA	1ABC	1ABE
13	1AD4	1ADA	1ADC	1ADE
13	0AF4	0AFA	0AFC	0AFE
13	1B14	1B1A	1B1C	1B1E
13	1B34	1B3A	1B3C	1B3E
13	1B54	1B5A	1B5C	1B5E
13	1B74	1B7A	1B7C	1B7E
13	1B94	1B9A	1B9C	1B9E
13	1BB4	1BBA	1BBC	1BBE
13	1BD4	1BDA	1BDC	1BDE
13	1BF4	1BFA	1BFC	1BFE

5.0 DP83856 Initialization (Continued)

TABLE I. Unaccessible SRAM Locations (8k x 16 Map, word addressing, in hex) (Continued)

DP83850 #	Offset xx4	Offset xxA	Offset xxC	Offset xxE
14	1C14	1C1A	1C1C	1C1E
14	1C34	1C3A	1C3C	1C3E
14	1C54	1C5A	1C5C	1C5E
14	1C74	1C7A	1C7C	1C7E
14	1C94	1C9A	1C9C	1C9E
14	1CB4	1CBA	1CBC	1CBE
14	1CD4	1CDA	1CDC	1CDE
14	1CF4	1CFA	1CFC	1CFE
14	1D14	1D1A	1D1C	1D1E
14	1D34	1D3A	1D3C	1D3E
14	1D54	1D5A	1D5C	1D5E
14	1D74	1D7A	1D7C	1D7E
14	1D94	1D9A	1D9C	1D9E
14	1DB4	1DBA	1DBC	1DBE
14	1DD4	1DDA	1DDC	1DDE
14	1DF4	1DFA	1DFC	1DFE
15	1E14	1E1A	1E1C	1E1E
15	1E34	1E3A	1E3C	1E3E
15	1E54	1E5A	1E5C	1E5E
15	1E74	1E7A	1E7C	1E7E
15	1E94	1E9A	1E9C	1E9E
15	1EB4	1EBA	1EBC	1EBE
15	1ED4	1EDA	1EDC	1EDE
15	1EF4	1EFA	1EFC	1EFE
15	1F14	1F1A	1F1C	1F1E
15	1F34	1F3A	1F3C	1F3E
15	1F54	1F5A	1F5C	1F5E
15	1F74	1F7A	1F7C	1F7E
15	1F94	1F9A	1F9C	1F9E
15	1FB4	1FBA	1FBC	1FBE
15	1FD4	1FDA	1FDC	1FDE
15	1FF4	1FFA	1FFC	1FFE

5.2 NETWORK COUNTER INITIALIZATION

The network counters described in Sections 3.1.4 (Collision Counter), 3.1.5 (Network Utilization Counter), and 3.1.6 (False Carrier Counter) are cleared by power-up reset and require no further initialization.

5.3 INTERRUPT INITIALIZATION AND USAGE

The DP83856 supports, but does not require, the use of external interrupts. Interrupts are initialized by programming the Interrupt Register (02h). Interrupt generation and control is described in Section 3.4.

The following is one suggestion on how to use interrupts:

First of all, the agent will probably want to receive updated statistic information based on a timer tick, say once every second.

Software will want to get all of the statistics for each port, so it needs to talk to both the DP83856 and the DP83850.

Using the Block SRAM Read feature of the DP83856, software will have to wait on the order of 10 μs for the DP83856 to complete the SRAM dump per port. Thus, it does not seem worthwhile to use interrupts given the overhead of getting in/out of the interrupt service routine.

Using the Block MII Read feature of the DP83856, software will have to wait on the order of 100 μs for the DP83856 to complete the DP83850 register dump. (7 MII accesses @ 32 x 400 ns per access, plus overhead) thus, this is where interrupt usage is recommended. Allow software go off and do something else while the DP83850 registers are being read.

The next issue is the MII read error. Software will probably poll the stack of hubs periodically, looking for the addition or removal of a hub from the stack. It is assumed that this polling routine is not executed very often, perhaps once every 5s or 10s. MII_RD_ERR interrupts should only be generated by accessing hubs that are not there (although damaged units may also not respond). The point is that an insignificant number of MII_RD_ERR interrupts should be generated, and thus very little bandwidth should be expended servicing these.

In summary, enable interrupts for MII accesses and MII read errors, but not SRAM accesses.

6.0 Repeater MIB Support

6.1 REPEATER MIB SUPPORT

The following tables enumerate the groups within IEEE 802.3 u/D5, Clause 30 Repeater MIB, and the mapping to the DP83856/DP83850/DP83840 system implementation.

BASIC GROUP

Repeater Managed Object Class	Implemented In:
aRepeaterID	SW
aRepeaterType	SW
aRepeaterGroupCapacity	SW
aGroupMap	SW
aRepeaterHealthState	SW
aRepeaterHealthText	SW
aRepeaterHealthData	SW
aTransmitCollisions	DP83856
acResetRepeater	SW, DP83850
acExecuteNonDisruptiveSelfTest	SW
nRepeaterHealth	SW
nRepeaterReset	SW
nGroupMapChange	SW

Group Managed Object Class	Implemented In:
aGroupID	SW
aGroupPortCapacity	SW
aPortMap	SW
nPortMapChange	SW

BASIC GROUP (Continued)

Repeater Port Managed Object Class	Implemented In:
aPortID	SW
aPortAdminState	SW
aAutoPartitionState	DP83850
aReadableFrames	DP83856
aReadableOctets	DP83856
aFrameCheckSequenceErrors	DP83856

Repeater Port Managed Object Class	Implemented In:
aAlignmentErrors	DP83856
aFramesTooLong	DP83856
aShortEvents	DP83850
aRunts	DP83856
aCollisions	DP83850
aLateEvents	DP83850
aVeryLongEvents	DP83856
aDataRateMismatches	DP83856
aAutoPartitions	DP83850
aIsolates	Plexus
aSymbolErrorDuringPacket	DP83856
aLastSourceAddress	DP83856
aPortAdminControl	SW

7.0 AC and DC Specifications

7.1 DC SPECIFICATIONS

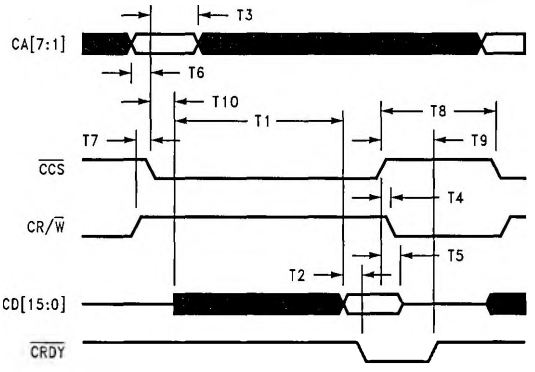
Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Minimum High Level Output Voltage		3.7		V
V_{OL}	Minimum Low Level Output Voltage			0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low Level Input Voltage			0.8	V
I_{IN}	Input Current			± 150	μA
I_{OZ}	Minimum TRI-STATE Output Leakage Current			± 160	μA
I_{CC}	Supply Current (Calculated)			150	mA

7.2 AC SPECIFICATIONS

Some timing parameters are shown more than once (both on the same timing diagram, and in different sections) for clarity.

7.2.1 CPU Read Timing

Parameter	Description	Min (ns)	Max (ns)
T1	$\overline{CSS}$ low to CPU Data valid		180
T2	CPU Data valid to $\overline{CRDY}$ low	10	
T3	CPU Address hold from $\overline{CSS}$ low	60	
T4	CR/$\overline{W}$ hold from $\overline{CSS}$ high	0	
T5	CPU Data hold from $\overline{CSS}$ high	0	
T6	CPU Address setup to $\overline{CSS}$ low	0	
T7	CR/$\overline{W}$ setup to $\overline{CSS}$ low	0	
T8	$\overline{CSS}$ high between cycles	100	
T9	$\overline{CSS}$ high to $\overline{CRDY}$ high		60
T10	$\overline{CSS}$ low to CPU Data driven	0	20



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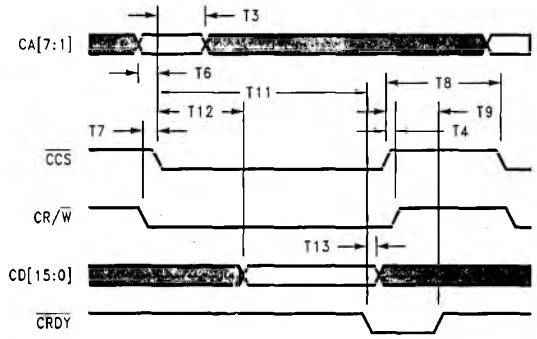
7.0 AC and DC Specifications (Continued)

7.2.2 CPU Write Timing

Parameter	Description	Min (ns)	Max (ns)
T3	CPU Address hold from $\overline{CSS}$ low	60	
T4	CR/$\overline{W}$ hold from $\overline{CSS}$ high	0	
T6	CPU Address setup to $\overline{CSS}$ low	0	
T7	CR/$\overline{W}$ setup to $\overline{CSS}$ low	0	
T8	$\overline{CSS}$ high between cycles	100	
T9	$\overline{CSS}$ high to $\overline{CRDY}$ high		60
T11	$\overline{CSS}$ low to $\overline{CRDY}$ low		180
T12	$\overline{CSS}$ low to CPU Data valid		70
T13	CPU Data hold from $\overline{CRDY}$ low	0	



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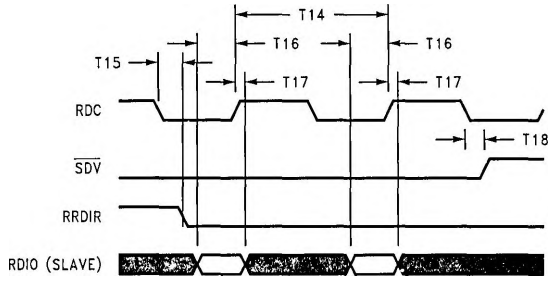
7.2.3 MII Slave Timing (DP83856 Receiving Data on RDIO)

Parameter	Description	Min (ns)	Typ (ns)	Max (ns)
T14	RDC pulse width		400	
T15	RDC falling edge to RRDIR			60
T16	RDIO setup to RDC rising edge	10		
T17	RDIO hold from RDC rising edge	0		
T18	RDC falling edge to $\overline{SDV}$ high			60



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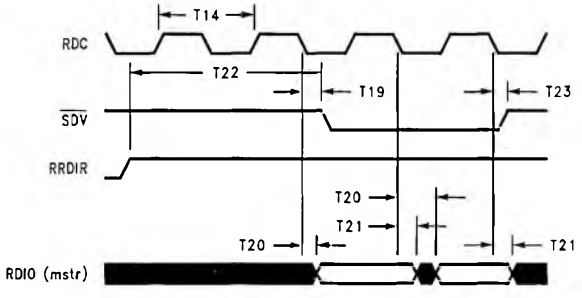
7.0 AC and DC Specifications (Continued)

7.2.4 MII Master Timing (DP83856 Sending Data on RDIO)

Parameter	Description	Min (ns)	Typ (ns)	Max (ns)
T14	RDC pulse width		400	
T19	RDC falling edge to $\overline{SDV}$ falling edge			60
T20	RDC falling edge to RDIO valid			60
T21	RDC falling edge to RDIO invalid	0		
T22	RRDIR rising edge to $\overline{SDV}$ falling edge	600		
T23	RDC falling edge to $\overline{SDV}$ rising edge			60



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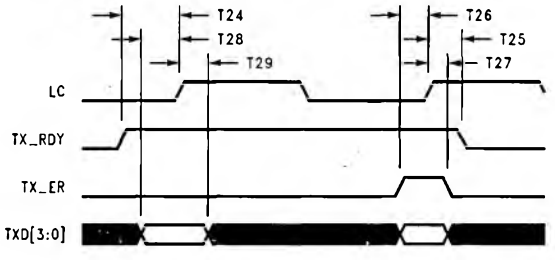
7.2.5 TX Bus Timing

Parameter	Description	Min (ns)	Typ (ns)	Max (ns)
T24	TX_RDY setup to LC rising edge	9		
T25	TX_RDY hold from LC rising edge	3		
T26	TX_ER setup to LC rising edge	5		
T27	TX_ER hold from LC rising edge	2		
T28	TXD[3:0] setup to LC rising edge	6		
T29	TXD[3:0] hold from LC rising edge	2		



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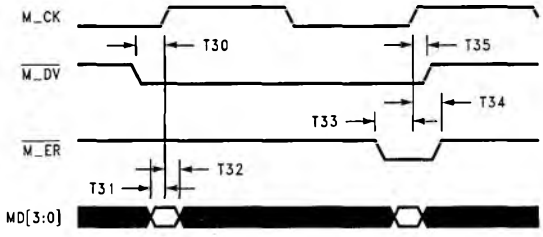
7.0 AC and DC Specifications (Continued)

7.2.6 Management Bus Timing

Parameter	Description	Min (ns)	Typ (ns)	Max (ns)
T30	$\overline{M\_DV}$ setup to M_CK rising edge	3		
T31	MD[3:0] setup to M_CK rising edge	1		
T32	MD[3:0] hold from M_CK rising edge	0		
T33	$\overline{M\_ER}$ setup to M_CK rising edge	3		
T34	$\overline{M\_ER}$ hold from M_CK rising edge	1		
T35	$\overline{M\_DV}$ hold from M_CK rising edge	1		



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7.2.7 SRAM Read Timing

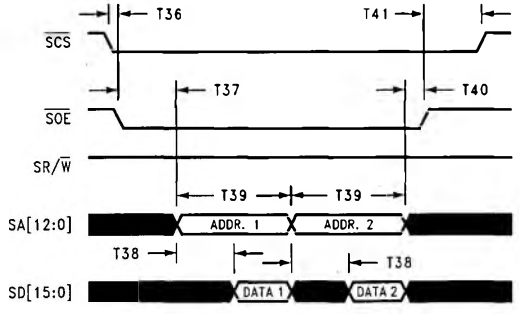
Parameter	Description	Min (ns)	Typ (ns)	Max (ns)
T36	$\overline{SCS}$ low to $\overline{SOE}$ low	0		
T37 (Note 1)	$\overline{SOE}$ low to SA[12:0] valid		20	30
T38 (Note 2)	SA[12:0] valid to SD[15:0] valid (SRAM t_{su})			25
T39 (Note 3)	SA[12:0] width	50		
T40 (Note 4)	SA[12:0] invalid to $\overline{SOE}$ high	0		
T41	$\overline{SOE}$ high to $\overline{SCS}$ high	35		

Note 1: All SRAM read cycles are Address controlled.

Note 2: SRAM must have a read access time of 20 ns or faster.

Note 3: The DP83856 latches data prior to changing the SA[12:0] value.

Note 4: The DP83856 latches data prior to terminating $\overline{SOE}$.



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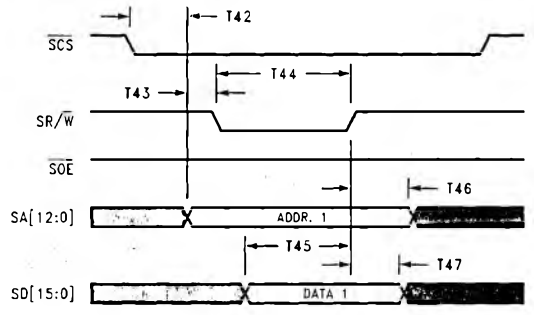
7.0 AC and DC Specifications (Continued)

7.2.8 SRAM Write Timing

Parameter	Description	Min (ns)	Typ (ns)	Max (ns)
T42	$\overline{SCS}$ low to SA[12:0] valid	30		
T43	SA[12:0] valid to SR/$\overline{W}$ low	10		
T44	SR/$\overline{W}$ width	35		
T45	SD[15:0] valid to SR/$\overline{W}$ high	25		
T46	SR/$\overline{W}$ high to SA[12:0] invalid	15		
T47	SR/$\overline{W}$ high to SD[15:0] invalid	15		



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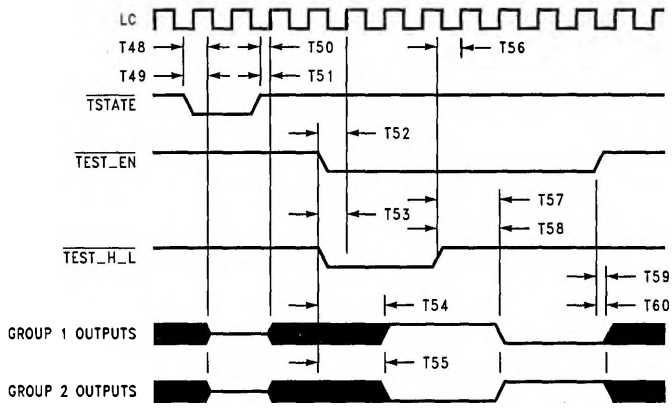
7.0 AC and DC Specifications (Continued)

7.2.9 Test Mode Timing

Parameter	Description	Min (ns)	Typ (ns)	Max (ns)
T48	$\overline{\text{TSTATE}}$ low to Group 1 Outputs Hi-Z			25
T49	$\overline{\text{TSTATE}}$ low to Group 2 Outputs Hi-Z			25
T50	$\overline{\text{TSTATE}}$ high to Group 1 Outputs driven			25
T51	$\overline{\text{TSTATE}}$ high to Group 2 Outputs driven			25
T52	$\overline{\text{TEST\_EN}}$ low setup to LC rising edge	20		
T53	$\overline{\text{TEST\_H\_L}}$ low setup to LC rising edge	20		
T54	$\overline{\text{TEST\_EN}}$, $\overline{\text{TEST\_H\_L}}$ low to Group 1 Outputs high			2 * LC + 0ns
T55	$\overline{\text{TEST\_EN}}$, $\overline{\text{TEST\_H\_L}}$ low to Group 2 Outputs low			2 * LC + 0ns
T56	$\overline{\text{TEST\_H\_L}}$ high setup to LC rising edge	20		
T57	$\overline{\text{TEST\_EN}}$ low, $\overline{\text{TEST\_H\_L}}$ high to Group 1 Outputs low			2 * LC + 0ns
T58	$\overline{\text{TEST\_EN}}$ low, $\overline{\text{TEST\_H\_L}}$ high to Group 2 Outputs high			2 * LC + 0ns
T59	$\overline{\text{TEST\_EN}}$ high to Group 1 Outputs undefined			2 * LC + 0ns
T60	$\overline{\text{TEST\_EN}}$ high to Group 2 Outputs undefined			2 * LC + 0ns



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Group 1 output pin numbers are:
21, 23, 27, 31, 35, 37, 39, 43, 61, 64, 68, 70, 72, 74, 78, 80, 82, 87, 89, 90, 92, 96, 98, 100, 104, 108, 113, 115.

Group 2 output pin numbers are:
20, 22, 24, 30, 34, 36, 38, 42, 44, 65, 69, 71, 73, 75, 79, 81, 83, 88, 91, 93, 97, 99, 103, 105, 114, 116.