National Semiconductor

DP84412 Dynamic RAM Controller Interface Series Circuit for the Series 32000[®] CPU

General Description

Connection Diagram

The DP84412 is a new Programmable Array Logic (PAL®) device, that replaces the DP84312, designed to allow an easy interface between the National Semiconductor Series 32000 family of processors and the National Semiconductor DP8409A, DP8429, or DP8419 DRAM controller.

The new DP84412 supplies all the control signals needed to perform memory read, write and refresh and work with the National Semiconductor Series 32000 family of processors up to 10 MHz. Logic is also included to insert WAIT states, if wanted, into the microprocessor READ or WRITE cycles when using fast CPUs.

Features

Provides a 3-chip solution for the Series 32000 family, dynamic RAM interface (DP8409A or DP8419, DP84412, and clock divider).

- Works with all Series 32000 family speed versions up to 10 MHz.
- Operation of Series 32000 processor at 10 MHz with no WAIT states.
- Controls DP8409A or DP8419 Mode 5 accesses, hidden refreshes and Mode 1 Forced Refreshes automatically.
- Inserts WAIT states in READ or WRITE cycles automatically depending on whether WAITRD or WAITWR are low, or if CS becomes active during a forced Refresh cycle.
- Uses a standard National Semiconductor PAL part (DMPAL16R6A).
- The PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new very high speed PALs ("B" PAL parts).



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	Operating	Programming
Supply Voltage, V _{CC}	7V	12V
Input Voltage	5.5V	12V

Off-State Output Voltage Storage Temperature Range

ige 5.5V 12V Range - -65°C to + 150°C

Recommended Operating Conditions

Symbol	Parameter		Commercial			11-14-
			Min	Тур	Max	Units
V _{CC}	Supply Voltage		4.75	5	5.25	v
•	Width of Clock	Low	15	10		
L.W.		High	15	10		ns
t _{su}	Setup Time from Input or Feedback to Clock		25	16		ns
t _h	Hold Time		0	-10		ns
T _A	Operating Free-Air Temperature		0	25	75	°C
т _с	Operating Case Temperature					°C

Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Тур	Max	Units
VIH	High Level Input Voltage			2			V
VIL	Low Level Input Voltage					0.8	v
VIC	Input Clamp Voltage	$V_{CC} = Min, I_1$	= -18 mA		-0.8	-1.5	v
V _{OH}	High Level Output Voltage	$V_{CC} = Min$ $V_{IL} = 0.8V$ $V_{IH} = 2V$	I _{OH} = -3.2 mA COM	2.4	2.8		v
V _{OL}	Low Level Output Voltage	$V_{CC} = Min$ $V_{IL} = 0.8V$ $V_{IH} = 2V$	I _{OL} = 24 mA COM		0.3	0.5	v
lozн		$V_{CC} = Max$ $V_{IL} = 0.8V$ $V_{IH} = 2V$	$V_{O} = 2.4V$			100	μΑ
IOZL	Off-State Output Current		$V_0 = 0.4V$			- 100	μA
lj -	Maximum Input Current	$V_{CC} = Max, V_I = 5.5V$				1	mA
lін	High Level Input Current	$V_{CC} = Max, V_I = 2.4V$				25	μA
ΙL	Low Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.02	-0.25	mA
los	Output Short-Circuit Current	$V_{CC} = 5V$ $V_0 = 0V$		-30	-70	-130	mA
lcc	Supply Current	V _{CC} = Max			120	180	mA

Switching Characteristics Over Recommended Ranges of Temperature and V_{CC} $V_{CC} = 5V \pm 10\%$. Commercial: T_A = 0°C to 75°C, V_{CC} = 5V ±5%

Symbol	Parameter	Test Conditions R1, R2	Commercial			Linite
			Min	Тур	Max	Onita
t _{PD}	Input or Feedback to Output			15	25	ns
^t CLK	Clock to Output or Feedback	CL = 50 pF		10	15	ns
t _{PZX}	Pin 11 to Output Enable			10	20	ns
t _{PXZ}	Pin 11 to Output Disable	$C_L = 5 pF$		11	20	ns
t _{PZX}	Input to Output Enable	$C_L = 50 pF$		10	25	ns
t _{PXZ}	Input to Output Disable	$C_L = 5 pF$		13	25	ns
f _{MAX}	Maximum Frequency		25	30		ns

V_{CC} = Max at minimum temperature.



PAL For Series 32000 Family Systems

TL/F/8397-2

DP84412

Mnemonic Description

	TE SIGNAL S	•
1)	"ECI K"	East clock from the NS22201 TCU
.0	TOLK	eleck chip, this signal rups at twiss
		the encoded the system electric
2)	"TOO"	From the NS22201 TCU clock.
2)	150	From the NS32201 TCU clock chip,
		this signal indicates the start of the
		"12" state and goes high at the be-
.		ginning of the "T4" state.
3)	"RFI/O"	RFRQ (refresh request) in mode 5.
		From 8409A, an active low signal.
4)	"ADS"	From the Series 32000 CPU, address
		strobe. If the system includes the
		MMU (NS32082) then PAV should be
		connected to this input.
5)	"DDIN"	Used to differentiate between READ
		and WRITE cycles, and to allow CS
		READ cycles to start early.
6)	"WAITWRITE"	This signal is used to add a WAIT
- /		state into a CS WRITE access cycle
		and delay RASIN until the end of the
		"T2" clock period
7)	"CTTL"	From the NS32201 TCU clock chip
''	OTTE	this signal runs at the system clock
		this signal runs at the system clock
0)		From decoder chin (chin coloct) (co
0)	05	From decoder chip (chip select) (ac-
•		tive low).
9)	"WAITREAD"	Used to insert 1 wait state into the Se-
		ries 32000 READ bus cycle. The wait
		state allows the use of memory with
		longer access times (t _{CAC}). An active
	and a starting	low signal.
10)	"OE"	This input enables the outputs of the
		"D-Flip Flop" outputs of the PAL.
OUT		
1)	NODE"	This sis sees to MO on the DD04004
0	MODE	This pin goes to W2 on the DP8409A
		to change from mode 5 to mode 1
		(only used for forced refresh).
2)	"2DLY"	Delay used internal to the PAL.
3)	"3DLY"	Delay used internal to the PAL.
4)	"4DLY"	Delay used internal to the PAL.
5)	"RASIN"	To the 8409A (creates RASs). Goes
		low earlier for READ cycles than
		WRITE cycles.
6)	"CYCLED"	Goes active low once a hidden re-
,		fresh (non CS cycle) or DRAM access
		has been performed CYCLED always
		does low at the beginning of the "T2"
		goes low at the beginning of the 13
		processor state. This signal goes high
		(reset) by the end of the processor
		bus cycle as indicated by 150 being
		high.
7)	"CWAIT"	This output inserts "WAIT" or
		"HOLD" states into the NS32016 ma-
		chine cycles (only WAIT states are
		used in this application). This output is
		in "not enabled" condition when CS is
		high (not chip selected).
8)	"INCYCLE"	This signal goes active from the CPU
		ADS signal. This signal indicates that
		the processor is doing an access
		somewhere in the system This signal
		stave low for soveral T states of the
		Stays IUW IUI Several I States of the
		access cycle.

Functional Description

The following description applies to both the DP8409A and the DP8419 dynamic RAM controllers.

A memory cycle starts when chip select (\overline{CS}) and address strobe (\overline{ADS}) are true. RASIN is supplied from the DP84412 to the DP8409A dynamic RAM controller, which then supplies a RAS signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8409A switches the address outputs to the column address. The DP8409A then supplies the required CAS signal to the DRAM. In order to do byte operations it is suggested that the user provide external logic, as shown in the system block diagram, to produce a HIGH WRITE ENABLE and/or a LOW WRITE ENABLE. To differentiate between a READ and a WRITE, the DDIN signal from the CPU is used. DDIN is also supplied to the external WRITE ENABLE logic.

A refresh cycle is started by one of two conditions. The refresh cycle caused by the first condition is called a hidden refresh. This occurs when refresh clock (RFCK) is high, CS is not true, and RASIN goes true. Here the CPU is accessing something else in the system and the DRAM can be refreshed at that time, thereby being transparent to the CPU. The second type of refresh is called forced refresh. This occurs if no hidden refresh was performed while RFCK was high. When RFCK transitions low a refresh request (RFRQ) is generated. If there is not a DRAM access in progress the DP84412 will force a refresh by putting the DP8409A into mode 1 (automatic forced refresh mode). If the CPU tries to access the DRAM during a forced refresh cycle WAIT states will be inserted into its cycles until the forced refresh is over and the DRAM RAS precharge time has been met. Then the pending DRAM access will be allowed to take place.

The DP84412 also allows forced refreshes to take place during long accesses of other devices. For instance, if EEPROM takes several microseconds to write to, the DRAM will still be refreshed while that access is in progress.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories or allow time to generate parity. This is accomplished by inserting a WAIT state into the processor access cycle. The DP84412 can insert WAIT states into either READ or WRITE cycles, or both. The extra WAIT state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

System Interface Description

All members of the Series 32000 family of processors are able to use the DP84412.

The DP84412 differentiates between READ and WRITE cycles, allowing the RASIN signal to start earlier during a READ cycle compared to a WRITE cycle.

RASIN during a READ cycle will always start at the beginning of the "T2" processor cycle. The user must also guarantee that \overline{CS} is valid a minimum of 30 ns before RASIN becomes valid. The worst case would be at 10 MHz where FCLK preceeds PHI1 by a maximum of 10 ns. RASIN can occur a minimum of approximately 8 ns after FCLK. Therefore \overline{CS} must occur a minimum of 32 ns (30 ns+2 ns) before the rising edge of PHI1 at 10 MHz.

The user may want to tie \overline{CS} low on the DP8409A/19 (disable HIDDEN REFRESH) and use the system transceivers to select the DRAM. In this case one only needs to concern himself with the 10 ns address setup time to \overline{RASIN} .

System Interface Description (Continued)

The DP84412 can be used in a system with the MMU (NS32082) but the signal PAV would be connected to the ADS input instead of ADS.

Several other critical parameters in this application that involve the input signals DDIN, CWAIT, TSO, and FCLK. These parameters become most critical at 10 MHz where it is suggested that they are directly connected to the corresponding pins of the Series 32000 family ICs.

This section of the data sheet goes through the calculation of the "tRAC" (RAS access time) and "tCAC" (CAS access time) required by the DRAM for the Series 32000 family CPUs to operate at a particular clock frequency without introducing wait states into the processor access cycles. Both "tRAC" and "tCAC" must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "tRAC" and "tCAC" parameters calculated. In order to determine the "tRAC" and "tCAC" needed the DP8419 and fast PALs ("B" type PALs) timing parameters were used. If the user is using the DP8408A/09A or a slower PAL device he should substitute their respective delays into the equations below.

Most all of the calculations contained in this note use "RAHS" = 1 (15 ns guaranteed minimum row address hold time). Calculations only used "RAHS" = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from RAS exceeded 200 ns. This is because DRAMs can be found with row access times up to 150 ns that require only 15 ns row address hold times.

EXAMPLE DRAM TIMING CALCULATIONS

A) 8 MHz Series 32000 CPU, No Wait states

- #1) RASIN = T1 2 ns (FCLK to PHI1 skew) + 12 ns ("B" PAL clocked output) = 125 - 2 + 12 = 135 ns maximum
- #2) RASIN to RAS low = 20 ns maximum (DP8419)
- #3) RASIN to CAS low = 80 ns (DP8419 RASIN CAS low) - 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns
- #4) 74F245 transceiver delay = 7 ns maximum
- #5) CPU data setup time to "T4" = data setup to PHI2 T.E. + maximum PHI2 F.E. to PHI1 R.E. = 15 + 5 = 20 ns minimum
- "tRAC" = T1 + T2 + T3 #1 #2 #4 #5

= 125 + 125 + 125 - 135 - 20 - 7 - 20 = 193 ns

"tCAC" = T1 + T2 + T3 - #1 - #3 - #4 - #5

$$= 125 + 125 + 125 - 135 - 77 - 7 - 20 = 136$$
 ns

Therefore the DRAM chosen should have a "tRAC" less then or equal to 193 ns and a "tCAC" less than or equal to 136 ns. Standard 150 ns DRAMs meet this criteria.

The minimum RAS PRECHARGE TIME will be approximately one and one half clock periods = 125 + 62 = 187 ns.

The minimum CAS PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 125 + 62 + 35 = 222 ns.

The minimum RAS PULSE WIDTH will be approximately two clock periods -5 ns (maximum t_{RPDL}-t_{RPDH} for the DP8409-2) = 250 -5 = 245 ns.

The minimum CAS PULSE WIDTH will be approximately two clock periods - 70 ns (maximum $t_{RICL}-t_{RICH}$ for the DP8409-2) = 250 - 70 = 180 ns.

The smallest pulse widths are generated during WRITE cycles since RASIN during WRITE cycles starts later than RASIN during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times and the RAS pulse width would be increased by one clock period (125 ns in this case). A WAIT state in WRITE cycles would just increase the RAS pulse width by one clock period.

B) 10 MHz Series 32000, No Walt States

- #1) RASIN low = T1 2 ns (FCLK PHI1 skew) + 12 ns ("B" PAL clocked output) = 100 - 2 + 12 = 110 ns maximum
- #2) RASIN to RAS low = 20 ns maximum
- #3) RASIN to CAS low = 80 ns maximum (DP8419 RASIN -CAS low) - 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns
- #4) 74F245 transceiver delay = 7 ns maximum
- #5) CPU data setup time to "T4" = data setup to PHI2 T.E. + maximum PHI2 F.E. to PHI1 R.E. = 15 + 5 = 15 ns minimum

"tRAC" = T1 + T2 + T3 - #1 - #2 - #4 - #5

= 100 + 100 + 100 - 110 - 20 - 7 - 15 = 148 ns

"tCAC" = T1 + T2 + T3 - #1 - #3 - #4 - #5

= 100 + 100 + 100 - 110 - 77 - 7 - 15 = 91 ns

Therefore the DRAM chosen should have a "tRAC" less then or equal to 148 ns and a "tCAC" less than or equal to 91 ns. Standard 120 ns DRAMs meet this criteria.

The minimum \overrightarrow{RAS} PRECHARGE TIME will be approximately one and one half clock periods = 100 + 50 = 150 ns.

The minimum $\overline{\text{CAS}}$ PRECHARGE TIME will be approximately one and one half clock periods plus 35 ns (minimum $t_{\text{RICL}} - t_{\text{RICH}}$ for the DP8409-2) = 100 + 50 + 35 = 185 ns.

The minimum RAS PULSE WIDTH will be approximately two clock periods -5 ns (maximum t_{RPDL}-t_{RPDH} for the DP8409-2) = 200 - 5 = 195 ns.

The minimum CAS PULSE WIDTH will be approximately two clock periods -70 ns (maximum $t_{RICL} - t_{RICH}$ for the DP8409-2) = 200 -70 = 130 ns.

The smallest pulse widths are generated during WRITE cycles since RASIN during WRITE cycles starts later than RASIN during READ cycles.

If one inserted a WAIT state in READ cycles the DRAM column access times and the RAS pulse width would be increased by one clock period (100 ns in this case). A WAIT state in WRITE cycles would just increase the RAS pulse width by one clock period.

SUGGESTIONS

It is suggested that the DP8409A could be used up to 8 MHz. Above 8 MHz one should use the DP8409-2 or the DP8419. Also, fast PALs ("A" or "B" parts) should be used at 8 MHz and above.

INTERPRETING THE DP84412 PAL EQUATIONS

The boolean equations for the DP84412 were written using the standard PALASMTM format. In other words the equation: "IF (V_{CC}) RASIN=INCY*MODE*4D*DDIN" will mean;

The output "RASIN" (see pin list for DP84412) will be active low (inverted RASIN) when the output "INCY" is low (making INCY high) AND the output "MODE" is high AND the output "4D" is low (making 4D high) AND the input DDIN is low (making DDIN high).

PAL Boolean Equations

PALLERGA ;FAST PAL NEW PAL FOR THE NATIONAL SEMICONDUCTOR NS32016, 32008, 32032 NATIONAL SEMICONDUCTOR (WORKS UP 10 MHz)

FCLK TSO RFIO ADS DDIN WAITWR CTTL CS WAITRD GND DE CWAIT 4DLY 3DLY 2DLY MODE RASIN CYCLED INCY VCC

 RASIN := INCY*CYCLED*WODE*CTTL*DDIN+
 ;Start RASIN fast during

 INCY*MODE*2DLY*WAITWR+
 ;"READ" cycle

 INCY*MODE*2DLY+
 ;'WRITE'' cycle without WAIT states

 CS*INCY*MODE*2DLY*WAITWR*CTTL+
 ;'WRITE'' cycle with WAIT states

 RASIN*INCY*MODE*2DLY
 ; Continue RASIN

CYCLED := MODE * 2DLY * WAITWR * DDIN * CTTL + ;No WAITS inserted MODE * 2DLY * WAITRD * DDIN * CTTL + ;No WAITS inserted MODE * 2DLY * 4DLY * WAITRD * DDIN * CTTL + ;WAIT in READ cycle MODE * 2DLY * 4DLY * WAITWR * DDIN * CTTL + ;WAIT in WRITE cycle CYCLED * TSO * MODE + CYCLED * MODE * CTTL

 MODE := RFI0*INCY*2DLY*CTTL+
 ;forced refresh during idle

 MODE*3DLY+
 ;or at the end of a cycle

 MODE*4DLY+
 ;or at the end of a cycle

MODE*4DLY+ MODE*CTTL

2DLY := MODE*4DLY*CTTL+ 2DLY*CTTL+ INCY*CYCLED*MODE*3DLY*4DLY*CTTL+ CS*DDIN*WAITRD*INCY*MODE*2DLY*3DLY*4DLY+ CS*DDIN*WAITWR*INCY*MODE*2DLY*3DLY*4DLY ; WAIT states are wanted

3DLY := 2DLY*4DLY*CTTL+ 3DLY*CTTL

4DLY := 3DLY*CTTL+ 4DLY*CTTL+ INCY*MODE*CTTL+ INCY*MODE*CTTL+

IF (VCC) INCY = ADS*MODE+ CS*TSO*CYCLED*MODE*2DLY*4DLY+ ;Start INCY for CS INCY*CYCLED+ ;access after forced INCY*2DLY :refresh

; CS WRITE cycle with

; WAIT states

FIGURE 1. Equations for the Series 32000 Family Interface PAL

System Timing Diagrams





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System Timing Diagrams (Continued)

DP84412



TL/F/8397-5



System Timing Diagrams (Continued)





System Timing Diagrams (Continued)

