National Semiconductor

**PRELIMINARY**

# DP84432 Dynamic RAM Controller Interface Circuit for the 8086/8088/80186/80188 CPU's

## General Description

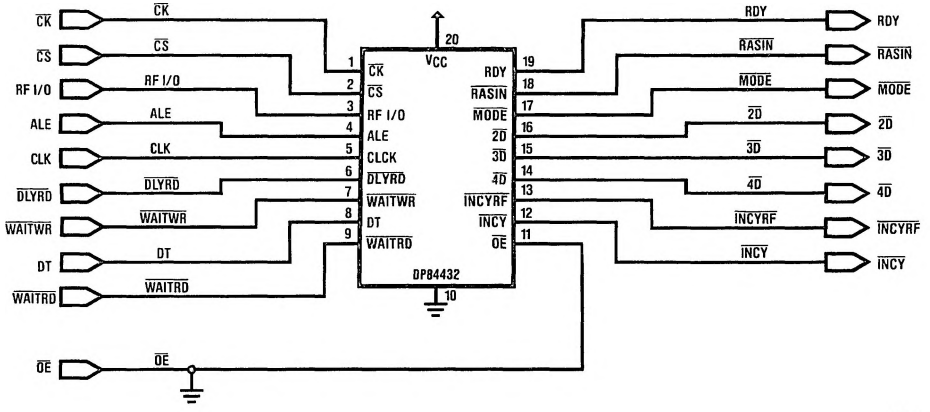
The DP84432 is a new Programmable Array Logic (PAL®) device, that replaces the DP84332, designed to allow an easy interface between the Intel 8088, 8086, 80188, 80186 CPU's and the National Semiconductor DP8409A, DP8429, or DP8419 DRAM controller.

The new DP84432 supplies all the control signals needed to perform memory read, write and refresh and work with the Intel processors up to 10 MHz. Logic is also included to insert WAIT states, if wanted, into the microprocessor READ or WRITE cycles when using fast CPU's.

## Features

- Provides a 3-chip solution for the 8086 family, dynamic RAM interface (DP8409A or DP8419, DP84432, and clock divider)
- Works with all 8086 family speed versions up to 10 MHz
- Operation of 8086, 8088, 80186, 80188 at 10 MHz with no WAIT states
- Controls DP8409A or DP8419 Mode 5 accesses, hidden refreshes and Mode 1 Forced Refreshes automatically
- Inserts WAIT states in READ or WRITE cycles automatically depending on whether WAITRD or WAITWR are low, or if $\overline{CS}$ becomes active during a forced Refresh cycle
- Uses a standard National Semiconductor PAL part (DMPAL16R4A)
- The PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new very high speed PALs ("B" PAL parts)

## Connection Diagram




TL/F/8399–1

**Order Number DP84432N or DP84432J**
**See NS Package Number N20A or J20A**

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | Operating | Programming |
|---|---|---|
| Supply Voltage, $V_{CC}$ | 7V | 12V |
| Input Voltage | 5.5V | 12V |
| Off-State Output Voltage | 5.5V | 12V |
| Storage Temperature Range | −65°C to +150°C | |

## DP84432 Recommended Operating Conditions

| Symbol | Parameter | | Commercial | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $t_w$ | Width of Clock | Low | 15 | 10 | | ns |
| | | High | 15 | 10 | | |
| $t_{su}$ | Setup Time from Input or Feedback to Clock | | 25 | 16 | | ns |
| $t_h$ | Hold Time | | 0 | −10 | | ns |
| $T_A$ | Operating Free-Air Temperature | | 0 | 25 | 75 | °C |
| $T_C$ | Operating Case Temperature | | | | | °C |

## Electrical Characteristics Over Recommended Operating Temperature Range

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | | 0.8 | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min., $I_I$ = −18 mA | | | −0.8 | −1.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min.<br>$V_{IL}$ = 0.8V<br>$V_{IH}$ = 2V | $I_{OH}$ = −3.2 mA COM | 2.4 | 2.8 | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min.<br>$V_{IL}$ = 0.8V<br>$V_{IH}$ = 2V | $I_{OL}$ = −24 mA COM | | 0.3 | 0.5 | V |
| $I_{OZH}$ | Off-State Output Current | $V_{CC}$ = Max<br>$V_{IL}$ = 0.8V<br>$V_{IH}$ = 2V | $V_O$ = 2.4V | | | 100 | μA |
| $I_{OZL}$ | | | $V_O$ = 0.4V | | | −100 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max., $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max., $V_I$ = 2.4V | | | | 25 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max., $V_I$ = 0.4V | | | −0.02 | −0.25 | mA |
| $I_{OS}$ | Output Short-Circuit Current | $V_{CC}$ = 5V $V_O$ = 0V | | −30 | −70 | −130 | mA |
| $I_{CC}$ | Supply Current† | $V_{CC}$ = Max. | | | 120 | 180 | mA |

## Switching Characteristics Over Recommended Ranges of Temperature and $V_{CC}$

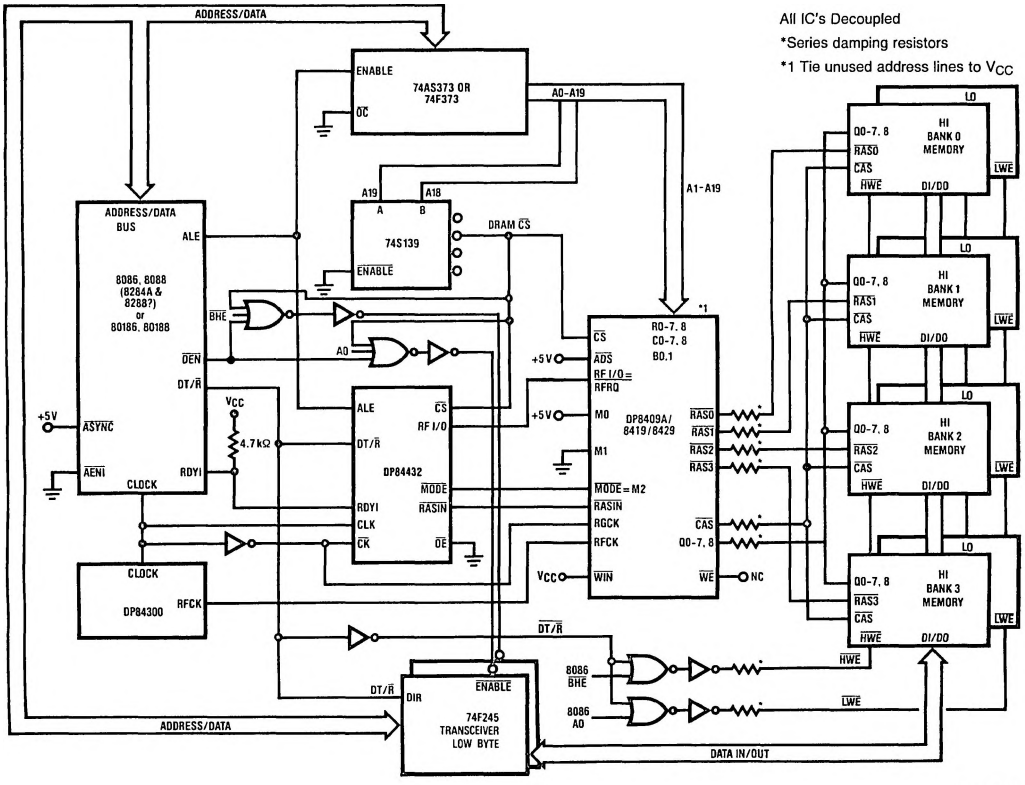
$V_{CC}$ = 5V ± 10%. Commercial: $T_A$ = 0 to 75°C, $V_{CC}$ = 5V ± 5%

| Symbol | Parameter | Test Conditions R1,R2 | Commercial | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Output | CL = 50 pF | | 15 | 25 | ns |
| $t_{CLK}$ | Clock to Output or Feedback | | | 10 | 15 | ns |
| $t_{PZX}$ | Pin 11 to Output Enable | | | 10 | 20 | ns |
| $t_{PXZ}$ | Pin 11 to Output Disable | $C_L$ = 5 pF | | 11 | 20 | ns |
| $t_{PZX}$ | Input to Output Enable | $C_L$ = 50 pF | | 10 | 25 | ns |
| $t_{PXZ}$ | Input to Output Disable | $C_L$ = 5 pF | | 13 | 25 | ns |
| $f_{MAX}$ | Maximum Frequency | | 25 | 30 | | ns |

$V_{CC}$ = Max. at minimum temperature.

## Block Diagram

**8086 System Block Diagram**




TL/F/8399–2

## Mnemonic Description

**INPUT SIGNALS**

1) "$\overline{\text{CLOCK}}$" Inverted clock from 8284A or 8288. "$\overline{\text{CLOCK}}$" should be delayed from CLOCK (pin 5).

2) "$\overline{\text{CS}}$" From decoder chip (chip select) (active low).

3) "ALE" From 8086 (active high).

4) "RFI/O" $\overline{\text{RFRQ}}$ (refresh request) in mode 5. From 8409A, an active low signal.

5) "CLOCK" The non-inverted clock directly from the 8284A. This signal should be unbuffered to this input so as not to incur any extra delay in the $\overline{\text{RASIN}}$ generation time.

6) "$\overline{\text{DELAYREAD}}$" This input signal allows the user to delay when the $\overline{\text{RASIN}}$ signal becomes valid to the DP8409A during a READ cycle of the 8086. This input should be low when using the DP8409A unless an external delay line is used to guarantee a 30 ns $\overline{\text{CS}}$ to $\overline{\text{RASIN}}$ delay (for DP8409A or 15 ns for DP8419) or if the user can afford to disable the hidden refresh by permanently tying $\overline{\text{CS}}$ low on the DP8409A.

7) "$\overline{\text{WAITWRITE}}$" This signal is used to delay when $\overline{\text{RASIN}}$ becomes valid during an 8086 WRITE cycle and also adds a WAIT state into a $\overline{\text{CS}}$ WRITE access cycle. One may want to delay when $\overline{\text{RASIN}}$ becomes valid during a WRITE cycle when generating a parity bit for each byte. This would allow time to generate parity and be assured that the data and parity bit were both written to memory.

8) "DT/$\overline{\text{R}}$" or "$\overline{\text{S1}}$" Used to differentiate between READ and WRITE cycles, and to allow $\overline{\text{CS}}$ READ cycles to start early. If the system is not a minimum mode 8086 or 8088 system then the status signal "$\overline{\text{S1}}$" should be used instead of "DT/R" so that the DP84432 knows immediately whether the CPU is doing a READ or a WRITE access cycle.

## Mnemonic Description (Continued)

9) "WAITREAD" Used to insert 1 wait state into the 8086 READ bus cycle. The wait state following bus cycle "T3" allows the use of memory with longer access times ($t_{CAC}$). An active low signal.

10) "OE" This input enables the outputs of the "D-Flip Flop" outputs of the PAL.

**OUTPUTS SIGNALS**

1) "MODE" This pin goes to M2 on the DP8409A to change from mode 5 to mode 1 (only used for forced refresh).

2) "2DLY" Delay used internal to the PAL.

3) "3DLY" Delay used internal to the PAL.

4) "4DLY" Delay used internal to the PAL.

5) "RASIN" To the 8409A (creates RAS's).

6) "RDY1" To the 8284A or 8288 to insert wait states into the 8086 bus cycles (active low).

7) "INCYCLE REFRESH" This signal is used in the *Figure 1* PAL to detect that an access cycle was started during a DRAM refresh cycle. This allows the PAL to determine, later in the cycle, whether to restart the "INCYCLE" signal or not. If the CPU is not accessing the DRAM, as determined by "CS" being low, then "INCYCLE" is not restarted.

8) "INCYCLE" This signal goes active from the CPU ALE signal. This signal indicates that the processor is doing an access somewhere in the system. This signal stays low for several T states of the access cycle.

## Functional Description

The following description applies to both the DP8409A and the DP8419 dynamic RAM controllers.

A memory cycle starts when chip select (CS) and address latch enable (ALE) are true. RASIN is supplied from the DP84432 to the DP8409A dynamic RAM controller, which then supplies a RAS signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8409A switches the address outputs to the column address. The DP8409A then supplies the required CAS signal to the DRAM. In order to do byte operations it is suggested that the user provide external logic, as shown in the system block diagram, to produce a HIGH WRITE ENABLE or a LOW WRITE ENABLE. To differentiate between a READ and a WRITE, the DT/R (or status signal "S1" in a maximum mode 8086 or 8088 system or in a 80186, 8188 system) signal from the CPU is inverted and also supplied to the external WRITE ENABLE logic.

A refresh cycle is started by one of two conditions. The refresh cycle caused by the first condition is called a hidden refresh. This occurs when refresh clock (RFCK) is high, CS is not true, and RASIN goes true. Here the CPU is accessing something else in the system and the DRAM can be refreshed at that time, thereby being transparent to the CPU. The second type of refresh is called forced refresh. This occurs if no hidden refresh was performed while RFCK was high. When RFCK transitions low a refresh request (RFRQ) is generated. If there is not a DRAM access in progress the DP84432 will force a refresh by putting the DP8409A into mode 1 (automatic forced refresh mode). If the CPU tries to access the DRAM during a forced refresh cycle WAIT states will be inserted into its cycles until the forced refresh is over and the DRAM RAS precharge time has been met. Then the pending DRAM access will be allowed to take place.

The DP84432 also allows forced refreshes to take place during long accesses of other devices. For instance, if EEPROM takes several microseconds to write to, the DRAM will still be refreshed while that access is in progress.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories or allow time to generate parity. This is accomplished by inserting a WAIT state into the processor access cycle. The DP84432 can insert WAIT states into either READ or WRITE cycles, or both. The extra WAIT state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

**SYSTEM INTERFACE DESCRIPTION**

The 80186 or 80188 will be able to use the DP84432 but it will be necessary to invert "ALE" of the 80186 or 80188 and logically NOR it with the "CLOCK" signal. This fix makes the 80186 or 80188 "ALE" signal appear to be similar to the 8086 or 8088 "ALE" signal. The 8088 will be able to use this PAL, but the 8088 will not need the logic necessary to produce LWE, HWE. The 80286 can not use this PAL because it's WAIT state logic is different. (See DP84532 data sheet).

The DP84432 differentiates between READ and WRITE cycles, allowing the RASIN signal to start earlier during a READ cycle compared to a WRITE cycle.

RASIN during a READ cycle can start during T1 or T2 of a processor cycle depending on whether the DELAYREAD input is set low or high. If DELAYREAD is false the user will need to use an external delay line to guarantee that CS will be valid a minimum of 30 ns before RASIN becomes true. If the user is willing to give up hidden refreshes (CS tied permanently low on DP8409A) he must only guarantee that the addresses are valid at the inputs of the DP8409A by a minimum of 10 ns before RASIN becomes valid.

This section of the data sheet goes through the calculation of the "tRAC" (RAS access time) and "tCAC" (CAS access time) required by the DRAM for the iAPX 86/88/186/188 family CPUs to operate at a particular clock frequency without introducing wait states into the processor access cycles. Both "tRAC" and "tCAC" must be considered in determining what speed DRAM can be used in a particular system design. The DRAM chosen must meet both the "tRAC" and "tCAC" parameters calculated. In order to determine the "tRAC" and "tCAC" needed the DP8419 and fast PALs ("B" type PALs) timing parameters were used. If the user is using the DP8408A/09A or a slower PAL device he should substitute their respective delays into the equations below.

Most all of the calculations contained in this note use "RAHS" = 1 (15 ns guaranteed minimum row address hold time). Calculations only used "RAHS" = 0 (25 ns guaranteed minimum row address hold time) when the calculated access time from RAS exceeded 200 ns. This is because DRAMs can be found with row access times up to 150 ns that require only 15 ns row address hold times.

## Functional Description (Continued)

**EXAMPLE DRAM TIMING CALCULATIONS**

**A) iAPX 86/88 8 MHz, No WAIT states, "/DLYRD" = low**

#1) $\overline{RASIN}$ low = 1 system clock period + 15 ns ("B" PAL combinational output delay) = 125 + 15 = 140 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F245 transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"$t_{RAC}$" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 125 + 125 + 125 − 140 − 20 − 7 − 20 = 188 ns

"$t_{CAC}$" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 140 − 77 − 7 − 20 = 131 ns

Therefore the DRAM chosen should have a "$t_{RAC}$" less then or equal to 188 ns and a "$t_{CAC}$" less then or equal to 131 ns. Standard 150 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately two clock periods = 125 + 125 = 250 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately two clock periods plus 50 ns (minimum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 125 + 50 = 300 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns ($t_{RPDL}$-$t_{RPDH}$ for the DP8409-2) = 125 + 125 − 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 125 − 70 = 180 ns.

The above times are assuming the use of the DP8409-2 and a fast ("A" part) PAL. The smallest pulse widths are generated during WRITE cycles since $\overline{RASIN}$ during WRITE cycles starts later than $\overline{RASIN}$ during READ cycles.

**B) 80186, 8 MHz, "$\overline{DLYRD}$" = HIGH, No Hidden Refresh ($\overline{CS}$ = Low), No Wait States**

Minimum $\overline{RASIN}$ = 55 ns (min clk low) + 1 ns (min PAL delay) = 68 ns

Maximum Address Valid = 44 ns (ADD valid max) + 8 ns (74F373) = 52 ns

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 70 + 15 = 85 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 97 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 Transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"$t_{RAC}$" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 125 + 125 + 125 − 85 − 20 − 7 − 20 = 243 ns

"$t_{CAC}$" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 85 − 94 − 7 − 20 = 169 ns

Therefore the DRAM chosen should have a "$t_{RAC}$" less then or equal to 243 ns and a "$t_{CAC}$" less then or equal to 169 ns. Standard 200 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one clock period + 55 ns (minimum clock low) − 15 ns (maximum DP84432 clocked output delay for ending $\overline{RASIN}$) = 125 + 55 − 15 = 165 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one clock period + 55 ns (minimum clock low) − 15 ns (maximum clocked output delay for ending $\overline{RASIN}$) + 35 ns (minimum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 55 − 15 + 35 = 200 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns ($t_{RPDL}$-$t_{RPDH}$ for the DP8409-2) = 125 + 125 − 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 125 − 70 = 180 ns.

**C) 8086, 8 MHz, $\overline{CS}$ Tied Low (no hidden refresh), $\overline{DLYRD}$ = HIGH, No Delay Line Needed, No Wait States**

Minimum $\overline{RASIN}$ = 69 ns (min clk low) + 13 ns (min PAL delay) = 82 ns

Maximum Address Valid = 60 ns (ADD valid max) + 8 ns (74F373) = 68 ns

The address must be valid a minimum of 10 ns before $\overline{RASIN}$ goes valid at the inputs of the DP8409A or DP8419, which it will be given the ICs used in this example.

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 82 + 15 = 97 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 97 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 94 ns maximum (using 25 ns minimum row address hold time)

#4) 74F245 Transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 20 ns minimum

"$t_{RAC}$" = T1 + T2 + T3 − #1 − #2 − #4 − #5
= 125 + 125 + 125 − 97 − 20 − 7 − 20 = 231 ns

"$t_{CAC}$" = T1 + T2 + T3 − #1 − #3 − #4 − #5
= 125 + 125 + 125 − 97 − 94 − 7 − 20 = 157 ns

Therefore the DRAM chosen should have a "$t_{RAC}$" less then or equal to 231 ns and a "$t_{CAC}$" less then or equal to 157 ns. Standard 200 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) + 15 ns (maximum DP84432 clocked output delay for ending $\overline{RASIN}$) = 125 + 69 − 15 = 179 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) − 15 ns (maximum clocked output delay for ending $\overline{RASIN}$) + 35 ns (minimum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 69 − 15 + 35 = 214 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns ($t_{RPDL}$-$t_{RPDH}$ for the DP8409-2) = 125 + 125 − 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 125 − 70 = 180 ns.

## Functional Description (Continued)

**D) 8086, 10 MHz, $\overline{CS}$ Tied Low (no hidden refresh), $\overline{DLYRD}$ = HIGH, No Delay Line Needed, No Wait States**

MINIMUM $\overline{RASIN}$ = 52 ns (min clk low) + 13 ns (min PAL delay) = 65 ns

MAXIMUM ADDRESS VALID = 50 ns (ADD valid max) + 8 ns (74F373) = 58 ns

The address must be valid a minimum of 10 ns before $\overline{RASIN}$ goes valid at the inputs of the DP8409A or DP8419. As an example use two 74ALS04 inverters to guarantee a minimum delay of 4 ns, therefore MINIMUM $\overline{RASIN}$ = 69 ns

#1) $\overline{RASIN}$ low = Maximum clock high + 15 ns ("B" PAL combinational output delay) = 61 + 15 = 76 ns maximum

#2) $\overline{RASIN}$ to $\overline{RAS}$ low = 20 ns maximum

#3) $\overline{RASIN}$ to $\overline{CAS}$ low = 80 ns (DP8419 $\overline{RASIN}$ − $\overline{CAS}$ low) − 3 ns (load of 72 DRAMs instead of 88 DRAMs speced in data sheet) = 77 ns maximum (using 15 ns minimum row address hold time)

#4) 74F245 Transceiver delay = 7 ns maximum

#5) CPU data setup time to "T4" = 5 ns minimum

"$t_{RAC}$" = T1 + T2 + T3 − #1 − #2 − #4 − #5

= 100 + 100 + 100 − 76 − 20 − 7 − 5 = 192 ns

"$t_{CAC}$" = T1 + T2 + T3 − #1 − #3 − #4 − #5

= 100 + 100 + 100 − 76 − 77 − 7 − 5 = 135 ns

Therefore the DRAM chosen should have a "$t_{RAC}$" less then or equal to 192 ns and a "$t_{CAC}$" less then or equal to 135 ns. Standard 150 ns DRAMs meet this criteria.

The minimum $\overline{RAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) − 15 ns (maximum DP84432 clocked output delay for ending $\overline{RASIN}$) = 125 + 69 − 15 = 179 ns.

The minimum $\overline{CAS}$ PRECHARGE TIME will be approximately one clock period + 69 ns (minimum clock low) − 15 ns (maximum clocked output delay for ending $\overline{RASIN}$) + 35 ns (minimum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 69 − 15 + 35 = 214 ns.

The minimum $\overline{RAS}$ PULSE WIDTH will be approximately two clock periods − 5 ns ($t_{RPDL}$-$t_{RPDH}$ for the DP8409-2) = 125 + 125 − 5 = 245 ns.

The minimum $\overline{CAS}$ PULSE WIDTH will be approximately two clock periods − 70 ns (maximum $t_{RICL}$-$t_{RICH}$ for the DP8409-2) = 125 + 125 − 70 = 180 ns.

**SUGGESTIONS**

It is suggested that the DP8409A is to be used up to 8 MHz. Above 8 MHz one should use the DP8409-2 or the DP8419. Also fast PALs ("A" parts) should be used at 8 MHz and above. If very fast PALs are used ("B" parts) the access will be 10 ns faster than calculated in the above sections.

These suggestions occur because of DRAM parameters that must be met, such as:

1) $\overline{CAS}$ ACCESS TIME—time from $\overline{CAS}$ valid until data is available at the DRAM outputs.

2) $\overline{RAS}$ PRECHARGE TIME—minimum amount of time from $\overline{RAS}$ high until $\overline{RAS}$ transitions low again.

3) $\overline{CAS}$ PRECHARGE TIME—minimum amount of time from $\overline{CAS}$ high until $\overline{CAS}$ transitions low again.

4) $\overline{RAS}$ PULSE WIDTH—minimum $\overline{RAS}$ valid time during an access, this usually occurs during a WRITE operation since $\overline{RASIN}$ is generated later then in a READ operation.

5) $\overline{CAS}$ PULSE WIDTH—minimum $\overline{CAS}$ valid time during an access.

6) DATA IN SETUP TIME—the data, during a DRAM WRITE access cycle, must be valid at the DRAM inputs when WRITE ENABLE or $\overline{CAS}$ transitions low, whichever occurrs last.

For instance, during a WRITE operation, one does not want $\overline{CAS}$ to go valid until the data to be written is setup at the inputs to the dynamic RAM. Therefore an 8086 running at 5 MHz should use a DP8409A and a slower DP84432 PAL.

EXAMPLE: 8086, 5 MHz, DP8409A, DP84432 (fast PAL "A" part)

MINIMUM $\overline{RASIN}$ = 3 ns (min clk inversion) + 7 ns (min fast PAL clocked output) + 13 ns (min combinational fast PAL output) = 23 ns into the T2 CPU cycle.

MINIMUM $\overline{CAS}$ = MINIMUM $\overline{RASIN}$ + MINIMUM $\overline{RASIN}$ TO $\overline{CAS}$ TIME = 23 + 95 = 118 ns

MINIMUM DATA VALID during an 8086 WRITE at 5 MHz = 110 ns

MINIMUM DATA VALID at DRAM input = MINIMUM DATA VALID + MINIMUM TRANSCEIVER DELAY (74F245) = 110 + 7 = 117 ns

Therefore, worst case, the data could be valid 1 ns before $\overline{CAS}$ becomes valid at the DRAM inputs. Most DRAMs specify 0 ns setup time so this is OK, but if the DP8409A is driving less then the full load specified in the data sheet $\overline{CAS}$ could become valid before the data was available at the DRAM inputs. Therefore the user may want to use a slower PAL or adjust the PAL equations to start the WRITE later in the access cycle. For example, the second equation in the $\overline{RASIN}$ term could be adjusted as follows to accomplish a later $\overline{RASIN}$ during WRITE cycles:

change "$\overline{CS}$•$\overline{INCY}$•$\overline{MODE}$•$\overline{2D}$•$\overline{WAITWR}$" to

"$\overline{CS}$•$\overline{INCY}$•$\overline{MODE}$•$\overline{2D}$•$\overline{WAITWR}$•$\overline{CLK}$"

At higher frequencies one generally wants to generate WRITE as the DP84432 does in order to guarantee that the $\overline{CAS}$ pulse width is great enough.

**INTERPRETING THE DP84432 PAL EQUATIONS**

The boolean equations for the DP84432 were written using the standard PALASM™ format. In other words the equation:

"IF (VCC) RASIN = INCY•$\overline{MODE}$•4D•$\overline{DT}$" will mean;

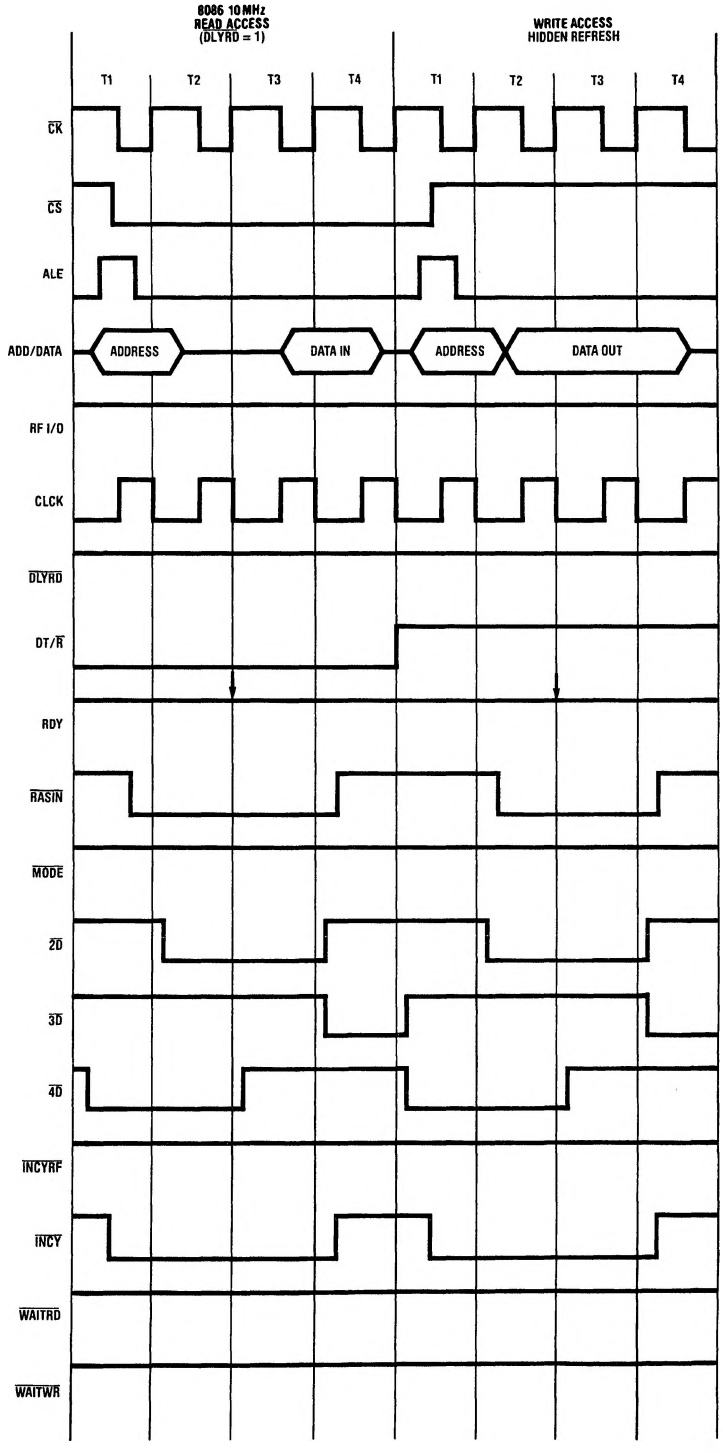
The output "$\overline{RASIN}$" (see pin list for DP84432) will be active low (inverted RASIN) when the output "$\overline{INCY}$" is low (making INCY high) AND the output "$\overline{MODE}$" is high AND the output "$\overline{4D}$" is low (making 4D high) AND the input DT/R is low (making $\overline{DT/R}$ high).

## PAL Boolean Equations

```
    PAL16R4A     ;FAST PAL
    NEW PAL FOR INTEL PROCESSORS 8086, 8088, 80186, 80188
    NATIONAL SEMICONDUCTOR (WORKS UP TO 10 MHz)

    /CK /CS RF10 ALE CLK /DLYRD /WAITWR DT /WAITRD GND /OE
    /INCY /INCYRF /4D /3D /2D /MODE /RASIN RDY VCC

IF (VCC) RASIN =
  INCY*/MODE*4D*/DT*/DLYRD*CLK+              ;Start RASIN, early READ
  CS*INCY*/MODE*2D*/WAITWR+                  ;Start RASIN, early WRITE
  CS*INCY*/INCYRF*/ALE*/MODE*3D*/DT*/CLK+    ;Start READ
  CS*INCY*/MODE*2D*DT*WAITWR*CLK+            ;Late WRITE
  /CS*INCY*/MODE*2D+                         ;Hidden RFSH
  RASIN*INCY*/ALE*/MODE*/3D*4D+              ;Continue RASIN
  RASIN*/MODE*2D                             ;Continue RASIN

IF (VCC) INCYRF = ALE*MODE+                  ;Start INCYCLE in REFRESH
                  INCYRF*MODE+               ;Continue INCY in REFRESH
                  INCYRF*4D*/CLK             ;Continue INCY in REFRESH

MODE := /RF10*/INCY*/2D+                     ;Forced RFSH at beginning
                                             ; of a cycle, during IDLE
        MODE*/3D+                            ; states, or during long
        MODE*/4D                             ; accesses of other devices

2D := MODE*/4D+
  INCY*/MODE*4D+
  CS*/DT*WAITRD*INCY*/MODE*2D*/3D*/4D+       ;Extend for "CS READ" cycle
  CS*DT*WAITWR*INCY*/MODE*2D*/3D*/4D         ;Extend for "CS WRITE" cycle

3D := 2D*/4D

4D := 3D+
      /INCY*/MODE+
      INCY*/MODE*/2D

IF (VCC) INCY = ALE*/MODE+                   ;Start INCY for access
         INCY*/INCYRF*/MODE*/3D*4D+          ;Continue INCY during access
         INCY*/MODE*2D+                      ;End INCY during access
         CS*INCYRF*/MODE*2D*/3D*4D+          ;Start INCY after REFRESH
         CS*INCY*/MODE*/3D*4D*/RDY           ;Continue INCY after REFRESH

IF (CS) /RDY = CS*INCYRF*/2D*/3D*4D+         ;Access at end of RFSH cycle
        CS*/RDY*/MODE*/2D*/3D*4D+            ;Continue RDY after RFSH
        CS*MODE+                             ;Continue RDY after RFSH
        CS*/DT*WAITRD*INCY*/MODE*2D*/3D*4D+  ;WAIT for "CS READ"
        CS*DT*WAITWR*INCY*/MODE*2D*/3D*4D    ;WAIT for "CS WRITE"
```

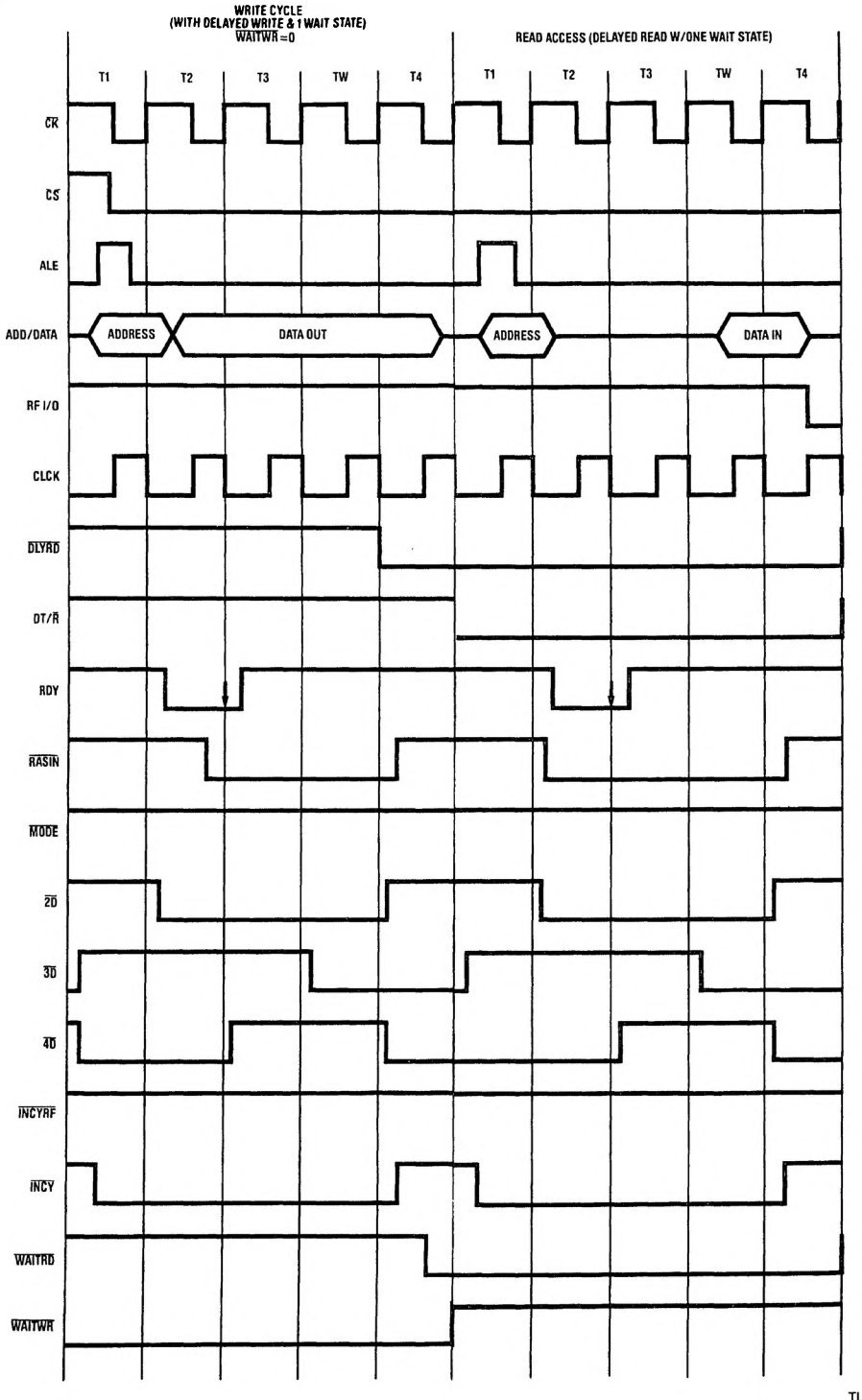
**FIGURE 1. Equations for the DP84432 Standard Interface PAL (Works in Minimum or Maximum Mode)**

## System Timing Diagrams



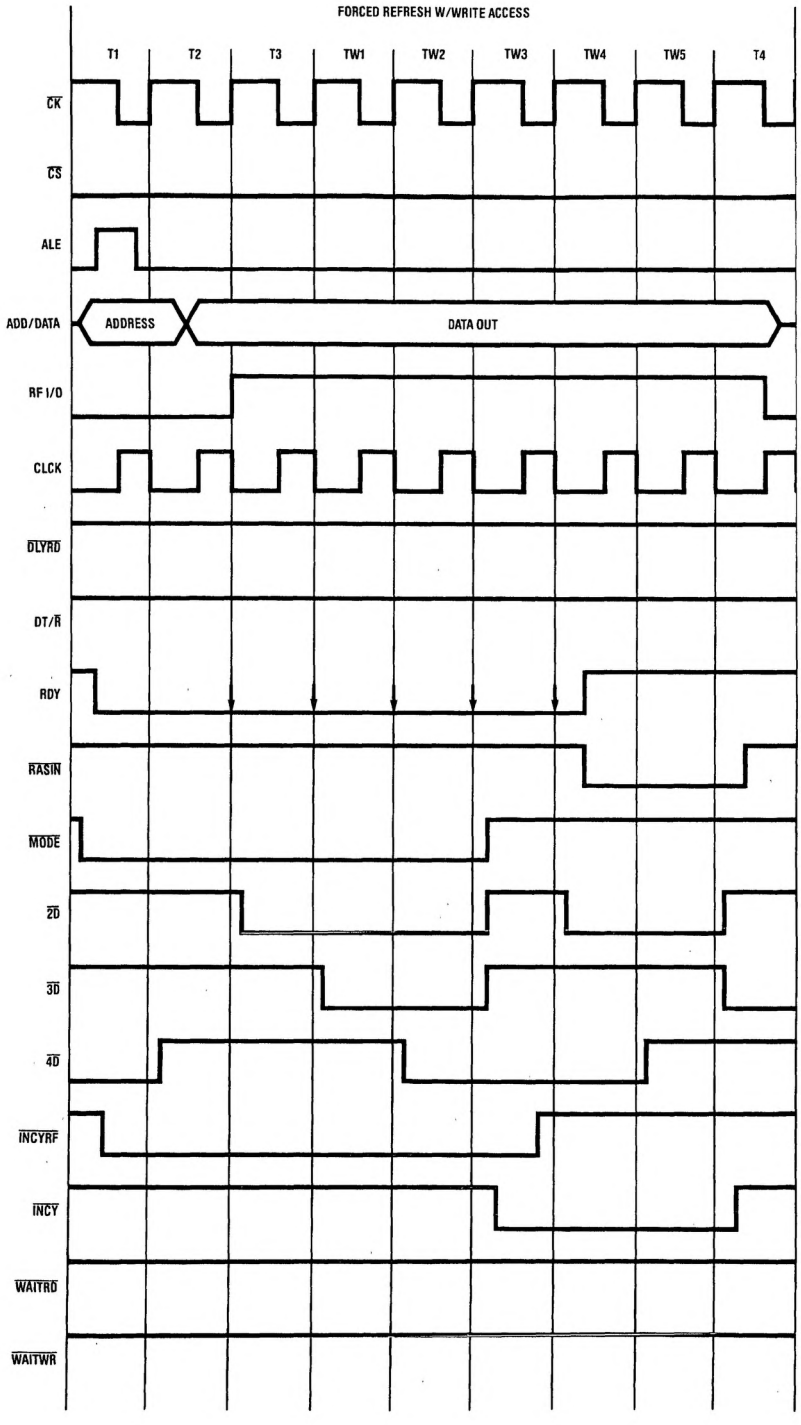

TL/F/8399–3

## System Timing Diagrams (Continued)



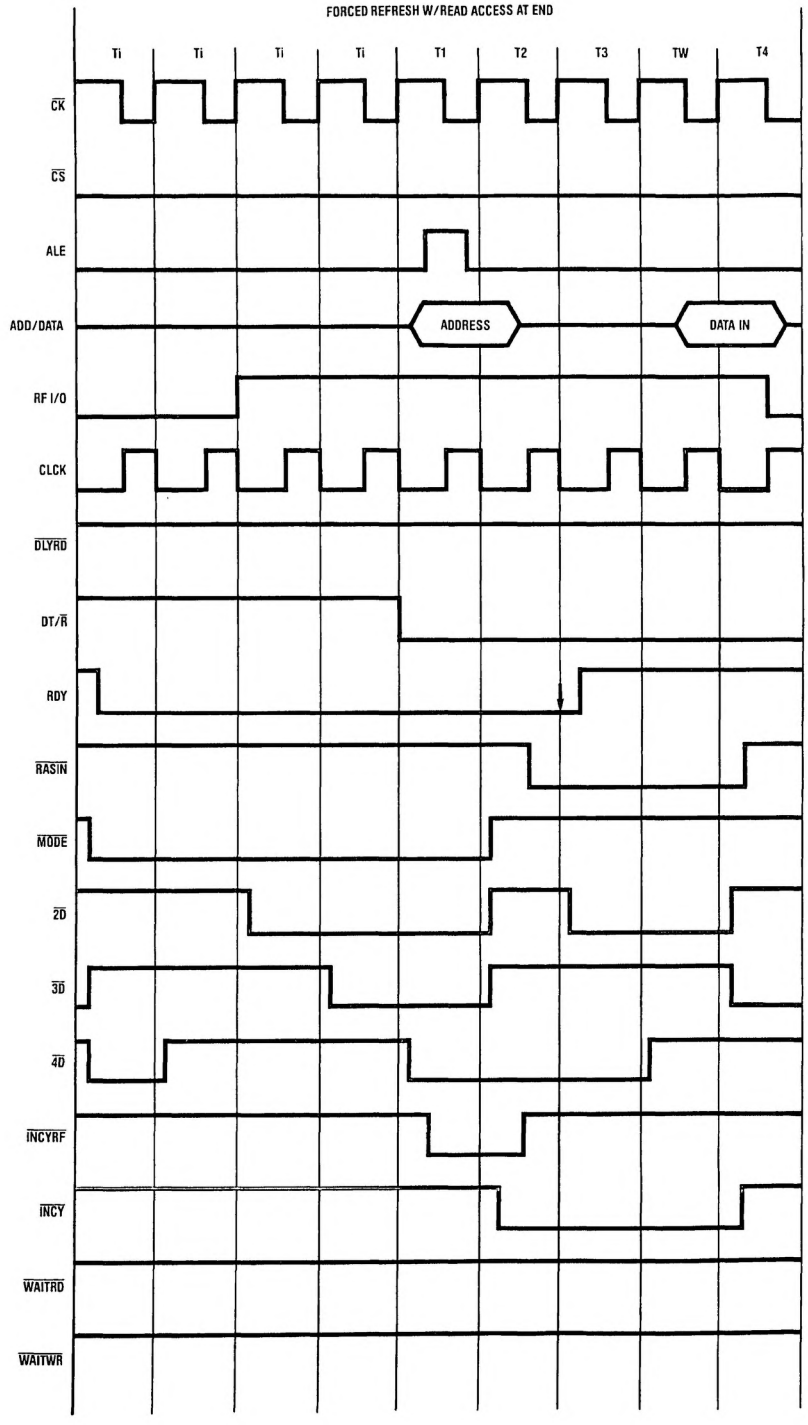

TL/F/8399–5

## System Timing Diagrams (Continued)



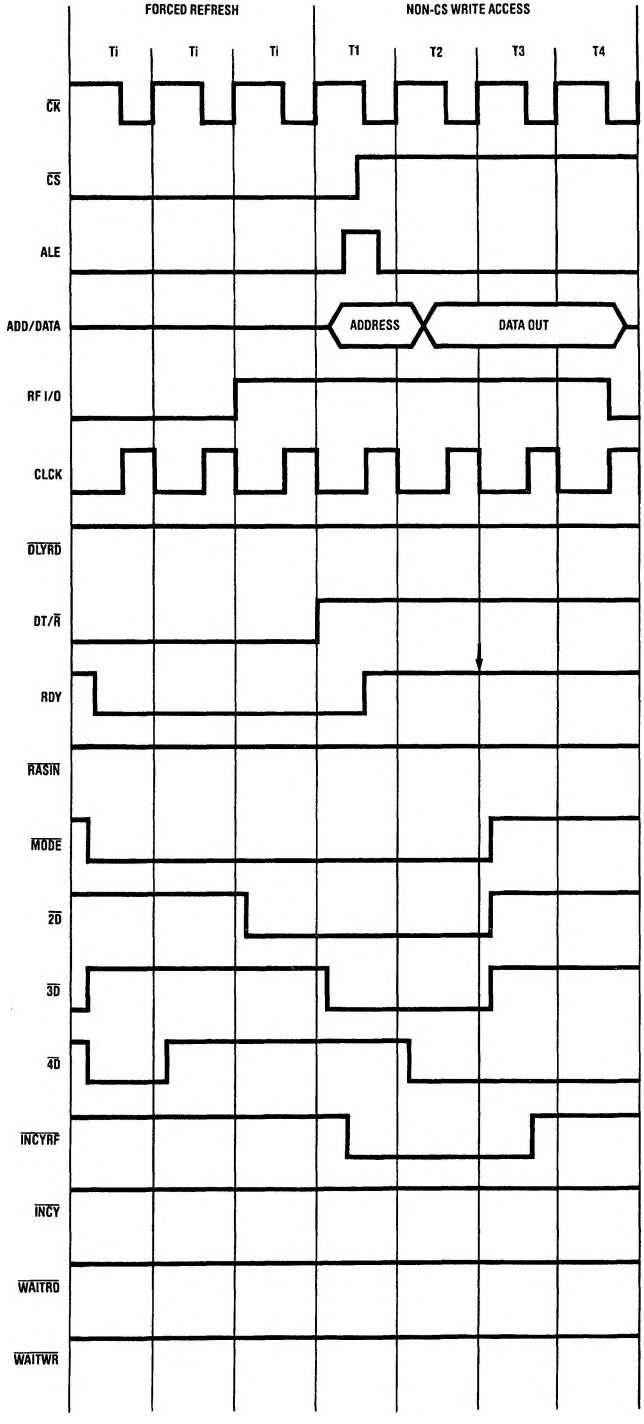

TL/F/8399–6

## System Timing Diagrams (Continued)



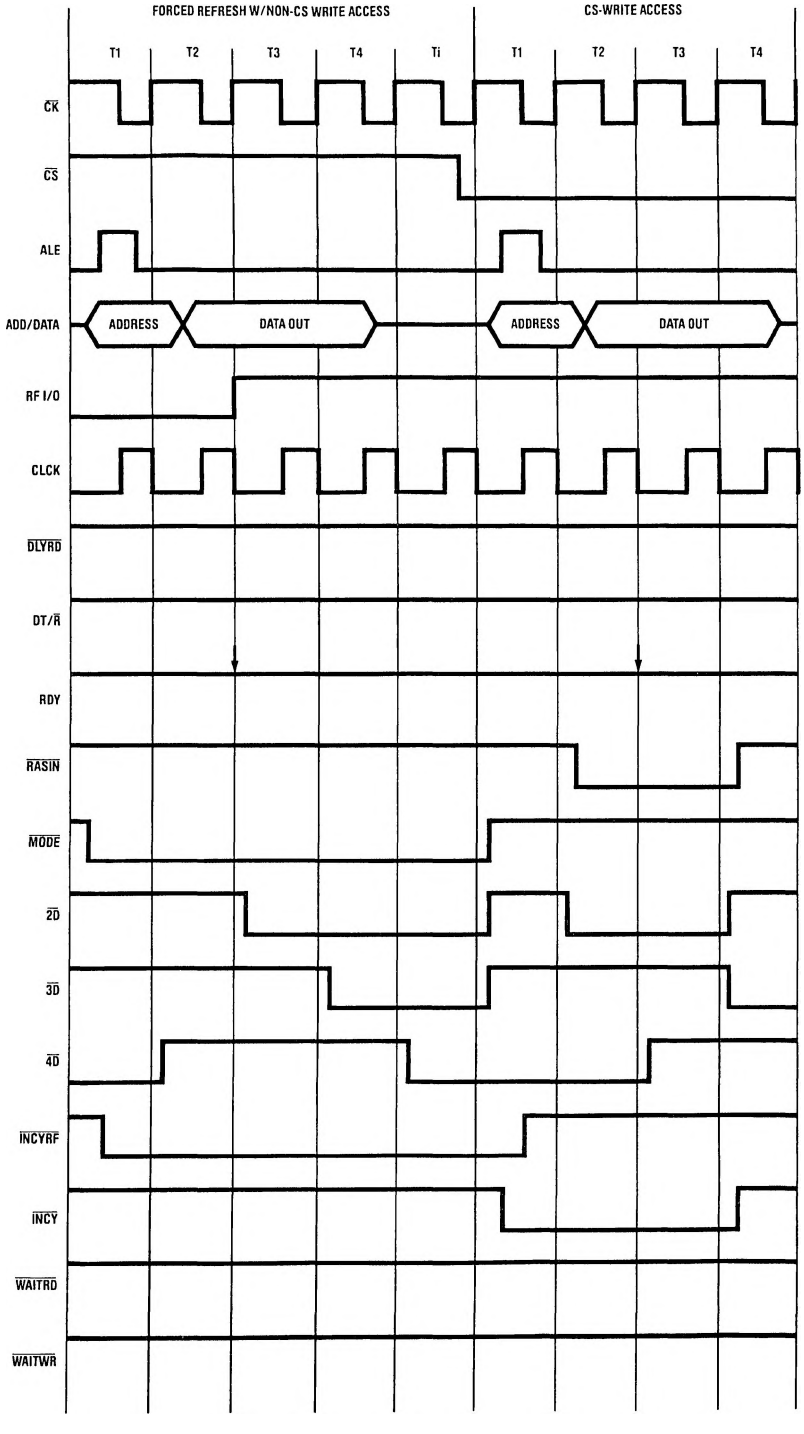

TL/F/8399–7

## System Timing Diagrams (Continued)




TL/F/8399–8

## System Timing Diagrams (Continued)




TL/F/8399–9