National Semiconductor

PRELIMINARY

DP84532 Dynamic RAM Controller Interface Circuit for the iAPX 286 CPU

General Description

This is a Programmable Array Logic (PAL®) device designed to allow an easy interface between the 80286 microprocessor and the National Semiconductor DP8419/29 or DP8409A dynamic memory controllers.

This PAL supplies all the control signals needed to perform memory read, write, and refresh operations up to a frequency of 16 MHz.

Features

- Provides a 3- or 4-chip solution for the 80286/DP8419 (or DP8409A/29) dynamic RAM interface (1 or 2 PALs, DP8419, and clock divider)
- Works with all speed versions of the 80286 up to 10 MHz
- Allows operation of 80286 at 8 MHz with no WAIT states with standard 120 ns 256k DRAMs
- Controls DP8409A/19 mode 5 accesses and mode 0 or 1 forced refreshes automatically
- Allows memory interleaving if desired
- CPU WAIT states are automatically inserted during contention between memory interleaving/DRAM accesses/DRAM refreshes
- Uses standard National Semiconductor PALs (i.e., DMPAL16R6A and DMPAL16R4A; the user may want to use faster versions of these PALs at higher CPU operating frequencies)
- The PAL programming equations are provided with comments for easy user modification to his specific requirements

Functional Description

The following description applies to both the DP8409A, DP8419 and DP8429.

A memory cycle starts when chip select ($\overline{CS}$) and the status ($\overline{S0}$*$\overline{S1}$) become true. $\overline{RASIN}$ is supplied from the PALs to the DP8419 DRAM controller, which then supplies $\overline{RAS}$ to the selected $\overline{RAS}$ bank. After the necessary row address hold time, the DP8419 switches the address outputs to the column address. The DP8419 then supplies the required $\overline{CAS}$ signal to the DRAM. In order to do byte operations a HIGH WRITE ENABLE and a LOW WRITE ENABLE are produced from PAL #2. All WRITE cycles are LATE WRITE cycles, to assure that valid data is written to the DRAMs. A $\overline{WRITE}$ strobe is produced by PAL #1 to assure enough $\overline{WIN}$ pulse width and to guarantee that valid data is latched into the DRAMs when writing to them. Memory buffers are used externally, to separate the data in from the data out of the DRAMs during LATE WRITE cycles.

Hidden REFRESH cycles are not allowed in this set of PALs because of the need for adequate $\overline{RAS}$ precharge times in all circumstances and the desire not to be inserting WAIT states into access cycles of other system elements.

These PALs perform automatic or externally controlled forced refreshes (mode 0 or 1). A refresh cycle occurs when the DP8419 input RFCK transitions low and the RFIO signal goes low requesting a refresh cycle. The PAL responds by pulling $\overline{RFSH}$ (M2, and/or MO depending on whether mode 1 or 0 is desired) low if there are no current DRAM accesses in progress. If a DRAM access is in progress the PAL waits until the current access is completed before performing the forced refresh cycle. If an access is requested during the forced refresh cycle WAIT states are automatically inserted into the access cycle until the refresh cycle is completed and adequate $\overline{RAS}$ precharge has been completed. The pending DRAM access cycle is then performed.

In order to guarantee adequate $\overline{RAS}$ precharge time during two consecutive accesses to the same DRAM bank, memory interleaving is performed by looking at the two lower address bits, A1 and A2. If the processor is sequentially accessing the DRAM, each $\overline{RAS}$ output will have plenty of precharge time. But if the system tries to access the same bank twice in a row the access will be delayed until adequate $\overline{RAS}$ precharge time has been met. During this time WAIT states will automatically be inserted into the pending access cycle.

The 8 MHz 80286 has two "T" states ("T_S" and "T_C"), it is possible for these PALs to get one clock phase out of sync with the 80286 CPU during access cycles pending while performing a refresh cycle. The two 8 MHz "T" states of the CPU contain four 16 MHz clock periods ("CLK" output of 82284 clock generator). This 2X clock is the clock the interface described herein uses. In other words, the PALs produce a $\overline{RASIN}$ output that is low for three 16 MHz clock periods for the 8 MHz 80286. Since WAIT states insert two 16 MHz clock periods and $\overline{RASIN}$ can start one clock period after $\overline{RFSH}$ transitions high, it is possible for $\overline{RASIN}$ to start one period early and go high one period before the access cycle ends, thus not holding the data valid during a READ access cycle long enough. To counteract this problem the term "ALE" is used in several of the PAL equations ($\overline{RASIN}$, $\overline{1DLY}$, and 2DLY) to sync the $\overline{RASIN}$ output to the access cycle. See the timing diagrams (*Figure 6*) and PAL equations for some further insight into the potential problems. This synchronization could also have been done externally by holding $\overline{CAS}$ low until either $\overline{MWTC}$ or $\overline{MRDC}$ go high, thus holding the READ data valid until the access cycle is over.

Two PALs were designed for this PAL interface. PAL #2 is used mostly for the support of memory interleaving. If one is not using memory interleaving (6 MHz or below) PAL #2 can be omitted and the PAL #1 "$\overline{PRECH}$" input can be tied high. The high and low memory write strobes can be produced externally.

Functional Description (Continued)

The PAL equations for this interface are written in the National Semiconductor PLAN™ format, which differs from the standard PALASM™ format.

EXAMPLE: PLAN FORMAT

```
/RASIN := RFSH*/2D*ALE
```

This translates as, "$\overline{\text{RASIN}}$" is low after the rising edge of the input clock given that "$\overline{\text{RFSH}}$" was high and "$\overline{\text{2D}}$" was low and "ALE" was high a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{2D}}$, and $\overline{\text{RFSH}}$ are outputs of the PAL and ALE is an input).

EXAMPLE: PALASM FORMAT

```
RASIN := /RFSH*2D*ALE
```

The above expression means the same as the PLAN format expression except it is written in PALASM format. In other words, "$\overline{\text{RASIN}}$" will go low after the rising edge of the clock given that "$\overline{\text{RFSH}}$" was high, "$\overline{\text{2D}}$" was low, and "ALE" was high a setup time before the clock transitions high (here $\overline{\text{RASIN}}$, $\overline{\text{2D}}$, and $\overline{\text{RFSH}}$ are outputs of the PAL and ALE is an input).

Depending on the specific type of PALs and logic used, the user can calculate the speed requirements for the DRAM at the specified processor frequency as follows:

CALCULATION OF DRAM "t_{RAC}" $\overline{\text{RAS}}$ ACCESS TIME AND "t_{CAC}" $\overline{\text{CAS}}$ ACCESS TIME REQUIRED FOR AN 8 MHz 80286, NO WAIT STATE, MICROPROCESSOR SYSTEM

#1) $\overline{\text{RASIN}}$ generation time = one period of the system clock + one 74AS244 gate delay (the system clock is inverted to the PALs) + one clocked output delay of the PAL generating the $\overline{\text{RASIN}}$ output (assume DMPAL16R6B) = 62.5 ns + 4.5 ns + 12 ns = 79 ns maximum

#2) $\overline{\text{RASIN}}$ to $\overline{\text{RAS}}$ out delay of the DP8419 = 20 ns maximum (used to determine "t_{RAC}")

#3) $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ out delay of the DP8419 DRAM controller driving a load of 4 banks of 256k DRAMs, each bank containing 18 (16 DRAMs plus byte parity) = 72 DRAMs

Since this is under the specified load in the data sheet (approximately 88 DRAMs) approximately 3 ns can be subtracted from the data sheet number, giving 80 ns − 3 ns = 77 ns maximum (used to determine "t_{CAC}").

#4) 74AS244 buffer delay = 7 ns maximum

#5) Data setup time required from the end of "T_C" phase 2 clock cycle = 10 ns minimum

A normal 8 MHz 80286 access cycle contains 4 clock periods (16 MHz) of 62.5 ns per period = 250 ns

The required DRAM "t_{RAC}" (row access time) can be calculated from 250 ns − #1 − #2 − #4 − #5 = 134 ns

The required DRAM "t_{CAC}" (column access time) can be calculated from 250 ns − #1 − #3 − #4 − #5 = 77 ns.

The DRAMs selected for this system must satisfy both the "t_{RAC}" and "t_{CAC}" requirements. Therefore the DRAMs must have a "t_{RAC}" (row access time) less than or equal to 134 ns and a "t_{CAC}" (column access time) less than or equal to 77 ns to be used in this system, under worst case conditions, for a no WAIT state, 8 MHz 80286 system. Common 120 ns 256k DRAMs meet this specification.

Other Options

In the system block diagram, buffers (74AS244s) were used to isolate the data in from the data out of the DRAM. This is needed because all WRITE accesses are late WRITEs (READ-MODIFY-WRITE cycles). In this system a HIGH and LOW WRITE enable were produced. The user could just as well have produced a HIGH and LOW CAS. In producing a HIGH and LOW CAS, the user would need the $\overline{\text{WRITE}}$ output of PAL #1 (to bring CAS low during a WRITE), A0 and $\overline{\text{BHE}}$ (for byte WRITEs), and the DT/$\overline{\text{R}}$ signal (for determining whether the access is a READ or WRITE access). Also, by generating a HIGH and LOW CAS, the system can use transceivers instead of buffers in the DRAM data path. The only problem with this approach is that $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ out may take a little longer since $\overline{\text{CAS}}$ goes through some external logic.

80286 PAL Inputs and Outputs

(Pin number of the PAL on the left)

PAL #1 INPUTS

1) "$\overline{\text{CLK}}$" This is the inverted system clock ("CLK") of the 82284 clock generator.

2) "$\overline{\text{CS}}$" This is the latched chip select (see system block diagram).

3) "$\overline{\text{RFRQ}}$" Refresh request from the DP8419.

4) "$\overline{\text{S0}}$" Status pin from the 80286.

5) "$\overline{\text{S1}}$" Status pin from the 80286.

6) "ALE" Address latch enable from 82288.

7) "NC1" No contact.

8) "$\overline{\text{PRECH}}$" This signal indicates that a back-to-back access cycle, to the same DRAM bank, is taking place. In this situation, the PAL controller will delay "$\overline{\text{RASIN}}$" until adequate $\overline{\text{RAS}}$ precharge time has been guaranteed, and also insert WAIT states into the present access cycle to accommodate the extra precharge time.

9) "NC2" No contact.

11) "$\overline{\text{OE}}$" This input enables the PAL outputs.

PAL #1 OUTPUTS

19) "$\overline{\text{CYREQ}}$" This signal indicates that an access was requested during a Refresh or during the precharge time of the previous access.

18) "$\overline{\text{RFREQ}}$" This output guarantees that the refresh request occurs within 15 ns after the system clock. This is necessary in order for the refresh/access arbitration to work correctly.

17) "$\overline{\text{RASIN}}$" This signal causes $\overline{\text{RAS}}$ (or $\overline{\text{RAS}}$s) to go low during a DRAM access or refresh.

16) "$\overline{\text{RFSH}}$" This signal initiates a DRAM Refresh.

15) "$\overline{\text{1DLY}}$" A delay that is used internally.

14) "$\overline{\text{2DLY}}$" A delay that is used internally.

13) "$\overline{\text{SYNRDY}}$" This output goes to the 82284 clock generator synchronous ready input. This output inserts WAIT states into DRAM access cycles during access/refresh/RAS precharge contention.

12) "$\overline{\text{WRITE}}$" This output produces a WRITE strobe for the DRAMs.

PAL #2 INPUTS

1) "ALE" This is the address latch enable input from the 82288.

2) "B0" This is the "A1" address bit from the 80286.

3) "B1" This is the "A2" address bit from the 80286.

4) "$\overline{\text{RASIN}}$" This signal causes $\overline{\text{RAS}}$ (or $\overline{\text{RAS}}$s) to go low during a DRAM access or refresh.

5) "$\overline{\text{1DLY}}$" This is a delay used internal to the PALs.)

6) "$\overline{\text{RFSH}}$" This signal initiates a DRAM Refresh.

7) "$\overline{\text{WRITE}}$" This output produces a WRITE strobe for the DRAMs.

8) "A0" This is the "A0" address bit from the 80286 and is used during byte read or byte write situations.

9) "$\overline{\text{BHE}}$" This is the high byte enable signal from the 80286 and is used during byte read or byte write situations.

11) "$\overline{\text{OE}}$" This input enables the PAL outputs.

PAL #2 OUTPUTS

19) "$\overline{\text{PRECH}}$" This signal indicates that a back-to-back access cycle, to the same DRAM bank, is taking place. In this situation, the PAL controller will delay "$\overline{\text{RASIN}}$" until adequate $\overline{\text{RAS}}$ precharge time has been guaranteed, and also insert WAIT states into the present access cycle to accommodate the extra precharge time.

18) "NC" No contact to this pin.

17) "$\overline{\text{PREV0}}$" Latches if the previous access was to Bank 0.

16) "$\overline{\text{PREV1}}$" Latches if the previous access was to Bank 1.

15) "$\overline{\text{PREV2}}$" Latches if the previous access was to Bank 2.

14) "$\overline{\text{PREV3}}$" Latches if the previous access was to Bank 3.

13) "$\overline{\text{WINLOW}}$" This is the low byte DRAM write input.

12) "$\overline{\text{WINHIGH}}$" This is the high byte DRAM write input.

Equations for PALs to Interface the DP8419 to the 80286

These PALs work up to 10 MHz and use mode 0 for doing externally controlled forced refreshes, guaranteeing 3 periods (of 2X clock from 82284) of RGCK RAS pulse width. This set of PALs will only work for the DP8419 since they use mode 0 forced refresh to reset the refresh request (RFIO) signal.

```
PAL #1
DMPAL16R6A
/CLK  /CS  /RFRQ  /S0  /S1  ALE  NC1  /PRECH  NC2  GND
/OE  /WRITE  /SYNRDY  /2DLY  /1DLY  /RFSH  /RASIN  /RFREQ  /CYREQ  VCC

IF (VCC) /CYREQ = /CS*/RFSH*S0*/S1                ;Read access during RFSH
           +/CS*/RFSH*/S0*S1                      ;Write access during RFSH
           +/CYREQ*/RFSH                          ;Hold "/CYREQ" during RFSH
           +/CYREQ*RASIN                          ;Hold "/CYREQ"
           +/CYREQ*1DLY                           ;Hold "/CYREQ"
           +/CS*RASIN*1DLY*/2DLY*S0*/S1           ;Precharge needed during access
           +/CS*RASIN*1DLY*/2DLY*/S0*S1           ;Precharge needed during access

IF (VCC) /WRITE = /S0*S1*/CS*ALE                  ;Write access
           +/WRITE*1DLY                           ;Hold "/WRITE" low
           +/WRITE*/RFSH                          ;Hold "/WRITE" low
           +/WRITE*/RASIN                         ;Hold "/WRITE" low

/RFREQ := /RFRQ

/RASIN := /RFSH*/1DLY*/ALE                        ;RFSH "/RASIN" except if "ALE"
  +/RFSH*/1DLY*/RASIN                             ;Keep "/RASIN" low during RFSH
  +RFSH*/S0*S1*PRECH*RFREQ*/ALE*/CS               ;WRITE access
  +RFSH*S0*/S1*PRECH*RFREQ*/ALE*/CS               ;READ access
  +/RASIN*RFSH*2DLY                               ;Hold "/RASIN" low
  +RFSH*/CYREQ*1DLY*2DLY*/ALE                     ;"/RASIN" after precharge delay
                                                  ;  or RFSH

/RFSH := /RFREQ*RASIN*1DLY*/2DLY                  ;Start RFSH after access
  +/RFREQ*RASIN*/1DLY*/2DLY                       ;Start RFSH after access
  +/RFREQ*RASIN*1DLY*2DLY*CYREQ                   ;Start RFSH after idle states
  +/RFSH*/1DLY                                    ;Hold RFSH low
  +/RFSH*/2DLY                                    ;Hold RFSH low
  +/RFSH*/RFREQ                                   ;Hold RFSH low

/1DLY := /RFSH*2DLY*/RFREQ                        ;"/1DLY" during RFSH
  +/RFSH*/RASIN*2DLY*/1DLY                        ;Hold "/1DLY" low
  +/RFSH*/RASIN*/1DLY*ALE                         ;Hold "/1DLY" low if "ALE"
  +RFSH*/RASIN                                    "/1DLY" during access

/2DLY := /RFSH*/RASIN                             ;"/2DLY" during RFSH
  +/RFSH*/2DLY*ALE                                ;Hold "/2DLY" low if "ALE"
  +RFSH*/RASIN*/1DLY                              ;"/2DLY" during access
  +RFSH*/1DLY*/2DLY*/PRECH*RASIN*RFREQ            ;Hold "/2DLY" low for precharge

/SYNRDY := /CS*/RASIN*1DLY*RFSH                   ;"/SYNRDY" during an access
```

Equations for PALs to Interface the DP8419 to the 80286 (Continued)

```
PAL #2

DMPAL16R4A
ALE  BO  B1  /RASIN  /1DLY  /RFSH  /WRITE  AO  /BHE  GND
/OE  /WINHIGH  /WINLOW  /PREV3  /PREV2  /PREV1  /PREV0  NC  /PRECH  VCC

IF (VCC) /PRECH = RFSH*/BO*/B1*/PREV0*RASIN*/1DLY  ;Need precharge during
          +RFSH*BO*/B1*/PREV1*RASIN*/1DLY           ;  present access if
          +RFSH*/BO*B1*/PREV2*RASIN*/1DLY           ;  previous access bank =
          +RFSH*BO*B1*/PREV3*RASIN*/1DLY            ;  present access bank

/PREV0 := /BO*/B1                              ;Previous access to bank 0

/PREV1 := BO*/B1                               ;Previous access to bank 1

/PREV2 := /BO*B1                               ;Previous access to bank 2

/PREV3 := BO*B1                                ;Previous access to bank 3

IF (VCC) /WINLOW = RFSH*/RASIN*/1DLY*/AO*/WRITE    ;"/WRITE" during access

IF (VCC) /WINHIGH = RFSH*/RASIN*/1DLY*/BHE*/WRITE  ;"/WRITE" during access
```

Equations for PALs to Interface the DP8409A or DP8419 to the 80286

These PALs work up to 10 MHz with the DP8419 and up to a frequency where the minimum RGCK high or low pulse width (of 82284 2X clock) is equal to or greater than 35 ns for the DP8409A. These PALs only guarantee 2 system clock periods of RAS low during refresh and 2 periods of RAS precharge time (of 82284 2X clock) between consecutive accesses to the same RAS bank.

```
PAL #1

DMPAL16R6A
/CLK  /CS  /RFRQ  /S0  /S1  ALE  NC1  /PRECH  NC2 GND
/OE  /WRITE  /SYNRDY  /2DLY  /1DLY  /RFSH  /RASIN  /RFREQ  /CYREQ  VCC

IF (VCC) /CYREQ = /CS*/RFSH*S0*/S1          ;Read access during RFSH
           +/CS*/RFSH*/S0*S1                ;Write access during RFSH
           +/CYREQ*/RFSH                    ;Hold "/CYREQ" during RFSH
           +/CYREQ*RASIN                    ;Hold "/CYREQ"
           +/CYREQ*1DLY                     ;Hold "/CYREQ"
           +/CS*RASIN*1DLY*/2DLY*S0*/S1     ;Precharge needed during access
           +/CS*RASIN*1DLY*/2DLY*/S0*S1     ;Precharge needed during access

IF (VCC) /WRITE = /S0*S1*/CS*ALE            ;Write access
           +/WRITE*1DLY                     ;Hold "/WRITE" low
           +/WRITE*/RFSH                    ;Hold "/WRITE" low
           +/WRITE*/RASIN                   ;Hold "/WRITE" low

/RFREQ := /RFRQ

/RASIN := RFSH*/S0*S1*PRECH*RFREQ*/ALE*/CS      ;WRITE access
     +RFSH*S0*/S1*PRECH*RFREQ*/ALE*/CS          ;READ access
     +/RASIN*RFSH*2DLY                          ;Hold "/RASIN" low
     +RFSH*/CYREQ*1DLY*2DLY*/ALE                ;"/RASIN" after precharge
                                                ;  delay or RFSH

   /RFSH := /RFREQ*RASIN*1DLY*/2DLY           ;Start RFSH after access
        +/RFREQ*RASIN*/1DLY*/2DLY             ;Start RFSH after access
        +/RFREQ*RASIN*1DLY*2DLY*CYREQ         ;Start RFSH after idle states
        +/RFSH*/1DLY                          ;Hold RFSH low
        +/RFSH*/2DLY                          ;Hold RFSH low
        +/RFSH*/RFRQ                          ;Hold RFSH low
```

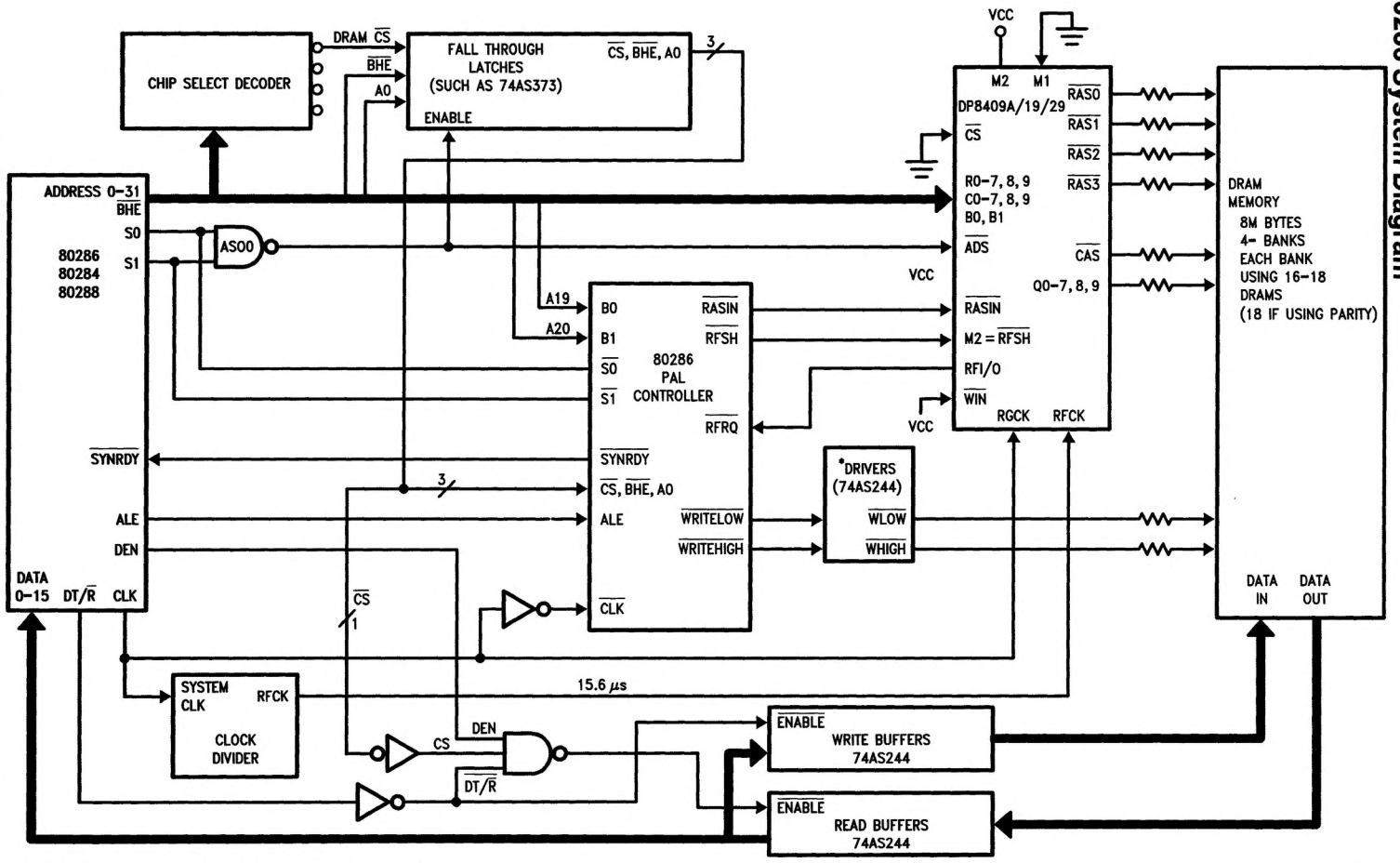
Equations for PALs to Interface the DP8409A or DP8419 to the 80286

(Continued)

```
/1DLY := /RFSH*2DLY*/RFRQ                    ;"/1DLY" during RFSH
      +/RFSH*/1DLY*2DLY                      ;Hold "/1DLY" low
      +RFSH*/RASIN                           ;"/1DLY" during access

/2DLY := /RFSH*/1DLY*/ALE                    ;"/2DLY" during RFSH
         +/RFSH*/2DLY*ALE                    ;Hold "/2DLY" low if "ALE"
         +RFSH*/RASIN*/1DLY                  ;"/2DLY" during access
         +RFSH*/1DLY*/2DLY*/PRECH*RASIN*RFREQ ;Hold "/2DLY" low for precharge

/SYNRDY := /CS*/RASIN*1DLY*RFSH              ;"/SYNRDY" during an access
```

If only 2 banks of DRAM were to be used the PAL interface would require only 1 PAL. The two inputs "$\overline{\text{PRECHOUT}}$ and NC" (pin #8 and #9) could be changed to "B0" and "$\overline{\text{PREVB0}}$" to allow interleaving of bank 0 and 1. "$\overline{\text{PREVB0}}$" could be produced externally using a "D" type flip-flop with "ALE" as its clock and "B0" as its input. The equations for "$\overline{\text{RASIN}}$" and "$\overline{\text{2DLY}}$" will have to be changed as follows:

```
/RASIN := /RFSH*/1DLY*/ALE                   ;RFSH "/RASIN"
  +/RFSH*/1DLY*/RASIN                        ;Hold "/RASIN" low in RFSH
  +RFSH*/S0*S1*B0*/PREVB0*RFREQ*/ALE*/CS     ;WRITE access
  +RFSH*/S0*S1*/B0*PREVB0*RFREQ*/ALE*/CS     ;WRITE access
  +RFSH*S0*/S1*B0*/PREVB0*RFREQ*/ALE*/CS     ;READ access
  +RFSH*S0*/S1*/B0*PREVB0*RFREQ*/ALE*/CS     ;READ access
  +/RASIN*RFSH*2DLY                          ;Hold ""/RASIN'' low
  +RFSH*/CYREQ*1DLY*2DLY*/ALE                ;"/RASIN" after precharge
                                             ;  delay or RFSH

/2DLY := /RFSH*/1DLY                         ;"/2DLY" during RFSH
   +/RFSH*/2DLY*ALE                          ;Hold "/2DLY" low if "ALE"
   +RFSH*/RASIN*/1DLY                        ;"/2DLY" during access
   +RFSH*/1DLY*/2DLY*/B0*/PREVB0*RASIN*RFREQ ;Hold "/2DLY" low for precharge
```



*Drivers may not be needed depending on the load being driven.

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FIGURE 1

80286 System Diagram (Continued)

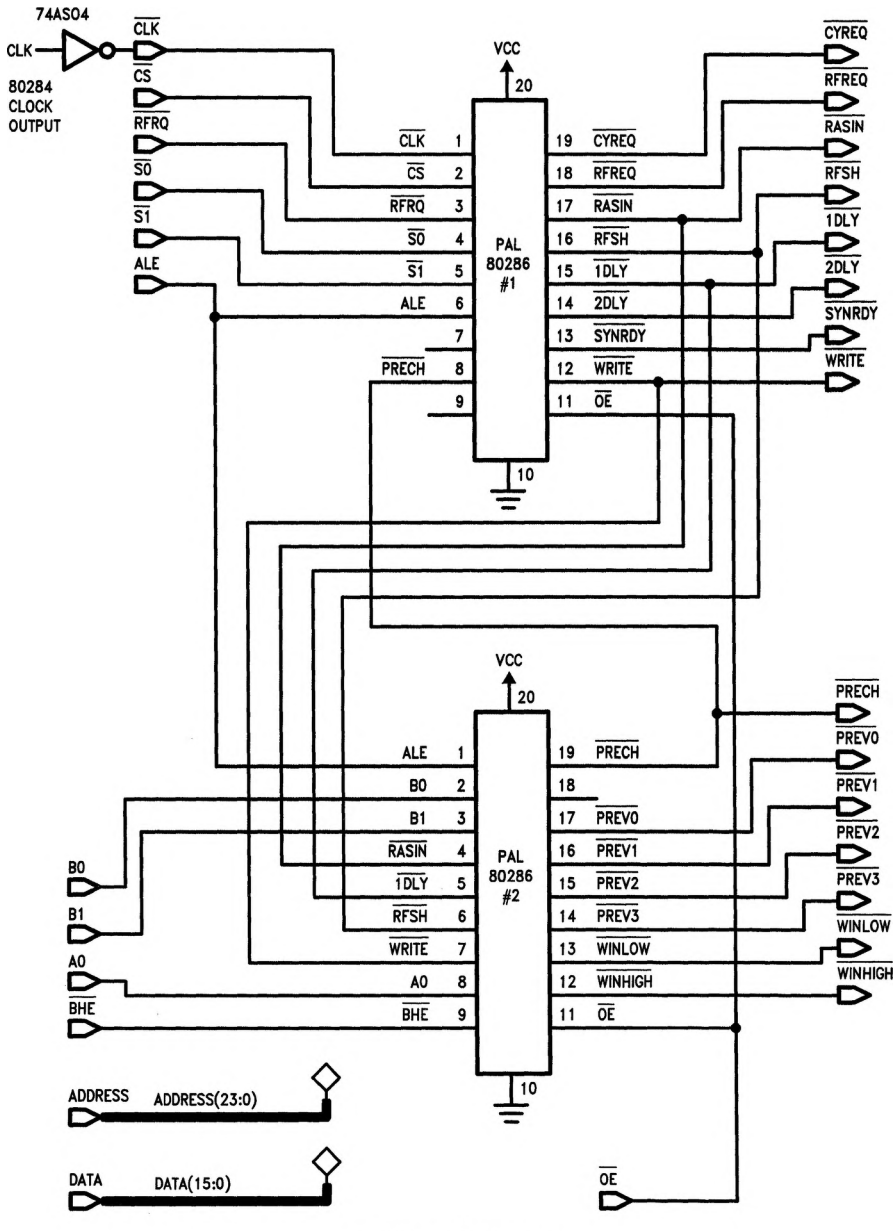

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FIGURE 2. 80286 PALs

System Timing Diagram

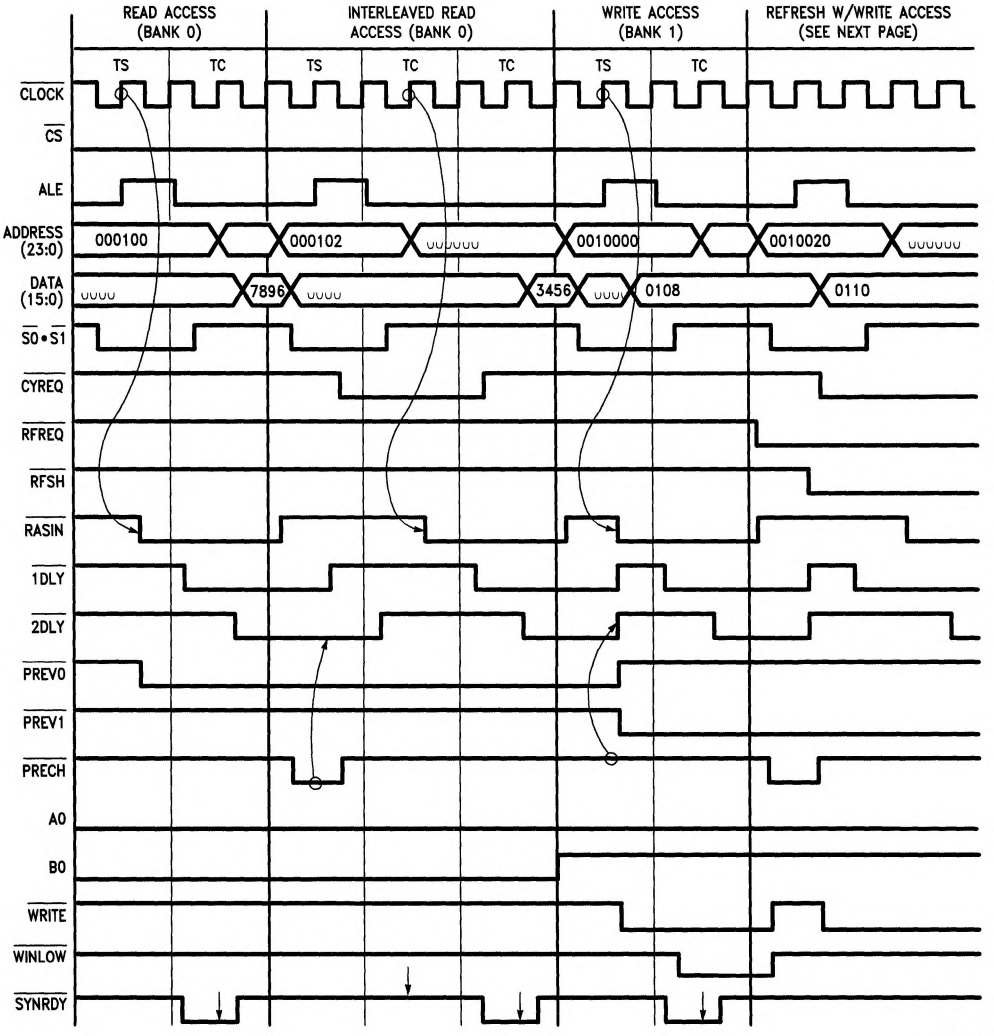

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FIGURE 3

System Timing Diagram (Continued)

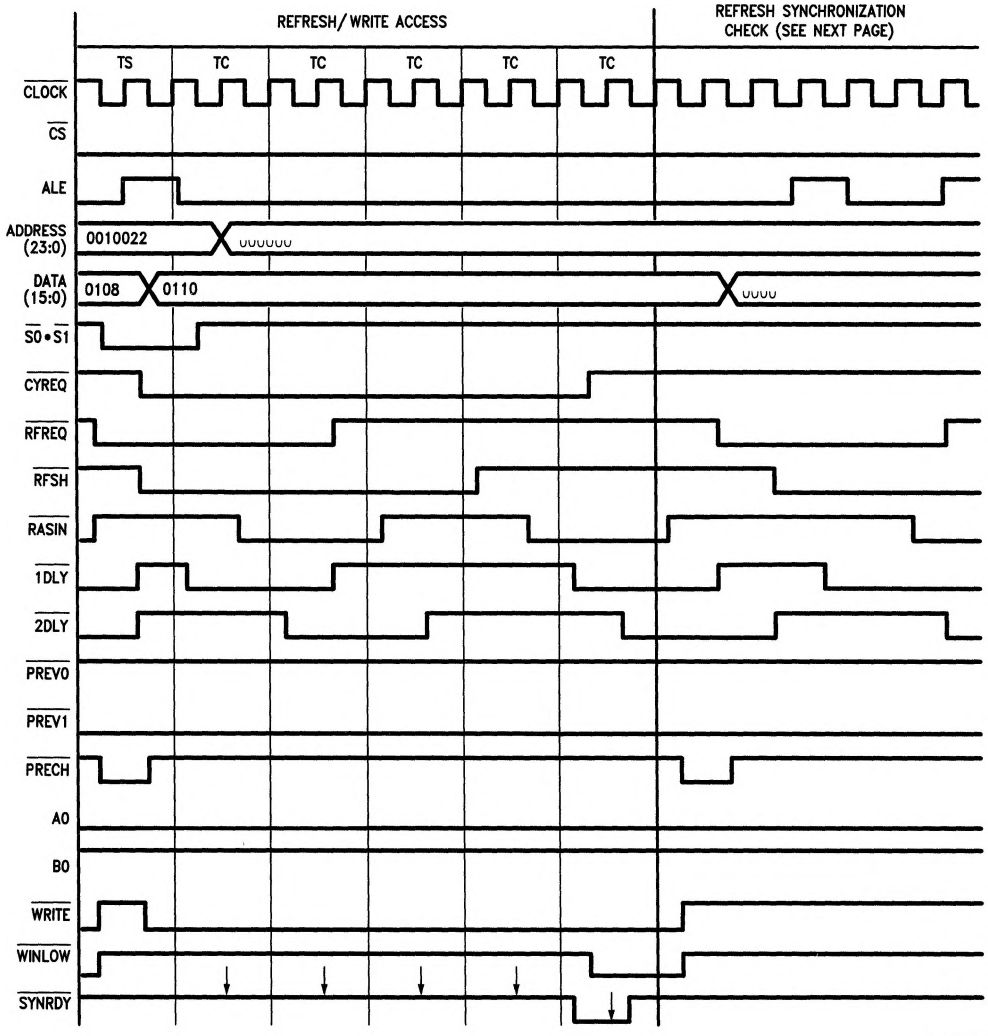

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FIGURE 4

System Timing Diagram (Continued)

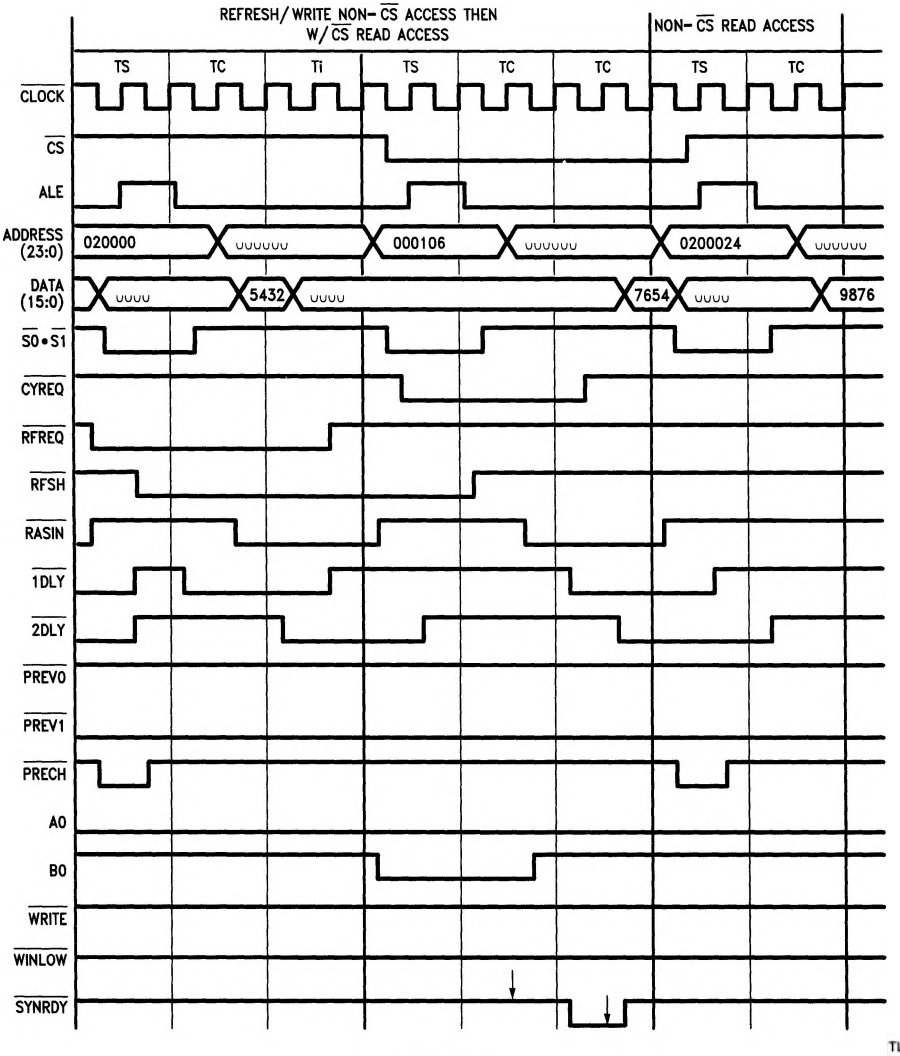

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FIGURE 5

System Timing Diagram (Continued)

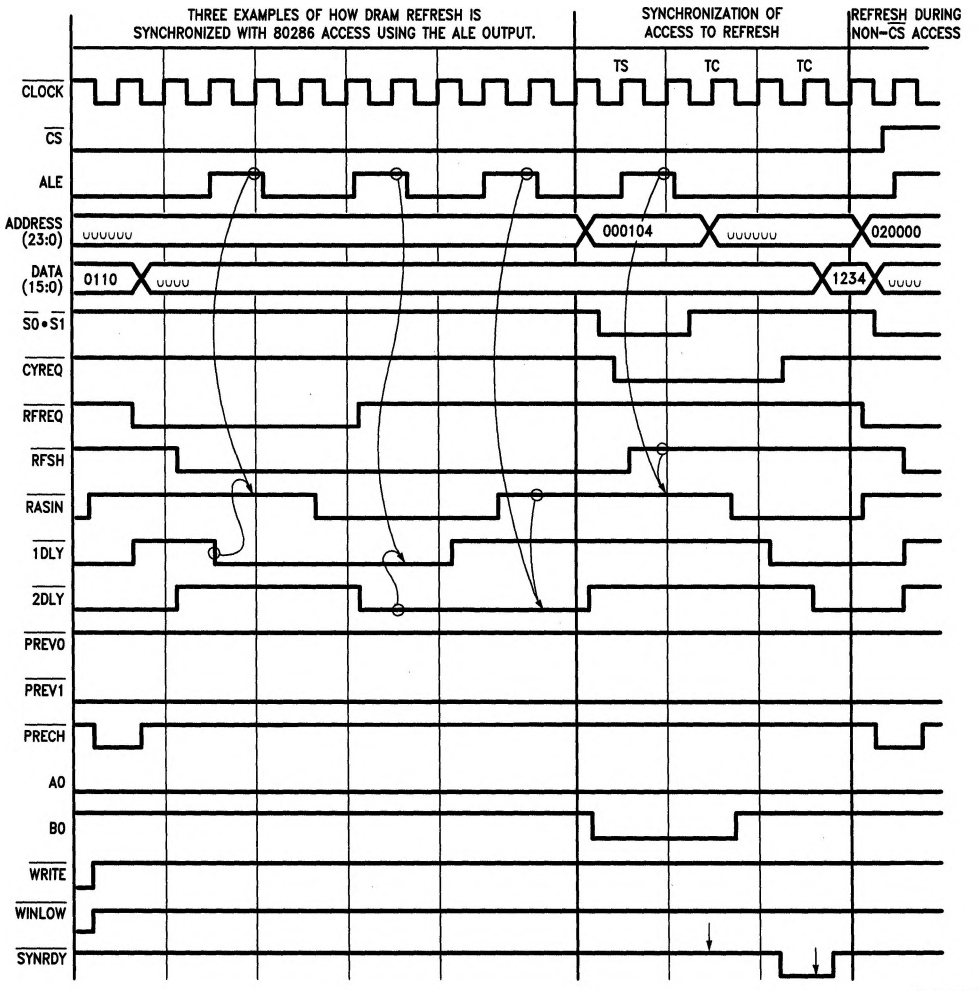

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FIGURE 6