National Semiconductor

DP8463B (2,7) ENDEC

General Description

The DP8463B (2,7) ENDEC performs the encoding and decoding for a disk memory system using a (2,7) Run-Length-Limited (RLL) code. This code gives a disk system the ability to record up to 50% more message data in the same media space without any increase in the Flux Changes per Inch (FCI) density, when compared to a system using Modified Frequency Modulation (MFM) coding. The DP8463B also performs other functions of writing or reading format segments that can not be done by a disk data controller. These additional functions include the writing and reading of Preambles (PLL synchronization fields) and various soft-sector format Address Marks that are compatible with (2,7) RLL code. The user may also select different lengths of preamble to count before the DP8463B issues a Lock Detect signal. The encoded CODE OUT output is automatically resynchronized to the 2f CRYSTAL/SERVO CLOCK for perfect periodic writing regardless of the duty cycle of the WRITE CLOCK input and regardless of the phase relationship between the WRITE CLOCK and the 2f CRYSTAL/SERVO CLOCK. The READ/REFERENCE CLOCK output is switched between clock sources without generating any short pulses. In addition to the detecting of standard ESDI and SMD Address Marks, there is an optional noise tolerant mode that allows the recognizing of an address mark gap even with a bit or two of noise.

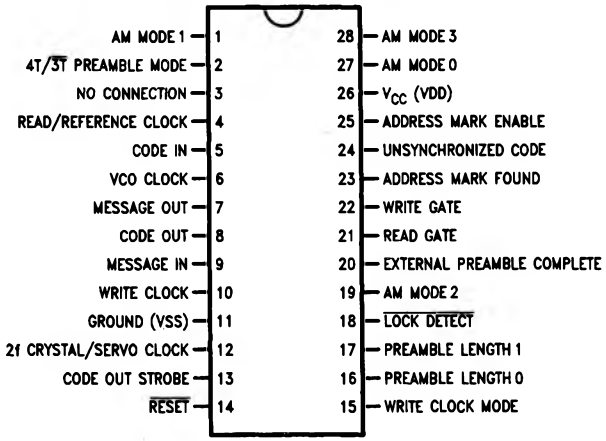
The DP8463B is compatible with the Storage Module Drive (SMD) and Enhanced Small Device Interface (ESDI) functional specifications, and has a format mode similar to the one used in ST-506 devices. The Input/Output (I/O) of the DP8463B are active-high, except LOCK DETECT, so inverting line drivers should be used for interfacing with the active-low I/O of ESDI. The term "Message" is used to designate unencoded data, also referred to as NRZ Data in disk literature. The term "Code" designates the encoded data.

Features

- Up to 50% increase in message data density over MFM
- Encodes and decodes using IBM (2,7) Message/Code Table
- Programmable Formats
  - — Hard Sector
  - — Soft Sector with Address Mark preceding Preamble
  - — Soft Sector with Address Mark following Preamble
- Programmable Address Marks
  - — ESDI 3-Byte transitionless gap, preceding Preamble
  - — ESDI 3-Byte transitionless gap, noise tolerant
  - — SMD 3-Byte transitionless gap, preceding Preamble
  - — SMD 3-Byte transitionless gap, noise tolerant
  - — IBM 2-Byte gap with three transitions, preceding Preamble
  - — N7V 2-Byte Address Mark with code word not in message/code table that does not violate (2,7) code constraints, following Preamble
    (Above gap lengths are in message-bytes)
- Programmable Preamble length counted before LOCK DETECT issued
  - — Externally determined (e.g., from DP8462 Data Synchronizer)
  - — 6 Message Bytes
  - — 8 Message Bytes
- Code output is resynchronized to 2f CRYSTAL/SERVO CLOCK
- Glitchless Multiplexer is used to switch between READ/REFERENCE CLOCK sources
- Strobe available to clock CODE OUT output into external register
- ADDRESS MARK FOUND appears after first "1" bit following Address Mark
- Message Data Rate to 20 Megabits/second (Code rate = 40 Mb/s)
- Compatible with ESDI
- Compatible with SMD
- Compatible with DP8462 Data Synchronizer
- Compatible with DP8466 Disk Data Controller
- 2-micron dual metal CMOS
- Single +5V Supply
- Packages
  - — 28-pin Dual-In-Line Package
  - — 28-pin Plastic Chip Carrier

Connection Diagrams

Dual-In-Line Package (DIP)



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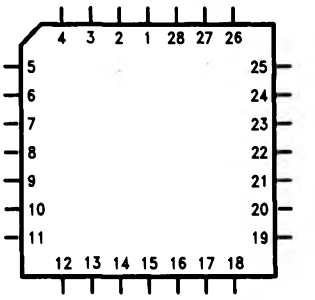
Order Number DP8463BN
See NS Package Number N28B

Plastic Chip Carrier
(Signal Assignments to the Pin Numbers are Identical to DIP)



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Order Number DP8463BV
See NS Package Number V28A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	−0.5V to +7.0V
Input or Output Voltage	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C
Lead Temperature	260°C

Recommended Operating Conditions

Temperature Range (T_A)	+0.0°C to +70°C

ESD rating is to be determined.

DC Electrical Characteristics

V_{CC} = +5V ±10%; Min./Max. limits apply across temperature range T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage		2.25		V
V_{IL}	Low Level Input Voltage			0.65	V
V_{OH1}	High Level Output Voltage	V_I = V_{CC} or GND I_O = 20 μA	V_{CC} − 0.1		V
V_{OH2}	High Level Output Voltage	V_I = V_{CC} or GND I_{OH} = −4.0 mA	3.5		V
V_{OL1}	Low Level Output Voltage	V_I = V_{CC} or GND I_O = 20 μA		0.1	V
V_{OL2}	Low Level Output Voltage	V_I = V_{CC} or GND I_{OL} = +4 mA		0.4	V
I_{IH}	High Level Input Current	V_I = V_{CC}		+10	μA
I_{CC} DY	Supply Current, Dynamic	V_I = V_{CC} or GND T_A = 25°C, f_{VCO} = 40 Mb/s		60	mA
I_{CC} SB	Supply Current, Standby	V_I = V_{CC} or GND T_A = 25°C, f_{VCO} = 1Mb/s		10	mA

AC Electrical Characteristics

(V_{CC} = 5V ±10%; Min./Max. limits apply across temperature unless otherwise specified. Output Load = 50 pF.)

Symbol	Parameter	Part No.	Min	Typ	Max	Units
f_{DATA}	Maximum Message Data Frequency (NRZ Data)	DP8463B-12	12			Mb/s
f_{VCO} $f_{C/S}$	Maximum VCO Frequency Maximum CRYSTAL/SERVO CLOCK frequency	DP8463B-12	24			Mb/s
t_{MISU}	Set-Up Time of MESSAGE IN Before WRITE CLOCK Positive Edge		10			ns
t_{MIH}	Hold Time of MESSAGE IN After WRITE CLOCK Positive Edge		10			ns
t_{MOSU}	Set-Up Time of MESSAGE OUT Before READ/REFERENCE CLOCK Positive Edge		24			ns
t_{MOH}	Hold Time of MESSAGE OUT After READ/ REFERENCE CLOCK Positive Edge		14			ns
t_{CISU}	Set-Up Time of CODE IN Before VCO CLOCK Positive Edge		7			ns
t_{CIH}	Hold Time of CODE IN After VCO CLOCK Positive Edge		10			ns
t_{COSU}	Set-Up Time of CODE OUT Before CODE OUT STROBE Positive Edge		10			ns
t_{COH}	Hold Time of CODE OUT After CODE OUT STROBE Positive Edge		5			ns
t_{PWUC}	Pulse Width of UNSYNCHRONIZED CODE		10			ns
t_{PWPC}	Pulse Width of EXTERNAL PREAMBLE COMPLETE		4			VCO Clock Periods
t_{pdIE}	Propagation Delay of IBM Encoder from WRITE CLOCK Positive Edge to CODE OUT		7		7	Code Bits
			+5		+45	ns
t_{pdIDC}	Propagation Delay of IBM Decoder from VCO CLOCK Postive Edge to READ/REFERENCE CLOCK Positive Edge		5.5		5.5	Code Bits
			+5		+62	ns
WCL	WRITE CLOCK Low		20%		80%	WRITE CLOCK Period
WCH	WRITE CLOCK High		20%		80%	

Note 1. Mb/s = Megabits/second
Code bit = period of 2f or VCO Clock

Pin Descriptions

Pin No	Description
POWER	
11	**GROUND (V_{SS})**
26	**V_{CC} (V_{DD})**
INPUT SIGNALS	
5	**CODE IN.** This is the encoded data output of the data synchronizer (e.g., DP8462). Each flux transition on the disk is a high level signal here with a width of one VCO clock period. The CODE IN is read by the DP8463B at the time of the positive going edge of the VCO CLOCK.
6	**VCO CLOCK.** This is the VCO clock output of the data synchronizer (e.g., DP8462). During the read mode, the VCO CLOCK is phase locked to the flux transitions on the disk.
9	**MESSAGE IN.** This is the unencoded "write data" from the disk data controller (e.g., DP8466). MESSAGE IN is read into the DP8463B by the positive going edge of the WRITE CLOCK input.
10	**WRITE CLOCK.** This clock strobes the MESSAGE IN "write data" into the encoder.
12	**2f CRYSTAL/SERVO CLOCK (2f C/S CLOCK).** This is the clock output of a disk drive's dedicated servo track or the buffered output of a crystal oscillator. This signal is the reference clock for generating the CODE OUT signal when the WRITE CLOCK MODE pin is low.
14	**$\overline{\text{RESET}}$.** An active low input resets various flip-flops when the next 2f C/S CLOCK positive edge occurs, so RESET should have a pulse width of two 2f C/S CLOCK periods. The DP8463B should be reset after each time power is applied.
20	**EXTERNAL PREAMBLE COMPLETE.** With PL1 and PL0 both low, an "active" level on this pin signals the DP8463B that the reading of the preamble, for phase locking purposes, is complete. The DP8463B then switches into its normal decoding mode and issues an active low LOCK DETECT signal. This mode could be used for short preamble lengths in conjunction with the DP8462. The DP8462 Lock Detect output would be connected to the EXTERNAL PREAMBLE COMPLETE (observing polarities, see pin 28). The DP8462 will issue a "Lock Detect" after counting 16 code ones (3 to 4 Message Bytes depending upon which preamble pattern is used, 3T or 4T). The DP8463B must receive at least two 4T preamble patterns before an EXTERNAL PREAMBLE COMPLETE signal is received. The "active" level of this pin is determined by the state of pin 28, ADDRESS MODE 3.
21	**READ GATE.** An active high level input places the DP8463B in the read mode. During this mode: the source of the READ/REFERENCE CLOCK is switched to the VCO CLOCK/2, the address mark is searched for (if selected), the length of the preamble is counted as programmed, and the CODE IN signal is decoded and output as MESSAGE OUT at the appropriate time per the programming of the mode pins.
22	**WRITE GATE.** An active high level input places the DP8463B in the write mode. During this mode: the MESSAGE IN data is encoded and output as CODE OUT, and during the programmed time (when selected), the preamble and address marks appear at CODE OUT.
24	**UNSYNCHRONIZED CODE.** This is the encoded data output of the pulse detector (e.g., DP8464B). A flux transition on the disk produces an active high pulse for this pin. This input is used to detect the ESDI, SMD, and IBM address marks.
25	**ADDRESS MARK ENABLE (AME).** An active high level, while WRITE GATE is also active high, will write the address mark prescribed by the AM MODE pins. The AME must be high for the complete address mark. An active high level of AME while WRITE GATE and READ GATE are both low causes the 8463B to search for an Address Mark when in the ESDI Mode (AM2 & AM1 low). An active high level of AME when READ GATE is active high causes the 8463B to search for an AM when in the SMD Mode (AM2 low, AM1 high).
PROGRAMMING INPUTS	
1	**ADDRESS MARK MODE 1 (AM MODE 1).** Defined in Table I. A logic "1" is a high level.
2	**4T/$\overline{\text{3T}}$ PREAMBLE MODE.** A high level places the DP8463B in the mode to generate and detect "4T" preamble patterns (i.e., 1000 in code which is four time periods). In this mode, the MESSAGE IN input is inverted in the DP8463B before being encoded so that a 4T preamble can be generated from an all zeros MESSAGE IN data stream. The output of the decoder is also inverted in this mode so the double inversion is transparent to the user. The double inversion is always done in this mode, not just during the preamble. A low level input on this pin places the DP8463B in the mode to accept the "3T" pattern as the preamble (3T pattern is 100 in code). The Input/Output is not inverted in this mode. If the 3T preamble pattern is used with the IBM code, a non-zero three-bit repeating input pattern is required which

Pin Descriptions (Continued)

Pin No	Description
PROGRAMMING INPUTS (Continued)	
2 (Cont.)	is typically impossible for a disk data controller to generate. Therefore there is a special mode during which the disk data controller's input to MESSAGE IN is ignored by the encoder section and the DP8463B internally generates a 3T code output; as long as the MESSAGE IN input is all zeros. This 3T preamble starts after the initiation of WRITE GATE going active (high) and continues until the first "1" is seen at the MESSAGE IN pin. This mode of internally generating a 3T preamble with IBM code is activated by having high levels on the two PREAMBLE LENGTH 0 and PREAMBLE LENGTH 1 pins (16 & 17).
3	**NO CONNECTION.** This pin must be left open-circuited or tied to V_{CC}.
15	**WRITE CLOCK MODE.** A low level enables the automatic resynchronization circuitry for the IBM encoder. The WRITE CLOCK is resynchronized to the 2f C/S CLOCK and used for clocking the IBM encoder. The same 2f C/S is used to clock a flip-flop that provides the CODE OUT signal. A high level WRITE CLOCK MODE input allows the WRITE CLOCK to directly clock the IBM encoder. In this mode the CODE OUT signal comes directly from the encoder and does not get strobed out by the 2f C/S CLOCK.
16	**PREAMBLE LENGTH 0 (PL0).** This input and PREAMBLE LENGTH 1 (PL1) determine the length of preamble that is read before an active low LOCK DETECT signal is issued. These two pins also control the internal generation of a 3T preamble pattern for use with an all zeros MESSAGE IN input.

PL1	PL0	LENGTH OF PREAMBLE/ OTHER FUNCTION
0	0	Length Set by External Preamble Complete
0	1	6 Message Bytes
1	0	8 Message Bytes
1	1	6 Message Bytes/Generate 3T Preamble Internally

17	**PREAMBLE LENGTH 1 (PL1).** See pin 16.
19	**ADDRESS MODE 2.** Defined in Table I.
27	**ADDRESS MODE 0.** Defined in Table I.
28	**ADDRESS MODE 3.** Defined in Table I. The level of this pin also determines the active level polarity of the pin 20 EXTERNAL PREAMBLE COMPLETE input. This is possible since the Table 1 function is a Don't Care for all except one type of the N7V Address Mark. If ADDRESS MODE 3 is high or open-circuited, then pin 20 is active high. If ADDRESS MODE 3 is low, then pin 20 is active low.

Pin No	Description
OUTPUT SIGNALS	
4	**READ/REFERENCE CLOCK.** This is the clock that is provided to the disk data controller where it is typically labelled "read clock". It is, however, necessary for both reading and writing. The source of the clock is different during reading compared to writing. When READ GATE is active (high) the READ/REFERENCE CLOCK is the VCO CLOCK divided-by-two. The MESSAGE OUT data is read by the disk data controller using the positive going edge of READ/REFERENCE CLOCK. When READ GATE is inactive (low), the READ/REFERENCE clock is the 2f C/S CLOCK divided-by-two. This clock is used by the disk data controller as the timing source for its WRITE DATA and WRITE CLOCK outputs.
7	**MESSAGE OUT.** This is the "Read Data" input to the disk data controller. A high level represents a "one" of decoded (NRZ) data. It is read by the controller using the positive going edge of the READ/REFERENCE CLOCK. MESSAGE OUT is held at a low level when READ GATE is inactive (low) and other intervals specified in Table I.
8	**CODE OUT.** A high level for a 2f clock period is output for each "1" in code that is to be written on the disk as a flux transition by a write amplifier containing a write flip-flop that changes state every time a positive going pulse edge is received. Since (2,7) code always has at least two zeros between adjacent ones, this output is a Return-to-Zero (RZ) code. If the CODE OUT is to be sent to another register, instead of directly to the Write Amplifier, it can be clocked out by using the CODE OUT STROBE.
13	**CODE OUT STROBE.** The positive going edge of this signal should be used as the clock input to an external shift register for applications where the CODE OUT is transformed before being sent to the Write Amplifier, e.g., for precompensation of some code patterns on some tracks.
18	**$\overline{\text{LOCK DETECT}}$.** A low level signifies that a minimum, uninterrupted length of the programmed preamble pattern has been read. The length of the preamble read is programmed by PREAMBLE LENGTH 0 and 1. The LOCK DETECT level returns to a high when READ GATE goes inactive (low).
23	**ADDRESS MARK FOUND (AMF).** A high level appears when an address mark has been sensed and, depending upon programming, other conditions may also be required before the AMF goes active (high). Table I specifies the various conditions under which AMF becomes active and inactive. Also see the Address Mark section under "Description of Format and Circuit Characteristics".

TABLE I. Address Mark Modes

AM Mode	Program Inputs				AM Written	AM Read	Inputs		Output	
	AM 3	AM 2	AM 1	AM 0			Read Gate During AM Search	AME During AM Search	AMF Goes Active When:	AMF Returns Inactive When:
ESDI, Fully Compatible	X	0	0	0	ESDI	ESDI	Inactive (L)	Active (H)	AM Found & 1st Code "1" Following AM	AME Goes Inactive
ESDI, Noise Tolerant	X	0	0	1	ESDI	ESDI or IBM	Inactive (L)	Active (H)		
SMD, Fully Compatible	X	0	1	0	SMD	SMD	Active (H)	Active (H)		
SMD, Noise Tolerant	X	0	1	1	SMD	SMD or IBM	Active (H)	Active (H)		
Hard Sector	X	1	0	0	None (ESDI/SMD Signals)	None	Don't Care	Don't Care	NA	NA
ESDI/SMD (8466 Comp.)	X	1	0	1	ESDI = SMD	ESDI = SMD	Don't Care	Don't Care	AM Found & 1st Code "1" Following AM	2nd Code "1" Following AM is Read
IBM	X	1	1	0	IBM	IBM	Don't Care	Don't Care		
N7V-A (Note 1)	1	1	1	1	N7V (In Header & Data Segments)	N7V (In Header & Data Segments)	Active (H)	Don't Care	AM Found & 1st Message "1" Following AM	Read Gate Goes Inactive (L)
N7V-B	0	1	1	1	N7V (In Header Only)	N7V (In Header Only)	Active (H)	Active (H)		

X = Don't Care NA = Not Applicable

(Continued on next page)

TABLE I. Address Mark Modes (Continued)

AM Mode	Program Inputs AM 3	AM 2	AM 1	AM 0	Phase Sync (Byte) Requirements:	Byte Sync (Byte) Requirements	MESSAGE OUT = 0 Until: (& Phase Sync Mode Ends) (Note 2)
ESDI, Fully Compatible	X	0	0	0	1. With 4T Preamble: Function done by all zeros preamble. 2. With 3T Preamble: Recommend writing 10111100 which is read as 00000000.	1. With 4T Preamble: Must have one or more "1"s; with one in leading position, preferably. 2. With 3T Preamble: Must have one or more "1"s; Leading two bits should be zeros.	1. With 4T Preamble: After 6 or Programmed number of bytes of preamble are read. 2. With 3T Preamble: After two 4T patterns in phase sync byte are read.
ESDI, Noise Tolerant	X	0	0	1			
SMD, Fully Compatible	X	0	1	0			
SMD, Noise Tolerant	X	0	1	1			
Hard Sector	X	1	0	0			
ESDI/SMD = (8466 Comp.)	X	1	0	1			
IBM	X	1	1	0			
N7V-A (Note 1) N7V-B	1 0	1 1	1 1	1 1	1. With 4T Preamble: Write 8 zeros. 2. With 3T Preamble: Write 8 ones.	3. With 4T Preamble: Use 00000010 & 00000011. Same as 1 and 2 Above.	[N7V AM is Detected] $\underbrace{(\text{N7V AM Detected} \bullet \text{AME})}_{\text{For Header}} + \underbrace{\text{N7V AM Detected} \bullet \overline{(\text{AME})}}_{\text{For Data}}$ Segment (Note 3)

X = Don't Care NA = Not Applicable

Note 1. Use only for 8463A compatibility where there is an N7V AM in both header & data segments.

Note 2. After the time MESSAGE OUT = 0, MESSAGE OUT = Decoded CODE IN

Note 3. Data segment has no AM

TABLE II. Message Data/Code Tables

IBM (2,7,1,2,3) Message Data/Code Table

Normal Message Data		Inverted Message Data		Code	
MSB	LSB	MSB	LSB	MSB	LSB
000		111		000100	
10		01		0100	
010		101		100100	
0010		1101		00100100	
11		00		1000	
011		100		001000	
0011		1100		00001000	

Most Significant Bit (MSB) is read/written first.

Use the Normal Message Data column when 4T/$\overline{3T}$ PREAMBLE MODE (pin 2) is low.

Use the Inverted Message Data column when 4T/$\overline{3T}$ PREAMBLE MODE is high.

NOTE: The IBM (2,7,1,2,3) Code and some implementations of it are patented by IBM. National Semiconductor Corporation (NSC) has a license agreement with IBM enabling NSC to incorporate a particular implementation of the IBM (2,7) Endec in an integrated circuit for sale to others. Also see the Patent Indemnification section in NSC's Standard Terms and Conditions for Sales.

Note: Definition of (2,7,1,2,3):

2 = minimum number of zeros between adjacent code ones

7 = maximum number of zeros between adjacent code ones

1 = ratio of message data bits to code bits with first number (1)

2 = being the number of message bits

3 = number of different lengths of message data words

Description of Format and Circuit Characteristics

1. Address/Sector Marks

1A. Hard Sector Format—Sector Mark

In this format the sector mark signal from the disk drive is sent directly to the disk data controller and the DP8463B is not involved.

1B. Soft Sector Format—Address Mark (AM)

1B-1. ESDI Address Mark

This is a gap on the disk without any flux transitions for a length of three message bytes. The gap appears at the start of each sector. It is written by having the ADDRESS MARK ENABLE (AME) active (high) for 3 message bytes while WRITE GATE is also active (high). The AM is detected when an interval of 16 message bit times passes without a flux transition. Table I shows three different modes for using the ESDI AM. The "ESDI, FULLY COMPATIBLE" is the fully-compatible-with-ESDI specifications mode where AME is active (high) while READ GATE and WRITE GATE are inactive (low) when looking for an AM. When the AM is found, ADDRESS MARK FOUND (AMF) goes active (high), the disk data controller receives this and responds by having READ GATE go active (high) and AME go inactive (low). The AME going inactive will cause the 8463B's AMF to go inactive (low). A second mode "ESDI, NOISE TOLERANT" has the ability to accept a few noise bits in the AM gap and still output an AMF. (See Noise Tolerant ESDI/SMD AM section for full explanation). A third mode of ESDI AM has the state of the AME, during an AM search, as a "don't care" for compatibility with the DP8466 controller. In all these modes, the AMF appears only after both the AM is sensed and the first code "1" bit of the preamble is detected.

1B-2. SMD Address Mark

This AM is the same 3 message byte gap as ESDI. The difference is the state of READ GATE during the search for an AM. For SMD compatibility, READ GATE must be active (high) during the AM search. The three SMD modes shown in Table I are analogous to the three ESDI modes.

1B-3. IBM Address Mark:

This AM is a gap of 32 code bits which has no flux transitions except for two transitions in bit positions 8 and 20. The first 7 bit positions are "don't cares" per IBM's definition. The DP8463B writes a "1" (transition) in positions 3, 8 and 20. The DP8463B detects these AMs by detecting two gaps of 10 bits with a "1" between the two gaps. If the first gap is larger than 16 bits, the detector will reset and begin again.

1B-4. Noise Tolerant ESDI/SMD AM:

These modes will accept a perfect 2-message-byte ESDI or SMD gap or a gap which contains some noise bits. The ESDI/SMD AM gap detector is ORed with the IBM AM detector so an AMF will appear if either a 2-message-byte gap (32 code bits), or two 10-code-bit gaps with a "1" in between, is detected in the 3-message-byte (48 code bits) gap. The 16-bit limit on the first gap of the IBM AM detector is disabled.

1B-5. N7V Address Mark (N7V = Non 7 Violation):

This AM is a unique code word that does not violate the (2,7) RLL constraints but can not be generated by any message input to the IBM encoder. The N7V AM is a two-message-byte AM that must follow the preamble, since the decoder must be in phase sync to read the AM properly. The first byte of the AM consists of 4T phase sync patterns, the second byte is the unique N7V pattern. If the disk data controller randomly asserts READ GATE, the possibility of the N7V AM being detected in the write splice or in the data, before phase sync has been achieved, must be avoided. This can be done by not routing the CODE IN input to the 8463B until several bytes of the preamble have been detected externally. For example, this is done simply with the DP8462 by ANDing its SYNCHRONIZED DATA output with its inverted LOCK DETECT output, since the LOCK DETECT only appears after 3 or 4 bytes of the preamble have been read.

See Table I for more detail of Inputs/Outputs during AM reading and writing.

Description of Format and Circuit Characteristics (Continued)

2. Phase Sync Pattern

The decoder must be able to distinguish between the odd and even code bits to decode properly. This is impossible to do with the maximum frequency "3T" code pattern (100) in a preamble because the "1" alternates between odd and even positions. The "4T" code pattern (1000) must be used, along with the knowledge of what message pattern was used to generate it. A "3T" preamble can be used if it is followed by two "4T" patterns before data is read. See *Figure 1* formats for examples, and Table II for encode/decode definitions.

3. Byte Sync Pattern:

The purpose of the Byte Sync (or Sync Byte) is to define the message byte boundary for the disk data controller. The Byte Sync message byte should consist of one or more "1"s. With "4T" preambles, the Byte Sync should, preferably, have a "1" in the leading bit position. With "3T" preambles, the Byte Sync should have zeros in the two leading positions (to buffer it in time from the phase sync byte).

4. Error Propagation:

Since a single bit-shift error in a code word may be decoded as a different message word, there is error propagation. The longest error burst found for the IBM Code is 5 message bits. Therefore, the disk system must have Error Checking and Correcting (ECC) circuitry capable of correcting these errors.

5. Format Examples:

Figure 1 illustrates the sector formats and timing of various control signals for each of the Address Mark Modes and Preamble types for both reading and writing.

Formats

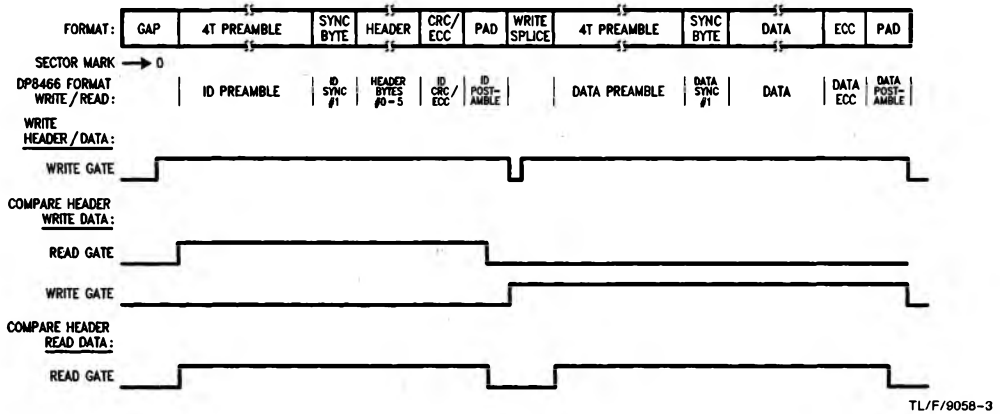

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FIGURE 1-1. Hard Sector, 4T Preamble

Formats (Continued)

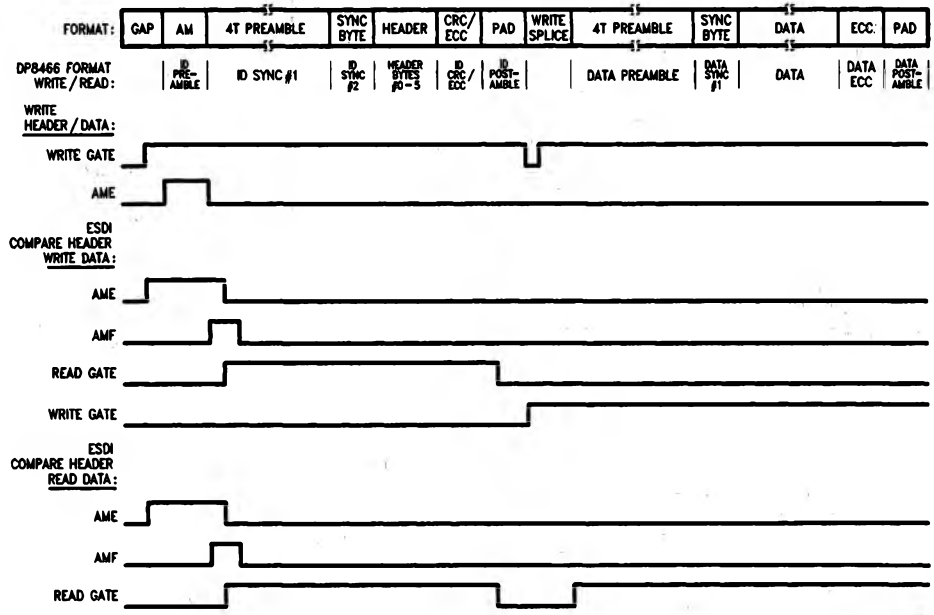

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FIGURE 1-2. SMD, ESDI, IBM Address Mark, 4T Preamble

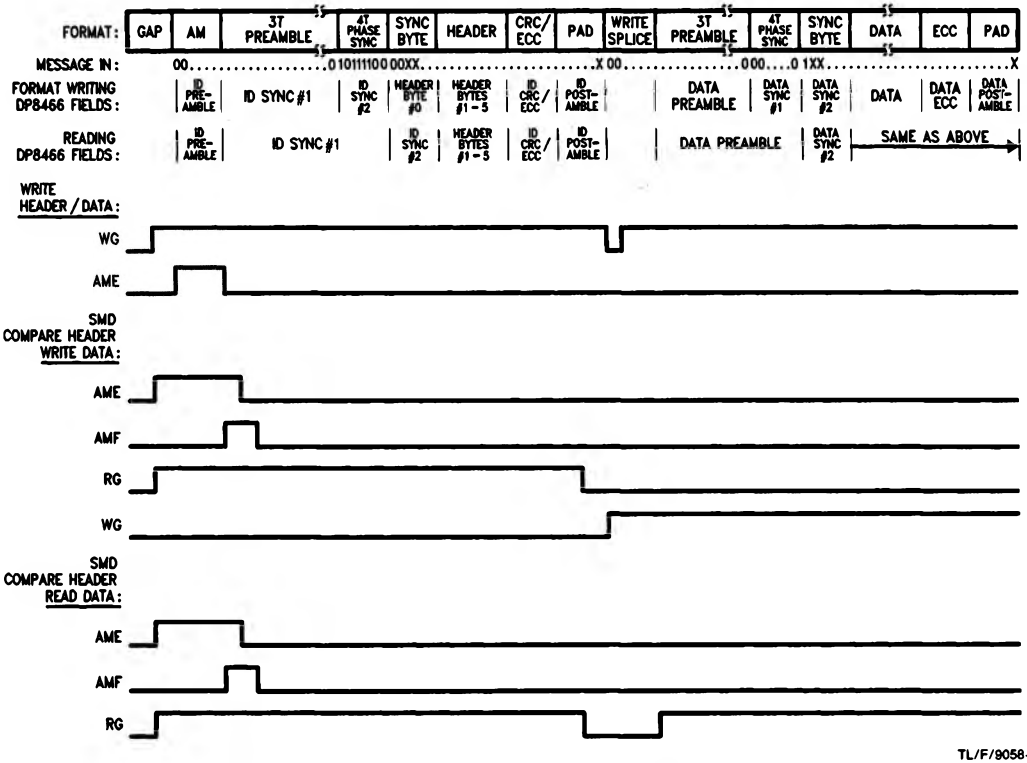

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FIGURE 1-3I. ESDI, SMD, or IBM AM, 3T Preamble

Formats (Continued)

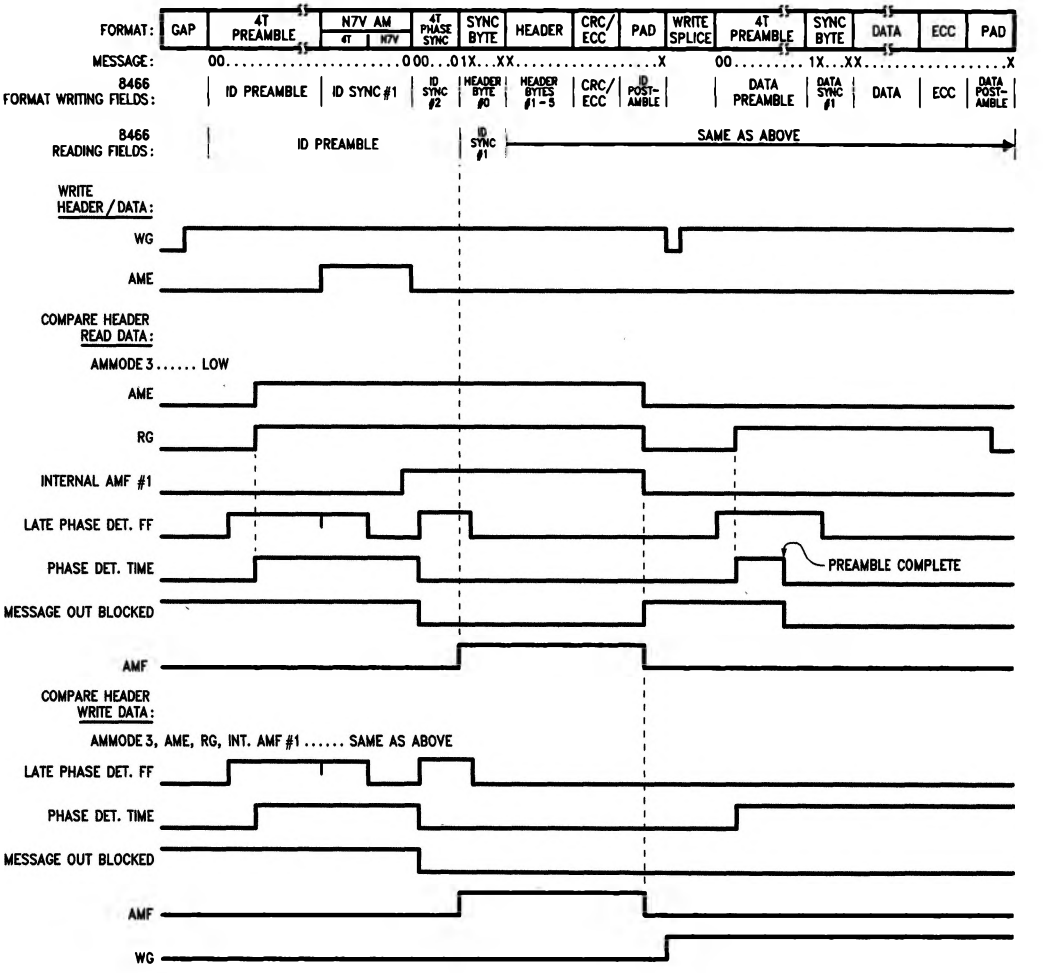

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FIGURE 1-4. 4T Preamble, N7V AM (N7V-B Mode)

Formats (Continued)

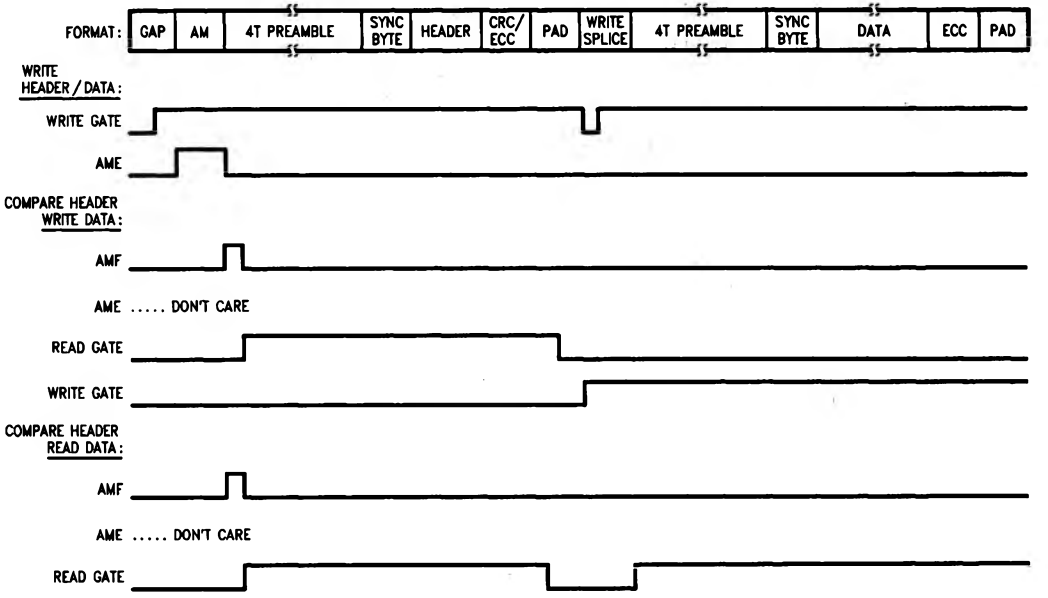

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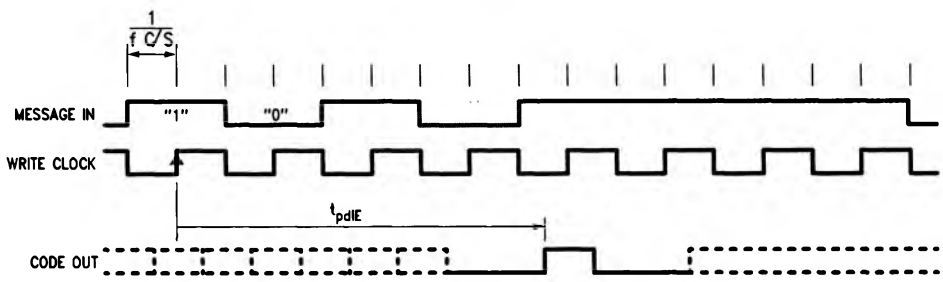
FIGURE 1-5. ESDI, SMD, or IBM AM; 4T Preamble (with Read Gate & AME as "don't cares" during search for AM)

Timing Waveforms

IBM Encoder



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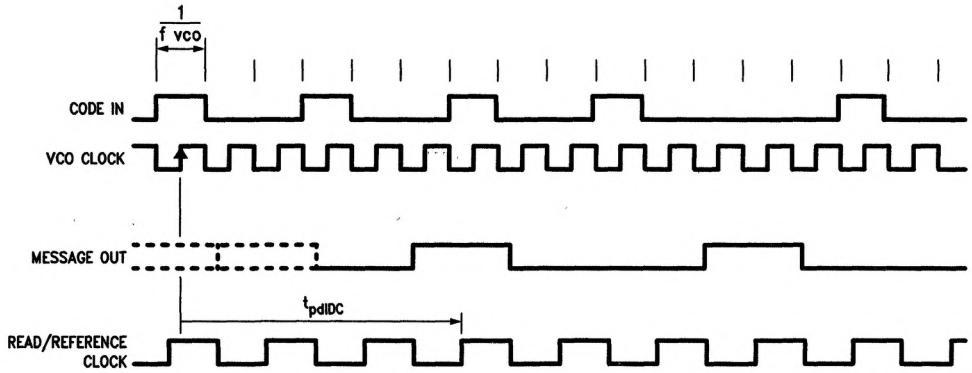
Timing Waveforms (Continued)

IBM Decoder



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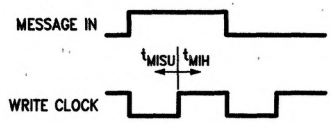

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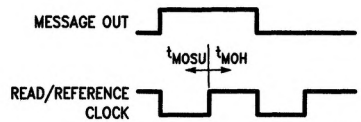

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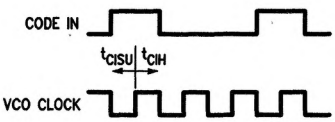

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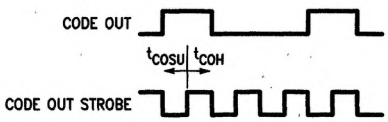

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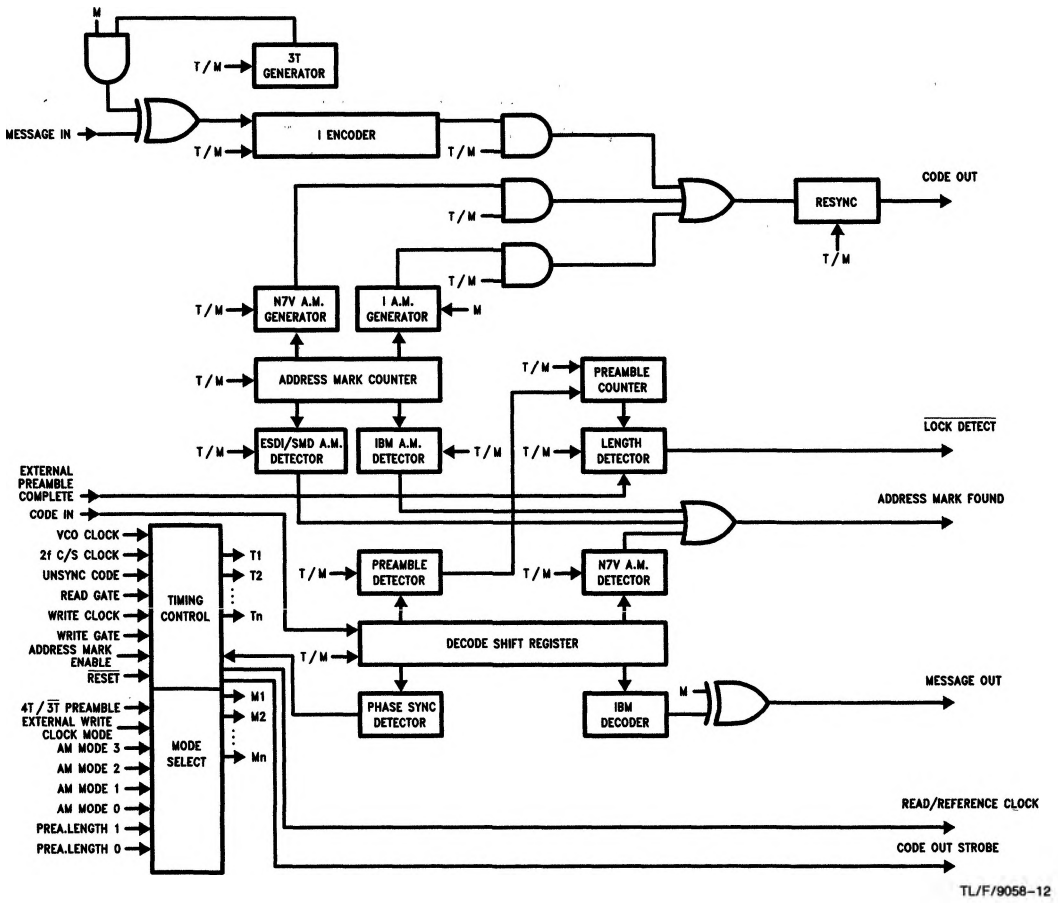
Typical Applications

DP8463B (2, 7) Endec Block Diagram



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Typical Applications (Continued)