

## 3 Phase Motor Driver-IC for Automotive Safety Applications

Check for Samples: [DRV3201-Q1](#)

### FEATURES

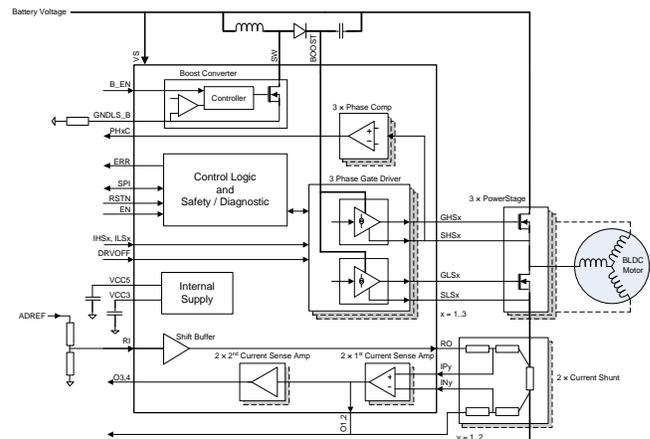
- Qualified for Automotive Applications
- AEC-Q100 Qualified
- 3 Phase Bridge Driver for Motor Control
- Drives 6 Separate N-Channel Power MOSFETs up to 250 nC Gate Charge
- Programmable 140 mA–1 A Gate Current Drive (Source/Sink) for Easy Output Slope Adjustment
- –7 V to 40 V Compliance on All FET Driver Pins to Handle Inductive Under/Overshooting
- Separate Control Input for Each Power MOSFET
- PWM Frequency up to 30 kHz
- Supports 100% Duty Cycle Operation
- Operating Voltage: 4.75 to 30 V
- Proper Low Supply Voltage Operation Due to Integrated Boost Converter for Gate-Driver Voltage Generation
- Logic Functional Down to 3 V
- Short Circuit Protection With VDS-Monitoring and Adjustable Detection Level
- Two Integrated High Accuracy Current Sense Amplifiers With Two Gain-Programmable Second Stage for Higher Resolution at Low Load Current Operation
- Over and Undervoltage Protection
- Shoot Through Protection With Programmable Dead Time
- Three Real Time Phase Comparators
- Over Temperature Warning and Shut Down
- Sophisticated Failure Detection and Handling Through SPI Interface
- Reverse Battery Protection Down to –4 V (With Series Protection Resistance)
- Sleep Mode Function
- Reset and Enable Function
- Package: 64-pin HTQFP PowerPAD™

### APPLICATIONS

- Automotive Safety Critical Motor-Control Applications
  - Electrical Power Steering (EPS, EHPS)
  - Electrical Brake/Brake Assist
  - Transmission
  - Oil-Pump
- Industrial Safety Critical Motor-Control Applications

### DESCRIPTION

The bridge driver is dedicated to automotive 3 phase brushless DC motor control including safety relevant applications. It provides six dedicated drivers for normal level N-Channel MOSFET transistors. The driver capability is designed to handle gate charges of 250 nC, and the driver source/sink currents are programmable for easy output slope adjustment. The device also incorporates sophisticated diagnosis, protection and monitoring features through an SPI interface. A boost converter with integrated FET provides the overdrive voltage, allowing full control on the power-stages even for low battery voltage down to 4.75 V.


**Figure 1. Typical Application Diagram**
**PRODUCT PREVIEW**


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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		DRV3201	UNIT
		HTQFP	
		PAP - 64 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	21.6	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance	10.9	
$\theta_{JB}$	Junction-to-board thermal resistance	4.5	
$\psi_{JT}$	Junction-to-top characterization parameter	0.1	
$\psi_{JB}$	Junction-to-board characterization parameter	4.4	
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PRODUCT PREVIEW

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

over operating temperature  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ 

SYMBOL	PARAMETER	CONDITIONS	VALUE		UNIT
			MIN	MAX	
VS, VSH	DC	VS, negative voltages with minimum serial resistor $5\ \Omega$	-5	38	V
		VS, negative voltages with external protection NMOS	-14	38	V
VS, VSH	Supply voltage, transient 1s	VS, negative voltages with minimum serial resistor $5\ \Omega$	-5	42	V
		VS, negative voltages with external protection NMOS driven by device internal circuit	-14	42	V
GHSx	Gate high-side voltage		-7	47	V
SHSx	Source high-side voltage		-7	42	V
GHSx-SHSx	Gate-source high-side voltage difference	External driven, internal limited (see $I_{\text{BOOST}}$ in <a href="#">RECOMMENDED OPERATING CONDITIONS</a> )	-0.3	15	V
GLSx	Gate low-side voltage		-7	20	V
SLSx	Source low-side voltage		-7	7	V
GLSx-SLSx	Gate-source low-side voltage difference	External driven, internal limited (see $I_{\text{BOOST,sw}}$ in <a href="#">RECOMMENDED OPERATING CONDITIONS</a> )	-0.3	15	V
BOOST, SW	Boost converter		-0.3	60	V
INx, IPx	Current sense Input voltage		-0.3	42	V
INx, IPx clamping current	Current sense input current	Clamping current	-5	5	mA
Ox	Current sense output voltage		-0.3	ADREF +0.3	V
Ox forced input current			-10	10	mA
VDDIO, ADREF	Analog input voltage		-0.3	8	V
ILSx, IHSx, EN, DRVOFF, SCLK, NCS, SDI, RSTN, CSM, B_EN	Digital input voltage		-0.3	18	V
SCTH	Analog input voltage		-0.3	18	V
GNDa, GNDL, GNDLS_B, PGND, NC	Difference one GND or NC to any other GND or NC		-0.3	0.3	V
$T_J$	Operating virtual junction temperature range		-40	150	$^{\circ}\text{C}$
$T_S$	Storage temperature range		-40	165	$^{\circ}\text{C}$
$T_{\text{LEAD}}$	Lead temperature (soldering, 10 s)			260	$^{\circ}\text{C}$
ESD all pins <sup>(3)</sup>	ESD performance of all pins to any other pin	HBM model	-2	2	kV
ESD pin SHSx <sup>(3)</sup>	ESD performance of SHSx to SHSx and GND	HBM model	-4	4	kV
ESD all pins <sup>(3)</sup>	ESD performance of all pins to any other pin	CDM model	-500	500	V
SR <sub>SHS</sub>	Maximum slew rate of SHSx pins		-150	150	V/ $\mu\text{s}$
ERR, SDO, PHxC, RO	Analog/digital output voltages		-0.3	8	V
ERR, SDO, PHxC, RO	Forced input/output current		-10	10	mA
TEST, AMUX, NC	Unused pins. Connect to GND		-0.3	0.3	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal, unless otherwise specified.

(3) ESD testing is performed according to AEC-Q100 standard.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup> (continued)**over operating temperature  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ 

SYMBOL	PARAMETER	CONDITIONS	VALUE		UNIT
			MIN	MAX	
RI	Analog input voltage		-0.3	18	V
VCC5	Internal supply voltage		-0.3	8	V
I_VCC5	Short-to-ground current	Internal current limit		40	mA
VCC3	Internal supply voltage		-0.3	3.6	V
VCC3	Short-to-ground current	Limited by VCC5		40	mA

**RECOMMENDED OPERATING CONDITIONS**over operating temperature  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, normal voltage operation, VS	Full device functionality	4.75		30	V
Supply voltage, logic operation, VSLO	Logic functional (during battery cranking after coming from full device functionality)	3		40	V
Supply voltage for digital IOs, VDDIO		1.72		5.5	V
Duty cycle of bridge drivers, D		0		100	%
PWM switching frequency, $f_{PWM}$		0		30	kHz
VS quiescent current normal operation (boost converter enabled, drivers not switching), $I_{VSN}$	Typically 65 mA (boost converter enabled), see <a href="#">Figure 13</a> and <a href="#">Figure 14</a> .			90	mA
BOOST pin quiescent current normal operation (drivers not switching), $I_{BOOST}$	Typically 15 mA			20	mA
BOOST pin additional load current due to switching gate-drivers, $I_{BOOST,sw}$	Without external power FETS (pure internal switching current, 30 kHz all gate-drivers switching at the same time)			3	mA
VS quiescent current shut down (EN = low; sleep mode), $I_{VSq}$	VS = 14 V, no operation, $T_J < 85^{\circ}\text{C}$ total leakage current on all supply connected pins			30	$\mu\text{A}$
Junction temperature, $T_J$		-40		150	$^{\circ}\text{C}$
Operating ambient free-air temperature, $T_A$	With proper thermal connection	-40		125	$^{\circ}\text{C}$
Current sense input voltage range, $V_{INx}, V_{IPx}$	Relative to GNDA	-0.14		1.6	V
Clamping voltage for current sense amplifier outputs O 1/ 2/ 3/ 4, ADREF		0.7		5	V
Internal supply voltage, VCC3	VS > 3 V, external load current < 100 $\mu\text{A}$ . Decoupling capacitance is typically 4.7 nF.	2.1 <sup>(1)</sup>		3.3	V
VCC3 output current, $I_{VCC3}$	Intended for MCU ADC input	0		100	$\mu\text{A}$
VCC3 decoupling capacitance, $C_{VCC3}$	Typically 4.7 nF	1		10	nF
Internal supply voltage, VCC5	VS > 6 V, external load current < 100 $\mu\text{A}$ . Decoupling capacitance is typically 4.7 nF.	4.5		5.5	V
VCC5 output current, $I_{VCC5}$	Intended for MCU ADC input	0		100	$\mu\text{A}$
VCC5 decoupling capacitance, $C_{VCC5}$	Typically 4.7 nF	1		10	nF

(1) Lower limit of functional range dependent of internal PowerOnReset level for internal digital logic. It is specified by VS > 3 V the internal digital logic is operational and not put into PowerOnReset.

## ELECTRICAL CHARACTERISTICS

over operating temperature  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  and recommended operating conditions,  $V_S = 4.75$  to  $30\text{ V}$ ,  $f_{\text{PWM}} < 30\text{ kHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Current Sense Amplifier First Stages</b>						
$V_{\text{off}1/2}$	Initial input offset of amplifiers at $T_J = 25^{\circ}\text{C}$		-1	0	1	mV
$V_{\text{off}1/2\_d}$	Temperature and aging offset		-1	0	1	mV
$I_{\text{leak,INxIPx}}$	Input leakage current INx, IPx	$-0.3\text{ V} < \text{INx}, \text{IPx} < 1\text{ V}$ pin-to-pin and pin-to-ground	-10		10	$\mu\text{A}$
$G_{\text{O}1/2}$	DC open loop gain	Specified by design	80			dB
$V_{\text{O}1/2\_N}$	Nominal output voltage range	Normal voltage operation, $V_S \geq 6\text{ V}$ , $\text{ADREF} = 5\text{ V}$ ; $0.5\text{ mA}$ load current	0.5		4.5	V
$V_{\text{O}1/2\_L}$	Output voltage range during low voltage operation	Low voltage operation, $4.75\text{ V} \leq V_S \leq 6\text{ V}$ , $\text{ADREF} = 5\text{ V}$ ; $0.5\text{ mA}$ load current	0.5		4	V
$\text{GBP}_{1/2}$	Gain bandwidth product (GBP)	$0.5\text{ V} \leq \text{O}1/2 \leq 4.5\text{ V}$ Specified by design	5			MHz
$\text{SR}_{1/2}$	Slew rate	$0.5\text{ V} \leq \text{O}1/2 \leq 4.5\text{ V}$ , cap load = $25\text{ pF}$	2.9			$\text{V}/\mu\text{s}$
$\text{PSRR}_{1/2}$	Power supply rejection ratio	$V_S$ to $\text{O}1/2$ . Decoupling capacitance is typically $4.7\text{ nF}$ on $\text{VCC5}$ and $\text{VCC3}$ .		80		dB
$\text{CMRR}_{1/2}$	Common mode rejection ratio	$\text{IN}1/2$ or $\text{IP}1/2$ to $\text{O}1/2$		80		dB
<b>Current Sense Amplifier Second Stages</b>						
$V_{\text{off}3/4}$	Initial input offset of amplifiers at $T_J = 25^{\circ}\text{C}$		-3	0	3	mV
$V_{\text{off}3/4\_d}$	Temperature and aging offset		-3	0	3	mV
$V_{\text{O}3/4\_N}$	Nominal output voltage range	Normal voltage operation, $V_S \geq 6\text{ V}$ , $\text{ADREF} = 5\text{ V}$ ; $0.5\text{ mA}$ load current	0.5		4.5	V
$V_{\text{O}3/4\_L}$	Output voltage range during low voltage operation	Low voltage operation, $4.75\text{ V} \leq V_S \leq 6\text{ V}$ , $\text{ADREF} = 5\text{ V}$ ; $0.5\text{ mA}$ load current	0.5		4	V
$\text{GBP}_{3/4}$	Gain bandwidth product (GBP)	$0.5\text{ V} \leq \text{O}3/4 \leq 4.5\text{ V}$ , gain = 8 Specified by design	5			MHz
$\text{SR}_{3/4}$	Slew rate	$0.5\text{ V} \leq \text{O}3/4 \leq 4.5\text{ V}$ , cap load = $25\text{ pF}$	2.9			$\text{V}/\mu\text{s}$
G1	Gain1		1.98	2	2.02	V/V
G2	Gain2		3.96	4	4.04	V/V
G3	Gain3		5.94	6	6.06	V/V
G4	Gain4		7.82	8	8.08	V/V
$\text{PSRR}_{3/4}$	Power supply rejection ratio	$V_S$ to $\text{O}3/4$ decoupling capacitance is typically $4.7\text{ nF}$ on $\text{VCC5}$ and $\text{VCC3}$ .		80		dB
<b>Shift Buffer</b>						
VRI	Shift input voltage range		0.1		2.6	V
VRO	Shift output voltage range		0.1		2.6	V
$\text{VR}_{\text{offset}}$	Shift voltage offset		-5		5	mV
$I_{\text{RO}}$	Shift output current capability		-5		5	mA
$I_{\text{leak,RI}}$	Input leakage current RI	pin-to-ground			5	$\mu\text{A}$
<b>ADREF</b>						
$V_{\text{oxm}}$	Maximum DC voltage of $\text{O}1/2/3/4$ relative to ADREF	$\text{ADREF} = 3.3/5\text{ V}$ ; $\text{Ox-ADREF}$	-0.1	0.03	0.25	V
$V_{\text{oxos}}$	Overshoot of $\text{O}1/2/3/4$ over ADREF	$\text{Ox-ADREF}$ ; for $< 1\text{ }\mu\text{s}$ ; never higher than $5\text{ V}$ over GND Specified by design			1.2	V
$I_{\text{ADREF}}$	Bias current for voltage clamping circuit				100	$\mu\text{A}$
<b>Gate-Driver</b>						
$V_{\text{GS,low}}$	Gate-source voltage low high/low-side driver	Active pulldown, $I_{\text{load}} = -2\text{ mA}$	0		0.2	V

**ELECTRICAL CHARACTERISTICS (continued)**

over operating temperature  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  and recommended operating conditions,  $V_S = 4.75$  to  $30\text{ V}$ ,  $f_{\text{PWM}} < 30\text{ kHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\text{GSp}}$	Passive gate-source resistance		500			k $\Omega$
$R_{\text{GSsa}}$	Semi-active gate-source resistance	In sleep mode, $V_{\text{gs}} > 2\text{ V}$	7			k $\Omega$
$R_{\text{GSa2}}$	Active gate-source resistance	$V_{\text{gs}} < 1\text{ V}$ , gate driven low by gate-driver, Regyx = 100	2.3			$\Omega$
$R_{\text{GSa1}}$	Active gate-source resistance	$V_{\text{gs}} < 1\text{ V}$ , gate driven low by gate-driver, Regyx = 010	4.5			$\Omega$
$R_{\text{GSa0}}$	Active gate-source resistance	$V_{\text{gs}} < 1\text{ V}$ , gate driven low by gate-driver, Regyx = 001	9			$\Omega$
$V_{\text{GS,HS,high}}$	high-side output voltage	$I_{\text{load}} = -2\text{ mA}$	9	12.8		V
$V_{\text{GS,LS,high}}$	low-side output voltage	$I_{\text{load}} = -2\text{ mA}$	9	12.8		V
IGC2C	Gate charge current high/low-side driver 2	VGLS-VSLS = 2 V - 5 V, Regyx = 100, if not disabled in CFG1	0.46	0.57	0.69	A
IGC1C	Gate charge current high/low-side driver 1	VGLS-VSLS = 2 V - 5 V, Regyx = 010, if not disabled in CFG1	0.23	0.29	0.34	A
IGC0C	Gate charge current high/low-side driver 0	VGLS-VSLS = 2 V - 5 V, Regyx = 001, if not disabled in CFG1	0.11	0.14	0.17	A
IGD2D	Gate discharge current high/low-side driver 2	VGLS-VSLS = 2 V - 5 V, Regyx = 100, if not disabled in CFG1	0.46	0.57	0.69	A
IGD1D	Gate discharge current high/low-side driver 1	VGLS-VSLS = 2 V - 5 V, Regyx = 010, if not disabled in CFG1	0.23	0.29	0.34	A
IGD0D	Gate discharge current high/low-side driver 0	VGLS-VSLS = 2 V - 5 V, Regyx = 001, if not disabled in CFG1	0.11	0.14	0.17	A
$t_{\text{Don}}$	Propagation on delay time	After ILx/IHx rising edge	200			ns
$t_{\text{Dondif}}$	Propagation on delay time difference		50			ns
$t_{\text{Doff}}$	Propagation off delay time	After ILx/IHx falling edge	200			ns
$t_{\text{Doffdiff}}$	Propagation off delay time difference		50			ns
$T_{\text{Don\_Doff\_diff}}$	Difference between propagation on delay time and propagation off delay time		15			ns
$t_{\text{DRVoff}}$	Propagation off (DRVOFF) delay time	After rising edge on DRVOFF	200			ns
$t_{\text{ENoff}}$	Propagation off (EN) deglitching time	After falling edge on EN	6			$\mu\text{s}$
$t_{\text{SD}}$	Time until device enters shutdown	After falling edge on EN	20	35		$\mu\text{s}$
$t_{\text{RSTNoff}}$	Propagation off (RSTN) delay time	After falling edge on RSTN	200			ns
$A_{\text{dt}}$	Accuracy of dead time	If not disabled in CFG1	-15	15		%
<b>Boost Converter</b>						
$V_{\text{BOOST}}$	Boost output voltage	BOOST-VS voltage	14	15	16	V
$I_{\text{BOOST}}$	Output current capability	For device internal use only	40			mA
$f_{\text{BOOST}}$	Switching frequency	BOOST-VS > $V_{\text{BOOSTUV}}$ <sup>(1)</sup>	2.5			MHz
$V_{\text{BOOSTUV}}$	Undervoltage shutdown Level	BOOST-VS voltage	11	11.9		V
$t_{\text{BCSD}}$	Filter time for undervoltage shutdown		5	6		$\mu\text{s}$
$V_{\text{GNDLS\_B,off}}$	Voltage at GNDLS_B pin at which boost FET switches off due to current limit		80	100	120	mV
$t_{\text{SW,off}}$	Delay of the GNDLS_B current limit comparator		20			ns
$I_{\text{SW,fail}}$	Internal second level current limit		480	1100		mA

(1) During startup when  $\text{BOOST-VS} < V_{\text{BOOSTUV}}$ ,  $f_{\text{BOOST}}$  is typically 1.25 MHz.

**ELECTRICAL CHARACTERISTICS (continued)**

over operating temperature  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  and recommended operating conditions,  $V_S = 4.75$  to  $30\text{ V}$ ,  $f_{\text{PWM}} < 30\text{ kHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Digital Inputs</b>						
INL	Input low threshold	All digital inputs: EN, RSTN, B_EN, NCS, DRVOFF, ILSx, IHSx, CSM, SDI			0.9	V
INH	Input high threshold	All digital inputs: EN, RSTN, B_EN, NCS, DRVOFF, ILSx, IHSx, CSM, SDI	2			V
Inhys	Input hysteresis	All digital inputs: EN, RSTN, B_EN, NCS, DRVOFF, ILSx, IHSx, CSM, SDI	0.3	0.4	0.78	V
$R_{\text{pd,EN}}$	Input pull down resistor at EN pin	EN	170	200	300	k $\Omega$
$t_{\text{deg,ENon}}$	Power-up time after EN pin high from sleep mode to active mode	After rising edge on EN, time until logic out-of-reset			TBD	Ms
$R_{\text{pullup}}$	Input pull up resistance	RSTN, B_EN, NCS, DRVOFF	100	140	200	k $\Omega$
$R_{\text{pulldown}}$	Input pull down resistance	ILSx, IHSx, CSM, SDI	100	140	200	k $\Omega$
<b>Digital Outputs</b>						
OH	Output high voltage	All digital outputs: ERR, SDO, PHxC $I = \pm 2\text{ mA}$ ;	VDDIO -0.2			V
OL	Output low voltage	VDDIO in functional range <sup>(2)</sup>			0.2	V
<b>VDS Monitoring</b>						
$V_{\text{SCTH}}$	VDS short circuit threshold input range	If not disabled in CFG1	0		2.5	V
$A_{\text{vds}}$	Accuracy of VDS monitoring		-100		100	mV
$t_{\text{VDS}}$	Detection filter time	Only rising edge of VDS comparators are filtered		5		$\mu\text{s}$
<b>THERMAL SHUTDOWN</b>						
$T_{\text{msd0}}$	Thermal recovery	Specified by characterization	140	150		$^{\circ}\text{C}$
$T_{\text{msd1}}$	Thermal warning		160	170		$^{\circ}\text{C}$
$T_{\text{msd2}}$	Thermal global reset		175	190	205	$^{\circ}\text{C}$
$T_{\text{hmsd}}$	Thermal shutdown hysteresis			40		$^{\circ}\text{C}$
$t_{\text{TSD}}$	Thermal warning filter time		40	45	50	$\mu\text{s}$
$t_{\text{TSD}}$	Thermal shutdown filter time		40	45	50	$\mu\text{s}$
<b>Phase Comparator</b>						
$V_{\text{PCHth}}$	Phase comparator high threshold		$0.7 \cdot V_{\text{SH}}$		$0.8 \cdot V_{\text{SH}}$	
$V_{\text{PCLth}}$	Phase comparator low threshold		$0.2 \cdot V_{\text{SH}}$		$0.3 \cdot V_{\text{SH}}$	
$t_{\text{DHL}}$	Delay time high–low	$C_{\text{out}} = 50\text{ pF}$		30		ns
$t_{\text{DLH}}$	Delay time low–high	$C_{\text{out}} = 50\text{ pF}$		30		ns
$t_{\text{D,match}}$	Matching between two channels				50	ns
$R_{\text{VSH}}$	Resistance of internal voltage divider to ground		170		330	k $\Omega$
<b>VS Monitoring</b>						
$V_{\text{VS,OV}}$	Overvoltage shutdown level	If not disabled in CFG1	30		30.5	V
$V_{\text{VS,UV}}$	Undervoltage shutdown level		4.5		4.75	V
$t_{\text{VS,SHD}}$	Filter time for voltage shutdown		5		6	$\mu\text{s}$
<b>Serial Peripheral Interface Timing</b>						
$f_{\text{SPI}}$	SPI clock (SCLK) frequency				$4^{(3)}$	MHz
$T_{\text{SPI}}$	SPI clock period		250			ns
$t_{\text{high}}$	High time: SCLK logic high duration		90			ns
$t_{\text{low}}$	Low time: SCLK logic low duration		90			ns

(2) All digital outputs have a push-pull output stage between VDDIO and ground.

(3) MAX SPI clock tolerance is  $\pm 10\%$ .

### ELECTRICAL CHARACTERISTICS (continued)

over operating temperature  $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  and recommended operating conditions,  $V_S = 4.75$  to  $30\text{ V}$ ,  $f_{\text{PWM}} < 30\text{ kHz}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{sMCUs}}$	Setup time NCS: time between falling edge of NCS and rising edge of SCLK	90			ns
$t_{\text{d1}}$	Delay time: time delay from falling edge of NCS to data valid at SDO			60	ns
$t_{\text{susi}}$	Setup time at SDI: setup time of SDI before the rising edge of SCLK			30	ns
$t_{\text{d2}}$	Delay time: time delay from falling edge of SCLK to data valid at SDO	0		30	ns
$t_{\text{hcs}}$	Hold time: time between the falling edge of SCLK and rising edge of NCS	45			ns
$t_{\text{hlcs}}$	SPI transfer inactive time: time between two transfers	250			ns
$t_{\text{tri}}$	3-state delay time: time between rising edge of NCS and SDO in 3-state			15	ns

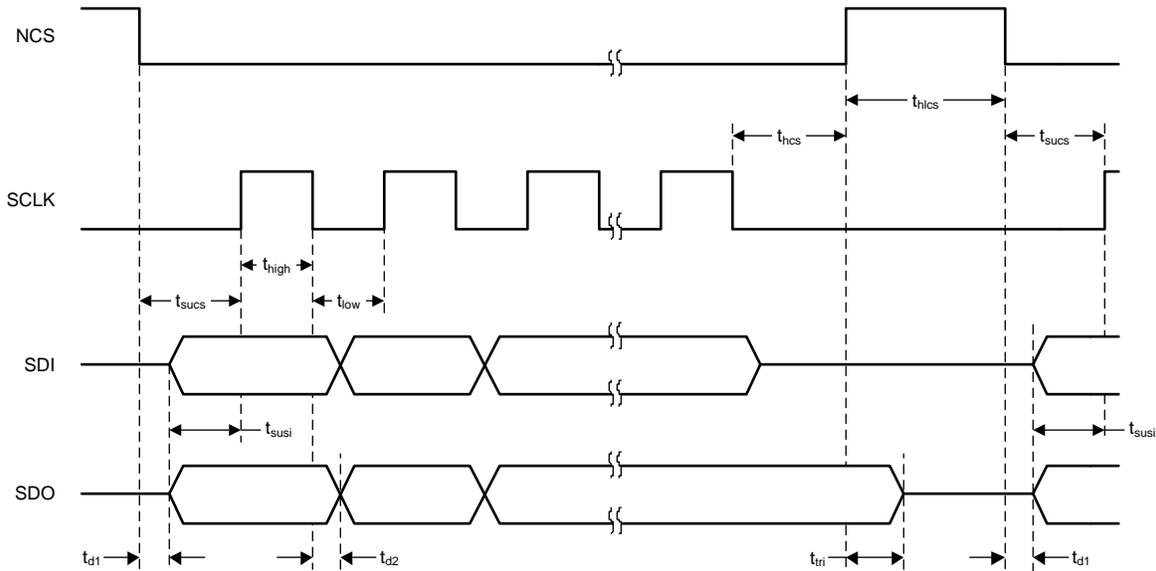


Figure 2. SPI Timing Parameters

PRODUCT PREVIEW

PIN FUNCTIONS

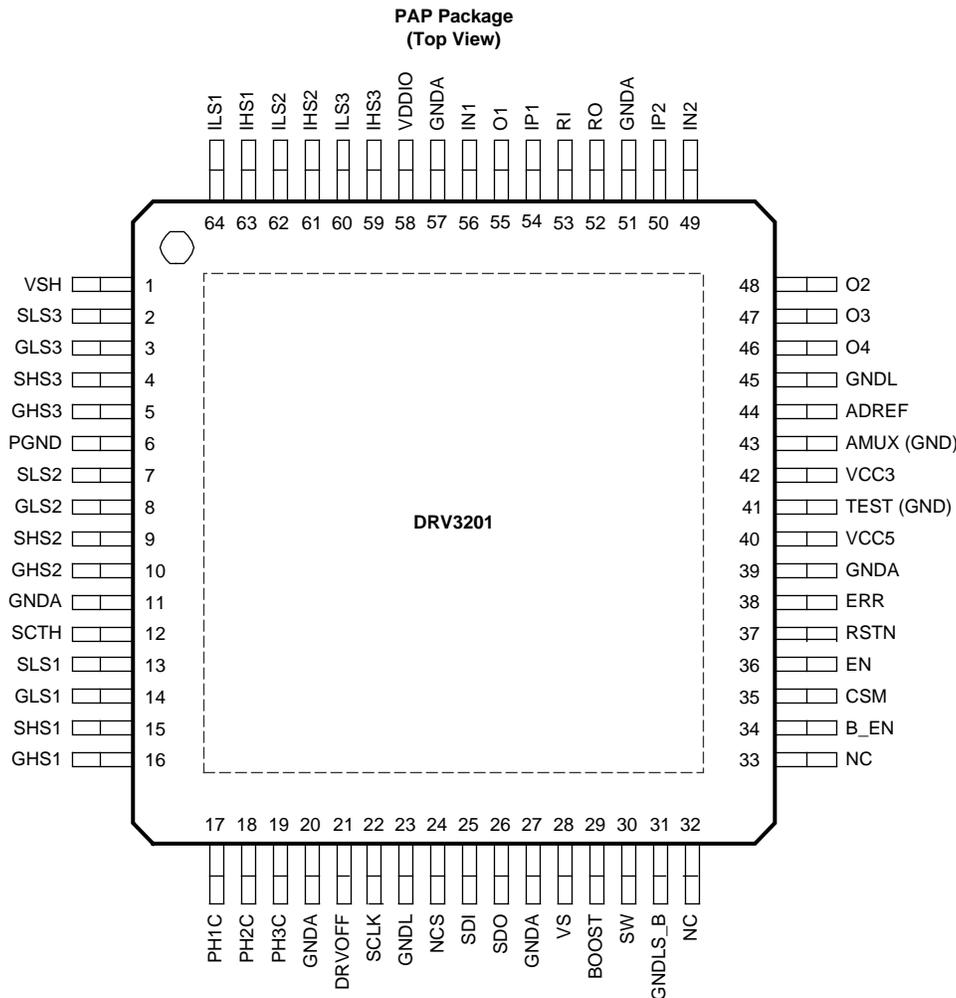


Figure 3. Pin Assignment (HTQFP-64 Package)

PIN FUNCTIONS

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
VSH	1	HVI_A	Sense high-side, sensing VS connection of the external power MOSFETs for VDS monitoring.
SLS3	2	PWR	Source low-side 3, connected to external power MOSFET for gate discharge and VDS monitoring.
GLS3	3	PWR	Gate low-side 3, connected to gate of external power MOSFET.
SHS3	4	PWR	Source high-side 3, connected to external power MOSFET for gate discharge and VDS monitoring.
GHS3	5	PWR	Gate high-side 3, connected to gate of external power MOSFET.
PGND	6	GND	Sense low-side (ground), sensing ground connection of the external power MOSFETs for phase comparators.
SLS2	7	PWR	Source low-side 2, connected to external power MOSFET for gate discharge and VDS monitoring.
GLS2	8	PWR	Gate low-side 2, connected to gate of external power MOSFET.
SHS2	9	PWR	Source high-side 2, connected to external power MOSFET gate discharge and VDS monitoring.
GHS2	10	PWR	Gate high-side 2, connected to gate of external power MOSFET.

(1) Description of pin type: GND = Ground, HVI\_A = High-Voltage Input Analog, HVI\_D = High-Voltage Input Digital, LVI\_A = Low-Voltage Input Analog, LVO\_A = Low-Voltage Output Analog, LVO\_D = Low-Voltage Output Digital, NC = NoConnect, PWR = Power Output, Supply = Supply Input.

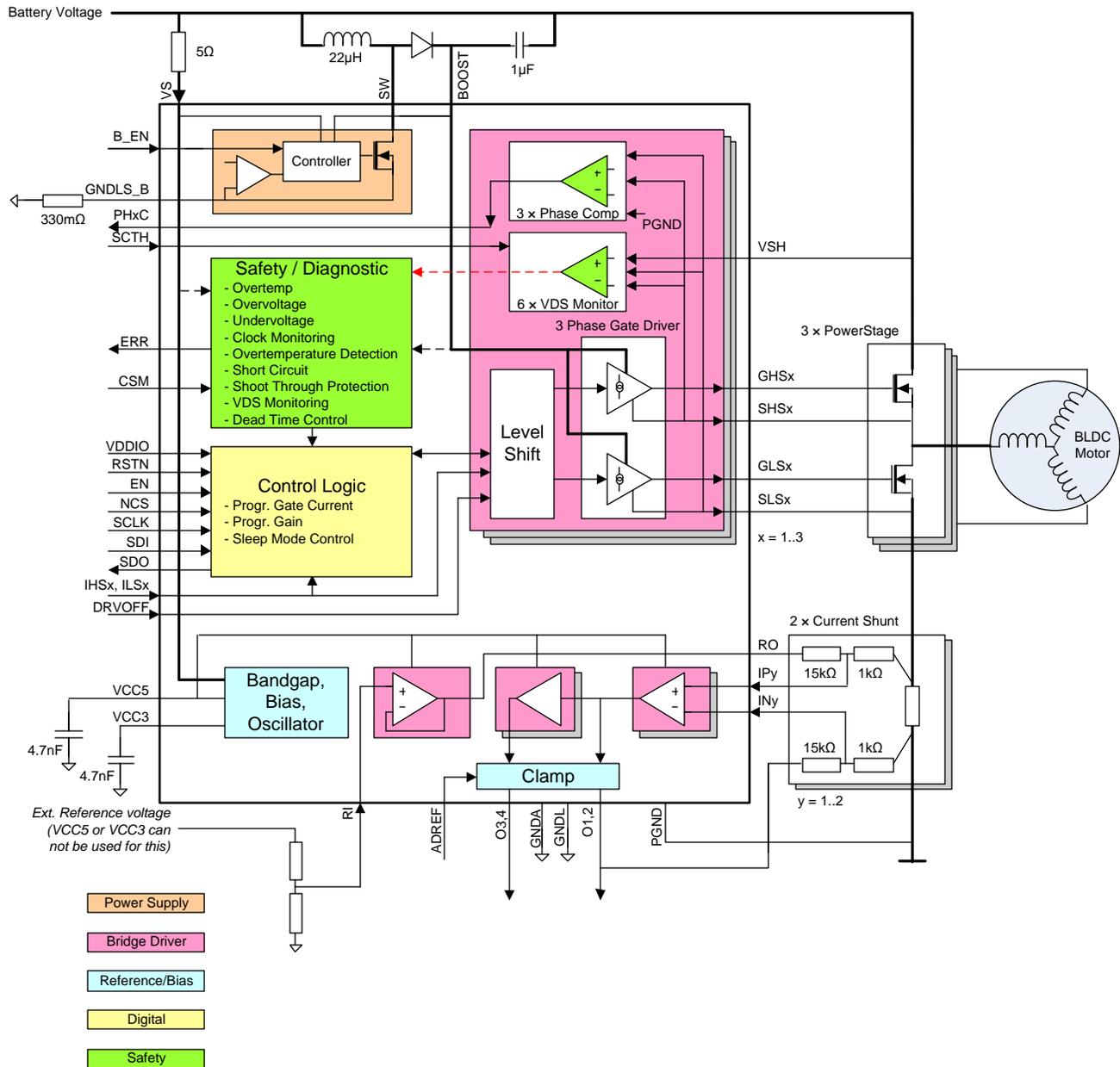
**PIN FUNCTIONS (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
GND_A	11	GND	Analog ground
SCTH	12	HVI_A	Short circuit threshold, reference input voltage for VDS monitoring.
SLS1	13	PWR	Source low-side 1, connected to external power MOSFET for gate discharge and VDS monitoring.
GLS1	14	PWR	Gate low-side 1, connected to gate of external power MOSFET.
SHS1	15	PWR	Source high-side 1, connected to external power MOS transistor for gate discharge and VDS monitoring.
GHS1	16	PWR	Gate high-side 1, connected to gate of external power MOS transistor.
PH1C	17	LVO_D	Phase comparator output1
PH2C	18	LVO_D	Phase comparator output2
PH3C	19	LVO_D	Phase comparator output3
GND_A	20	GND	Analog ground
DRVOFF	21	HVI_D	Driver OFF (high active), secondary bridge driver disable
SCLK	22	HVI_D	SPI clock
GNDL	23	GND	Logic ground
NCS	24	HVI_D	SPI chip select
SDI	25	HVI_D	SPI data input
SDO	26	LVO_D	SPI data output
GND_A	27	GND	Analog ground
VS	28	Supply	Power supply voltage
BOOST	29	Supply	Boost output voltage, used as supply for the gate-drivers.
SW	30	PWR	Boost converter switching node connected to external coil and external diode.
GNDL_B	31	GND	Boost GND to set current limit. Boost switching current goes through this pin via exterior resistor to GND.
NC	32	NC	NC pin, connected to GND during normal application.
NC	33	NC	NC pin, connected to GND during normal application.
B_EN	34	HVI_D	Boost enable. Enable boost operation or disable during e.g. sensitive measurement.
CSM	35	HVI_D	Configurable safety mode (high active), defines the level of safety.
EN	36	HVI_D	Enable (high active) of the device
RSTN	37	HVI_D	Reset (low active)
ERR	38	LVO_D	Error (low active). Error pin to indicate detected error.
GND_A	39	GND	Ground analog
VCC5	40	LVO_A	VCC5 regulator, for internal use only. Recommended external decoupling capacitance: 4.7 nF. External load < 100 $\mu$ A
TEST	41	HVI_A	TEST mode input, connected to GND during normal application.
VCC3	42	LVO_A	VCC3 regulator, for internal use only. Recommended external decoupling capacitance: 4.7 nF. External load < 100 $\mu$ A
AMUX (GND)	43	LVO_A	Analog TEST output MUX, connected to GND during normal application.
ADREF	44	LVI_A	ADC reference of MCU, used as maximum voltage clamp for O1-O4.
GNDL	45	GND	Logic ground
O4	46	LVO_A	Output second stage current sense amplifier 2
O3	47	LVO_A	Output second stage current sense amplifier 1
O2	48	LVO_AO	Output first stage current sense amplifier 2
IN2	49	HVI_A	Current sense input N 2
IP2	50	HVI_A	Current sense input P 2
GND_A	51	GND	Ground analog
RO	52	LVO_A	Current sense reference output for the shift voltage.
RI	53	HVI_A	Current sense reference input for the shift voltage.

**PIN FUNCTIONS (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IP1	54	HVI_A	Current sense input P 1
O1	55	LVO_A	Output first stage current sense amplifier 1
IN1	56	HVI_A	Current sense input N 1
GND A	57	GND	Ground analog
VDDIO	58	Supply	IO supply voltage, defines the interface voltage of digital I/O e.g. SPI.
IHS3	59	HVI_D	Input HS 3, digit input to drive the HS3
ILS3	60	HVI_D	Input LS 3, digit input to drive the LS3
IHS2	61	HVI_D	Input HS 2, digit input to drive the HS2
ILS2	62	HVI_D	Input LS 2, digit input to drive the LS2
IHS1	63	HVI_D	Input HS 1, digit input to drive the HS1
ILS1	64	HVI_D	Input LS 1, digit input to drive the LS1

FUNCTIONAL BLOCK DIAGRAM



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Figure 4. DRV3201-Q1 Functional Block Diagram

## DETAILED DESCRIPTION

The DRV3201-Q1 is designed to control 3 phase brushless DC motors in automotive applications using pulse width modulation. Three high-side and three low-side gate-drivers can be switched individually with low propagation delay. The input logic prevents simultaneous activation of high and low-side driver of the same channel. A configuration and status register can be accessed through the SPI communication interface.

### SUPPLY CONCEPT

The battery voltage functional operation range for the DRV3201-Q1 is between 4.75 V and 30 V. The DRV3201-Q1 operates with either 3.3 V or 5 V MCUs, which can be achieved by connecting the IO voltage of the MCU to the VDD\_IO pin of the DRV3201-Q1, and by connecting the ADC reference voltage of the MCU to the ADREF pin of the DRV3201-Q1. All digital outputs are related to VDDIO, and all analog outputs are related (clamped) to ADREF. All digital inputs are related to the internal supply VCC3, except the EN pin. The gate-drivers for the external power FETs operate down to 4.75 V battery voltage. For supply voltage falling below 4.75 V, the gates of the external FETs are pulled down actively. For supply voltage below 3 V, these gates are pulled down semi-actively. The minimum start-up battery voltage for the gate-drivers and the internal logic is 4.75 V.

Coming from full functional battery voltage range (i.e. between 4.7 V and 30 V) the internal logic, including the SPI interface, operates even during battery voltage drops down to 3 V. When the battery drops below 3 V, the DRV3201-Q1 triggers a complete internal reset, clearing all internal status bits and registers. Also, the SPI communication to the MCU is disabled when the DRV3201-Q1 logic is put in reset.

The VCC5 is an internal supply for the current sense amplifiers and other internal analog circuitry. The VCC5 pin needs to be externally decoupled with a typical 4.7 nF capacitance. The VCC5 has an internal current limit to avoid any internal damage due to an external short-to-ground on the VCC5 pin.

The VCC3 is an internal supply for the internal logic. The VCC3 pin needs to be externally decoupled with a typical 4.7 nF capacitance. Since the VCC3 is supplied from the VCC5 regulator, its output is current limited by the VCC5 current limit so any internal damage is avoided in case of an external short-to-ground on the VCC3 pin. In case of a short-to-ground on either the VCC5 pin or the VCC3 pin, the internal logic is put in reset, which is detectable by the MCU because of disabled SPI communication. In this situation it is strongly recommended that the MCU takes necessary action to bring down the EN pin and shut off the DRV3201-Q1 to avoid VCC5 and/or VCC3 overloading for too long.

### Boost Converter

The boost converter is configured to supply an add-on voltage to the supply voltage. The boost converter requires an external inductance, capacitor, Schottky-diode, and a series resistance in its ground for current sensing. Both the high-side and the low-side gate-drivers are supplied from the boost converter. This allows the DRV3201-Q1 to achieve full-range gate-source driving voltage for all external power FETs even at battery voltage down to 4.75 V. The boost converter has a separate B\_EN pin to enable/disable. When the device is put in sleep mode, the boost converter cannot be enabled.

### Sleep Mode/Active Mode

The EN (Enable) pin puts the device into sleep mode. At the falling edge on the EN pin, after a typical 6  $\mu$ s deglitch time, the gates of the external power FETs are actively pulled low by the gate-drivers. Afterwards (min 20  $\mu$ s, max 35  $\mu$ s later) the internal supplies VCC5, VCC3, the boost converter, and the current sense amplifiers are switched off and the gates of the external power FETs are pulled low with a semi-active pulldown resistor (see [Semi-Active Pull-Down Resistor](#)). The internal logic is put in reset state, and all internal registers are cleared. No diagnostic information is available during sleep mode.

A rising edge on the EN pin puts the device in active mode after TBD power-up time. In active mode, the supplies VCC5 and VCC3 are present, and the boost converter can be enabled or disabled with the B\_EN pin. Since all internal registers are cleared in sleep mode, the MCU must program the DRV3201-Q1 in the desired settings after each wake-up from sleep mode to active mode.

## DIGITAL INPUT/OUTPUT PINS

All digital input pins (marked HVI\_D in terminal function table), except the EN pin, have a threshold voltage related to the internal VCC3 supply. Therefore, the state of these input pins is effective regardless of whether the VDDIO level is out of limits. These digital input pins have a fail-safe ESD structure with only a reverse diode path to ground, and no reverse diode path to any supply voltage. Depending on the function, these input pins have an internal passive pulldown or pullup. All digital output pins (marked LVO\_D) have a push-pull stage between VDDIO and ground. Therefore, the logic high-levels are related to VDDIO.

## RESET

The DRV3201-Q1 can be reset by switching the RSTN to low. When RSTN is low, all status bits and register settings are cleared, the boost converter and the current sense amplifiers are off, and the gate-driver outputs are actively pulled low with the maximum setting for the sink current, hence turning off the external power FETs. The internal supplies VCC3 and VCC5 are still active when RSTN is forced low. The input high and low thresholds of RSTN are related to VCC3, and therefore independent of VDDIO, hence the state of the RSTN pin is effective regardless of whether the VDDIO level is out of limits.

## GATE-DRIVERS

The DRV3201-Q1 has three high-side and low-side gate-drivers. Each high-side and low-side gate-driver contains a programmable sourcing and sinking current to charge and discharge the gate of the external power FETs.

The digital logic prevents the simultaneous activation of high and low-side gate-driver of one power-stage. If a command from the MCU for simultaneous activation is detected, the failure is flagged in the status register.

### Gate-Driver Slope Control

The DRV3201-Q1 has been designed to support adaptive slope control by programmable sink and source currents to charge and discharge the gates of the external power FETs. [Table 1](#) gives the slope registers which are supported to program the sink and source currents of the gate-drivers.

**Table 1. Slope Configuration Registers**

Affected Gate-Drivers	Register	Slope	Current Range	Number of steps
HS1 & HS2	HS1/2 Slope Register (CURR0)	Rising Edge	140mA–1A	8
HS1 & HS2	HS1/2 Slope Register (CURR0)	Falling Edge	140mA–1A	8
LS1 & LS2	LS1/2 Slope Register (CURR1)	Rising Edge	140mA–1A	8
LS1 & LS2	LS1/2 Slope Register (CURR1)	Falling Edge	140mA–1A	8
HS3	HS3 Slope Register (CURR2)	Rising Edge	140mA–1A	8
HS3	HS3 Slope Register (CURR2)	Falling Edge	140mA–1A	8
LS3	LS3 Slope Register (CURR3)	Rising Edge	140mA–1A	8
LS3	LS3 Slope Register (CURR3)	Falling Edge	140mA–1A	8

To reduce the risk of a distorted slope due to changing the slope setting, a new slope setting for a rising edge only becomes active after the next falling edge of the affected gate-driver and vice versa for the falling edge. This does not apply directly after wake-up to active mode. As long as no low-side or high-side gate-driver has been switched after wake-up to active mode, the programmed slope settings are active immediately.

To allow a high scalability of the output FETs and switching speed, there is also one general reduced current mode setting, in which all gate charge/discharge currents are 25% of the programmed settings. Furthermore it is possible to set the drivers to switching mode by setting bit 7 in configuration register 1 (CFG1) to 1. In this setting the drivers are not current limited and limiting the switching speed can be done externally with resistors in the gate lines. In this mode it is strongly recommended to set the slope registers (CURR0–3) to 0x3F to get the maximum current setting and have the current limiting only from the external resistors.

### Direct Mode (6 x Inputs Operation)

The direct mode is the default operation mode after each wake-up from sleep mode to active mode. In direct mode, all gate-drivers can be controlled individually via the digital input pins IHSx/ILSx.

### PWM Mode (3 x Inputs Operation)

Alternatively, the gate-drivers can be operated in PWM mode by setting bit 6 in Configuration Register 1 (CFG1) to 1. PWM Mode controls all six gate-drivers with only three PWM signals. The valid controls in PWM mode are the IHSx inputs. The low-side controls are derived from the corresponding IHSx signals while all safety features remain active. In PWM mode, the ILSx inputs may be used as SPI-readable general purpose inputs.

### DRVOFF Gate-Driver Shutoff

When the DRVOFF pin is high, the gate-driver outputs are actively pulled low with the programmed setting for the sink current to turn off the external power FETs. Meanwhile, the IHSx/ILSx inputs can be read back through SPI. The VDS comparators, and flag errors (if VDS is too high) are enabled which can be used to ensure functionality of these blocks. The boost converter, the current sense amplifiers, and the internal VCC3 and VCC5 supplies are still active when DRVOFF is forced low. The input high and low thresholds of DRVOFF are related to VCC3, and are independent of VDDIO, so the state of the DRVOFF pin is effective regardless of whether the VDDIO level is out of limits.

### Active Pulldown

When the external power FETs need to be turned off and the DRV3201-Q1 is in active mode (either by normal control signal, DRVOFF signal, RSTN signal or by any error handling), the gate-drivers provide a low-ohmic active pulldown. Once the gate-source voltage of the power FETs reaches less than 2 V, the programmed current sink behavior changes into an  $R_{\text{dson}}$  behavior to increase the pulldown strength.

### Semi-Active Pull-Down Resistor

Each high and low-side driver has a typical 500 k $\Omega$  resistor from gate to source acting as passive pulldown to keep the external power FET turned off in unsupplied conditions. In addition a semi-active pulldown circuit is reducing the gate impedance at a typical voltage of 2 V to about 7 k $\Omega$ . This semi-active pulldown circuit is turned off in normal operation to avoid higher DC current consumption for the gate-driver.

### Gate-Driver Shutoff Paths

Table 2 summarizes the possible states of the EN, RSTN and DRVOFF pins and the effect on the gate-drivers.

**Table 2. Gate-Driver Shutoff Paths**

EN	RSTN	DRVOFF	Any Non-Masked Error	Gate-Driver Shutoff	Logic
Unpowered device <sup>(1)</sup>				Semi-active pulldown + passive pulldown	
0	X	X	X	Semi-active pulldown + passive pulldown	Reset

(1) For  $3\text{ V} < V_{\text{S}} < 4.75\text{ V}$ , the  $V_{\text{S}}$  undervoltage detection actively pulls down the gates of the external FETs. For  $V_{\text{S}} < 3\text{ V}$ , these gates are pulled down semi-actively.

**Table 2. Gate-Driver Shutoff Paths (continued)**

EN	RSTN	DRVOF F	Any Non-Masked Error	Gate-Driver Shutoff	Logic
1	0	X	X	Active pulldown	Reset
	1	1	X	Active pulldown	Enabled
		0	1 <sup>(1)</sup>	Active pulldown	Enabled
		0	0	Active, controlled by inputs	Enabled
1 ≥ 0	X	X	X	Active pulldown, afterwards device enters sleep mode ≥ semi-active pulldown + passive pulldown	Enabled during active pulldown, afterwards reset in sleep mode

## SAFETY

The DRV3201-Q1 has a wide range of safety features that helps the application to grant a high safety level.

### Monitored Errors

The following sections describe the monitored errors. The handling of these errors is described in [Configurable Safety Mode](#).

#### *Drain Source Voltage Monitoring*

The DRV3201-Q1 provides a drain-source voltage monitoring feature for each external power MOSFET. After input pin IHSx/ILSx goes high to turn on the external power MOSFET, its drain-source voltage is monitored. If this voltage stays higher than the VDS threshold for filter-time ( $t_{vds}$ ) then the error is raised and the status flag for this power MOSFET is set.

The internal VDS threshold for the VDS monitoring can be set by an external analog input level on the SCTH pin, and can be scaled in eight steps with a factor between 0 and 1 through SPI in configuration register 0 (CFG0), bits 5:3.

The VDS comparator configuration for each gate-driver is shown in [Figure 5](#). As shown in [Figure 5](#), the VSH pin is used as sense input voltage for the high-side VDS comparators. Externally, this VSH pin should be connected to the star-point of the positive supply of the power-stages.

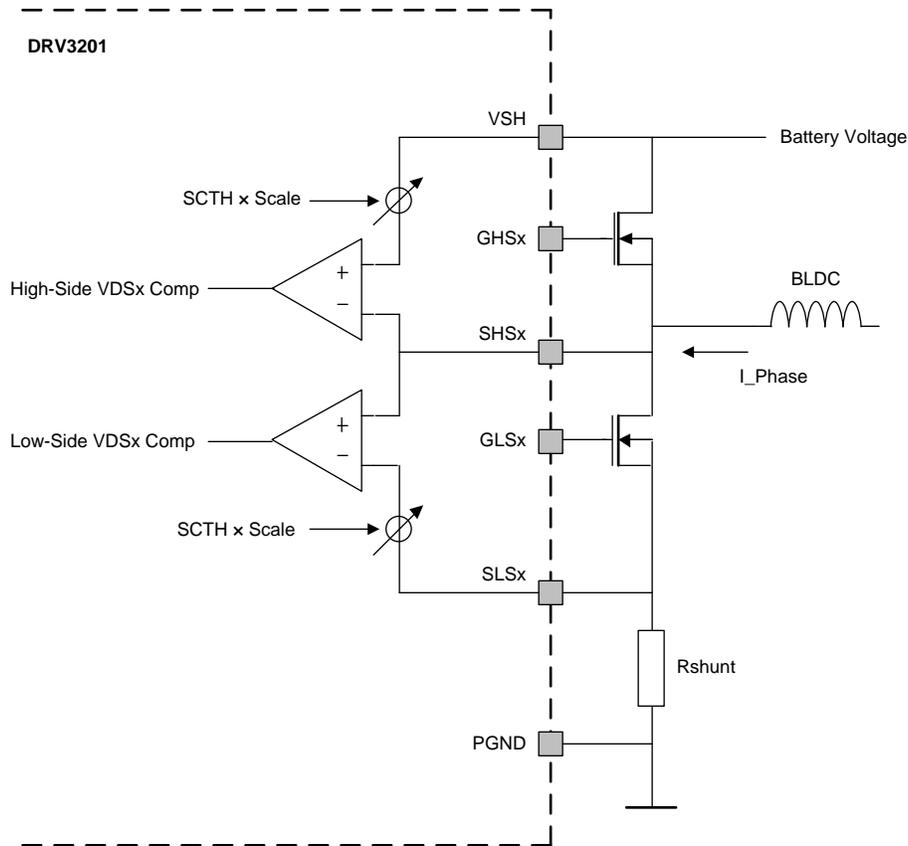
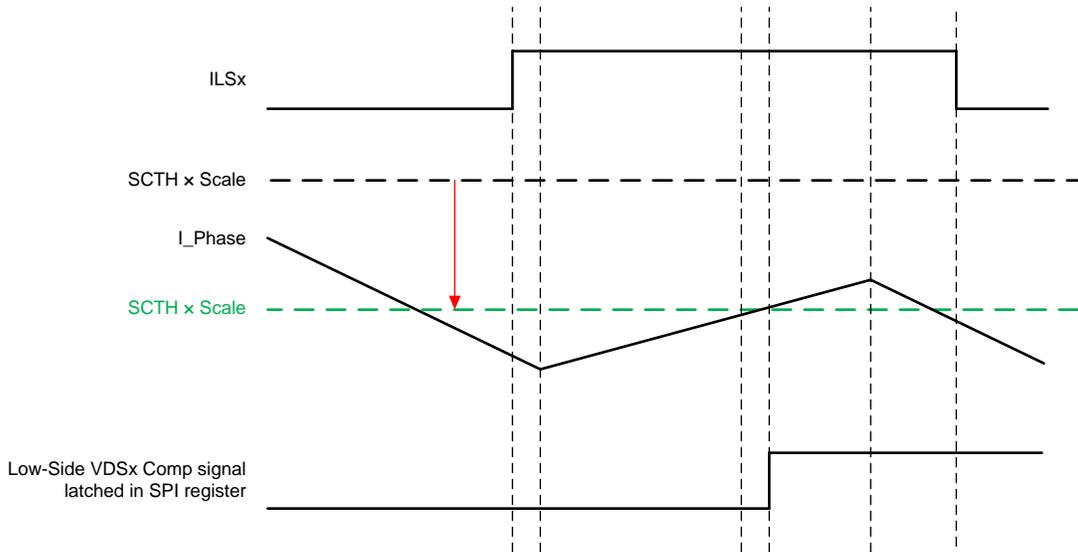


Figure 5. VDS Comparator Configuration for Each Driver-Stage

To verify the proper operation of the VDS comparators during normal operation, either the scale factor can be lowered through SPI, or the SPTH voltage can be externally lowered. This sets a lower VDS threshold (depending mostly on the random comparator offset  $< \pm 100$  mV) which causes the comparators to toggle at relative low current through the external power FETs (during normal operation without overcurrent). This is shown in Figure 6. During this verification, the error-handling of the VDS errors can be disabled as described in Configurable Safety Mode (configuration register 1 (CFG1), bits 3:4), such that the VDS errors are flagged in the SPI status register 0 (STAT0) and at the ERR pin only. The SPTH pin is a high-impedance input to a MOS gate with internal ESD protection to ground. There is no reverse pullup path present to any supply (fail-safe ESD structure).



**Figure 6. Checking VDS Comparators During Normal Operation (Low-Side Given as Example, Principle Also Applies to High-Side)**

**Shoot Through Detection and Programmable Dead Time**

The DRV3201-Q1 provides a mechanism that prevents both external MOSFETs of each power-stage from switching on at the same time connecting VS directly to GND. If the digital inputs try to force the device to switch on high-side and low-side gate-drivers of one power-stage, the error is raised in the status register and the bridges are switched according to [Figure 7](#).

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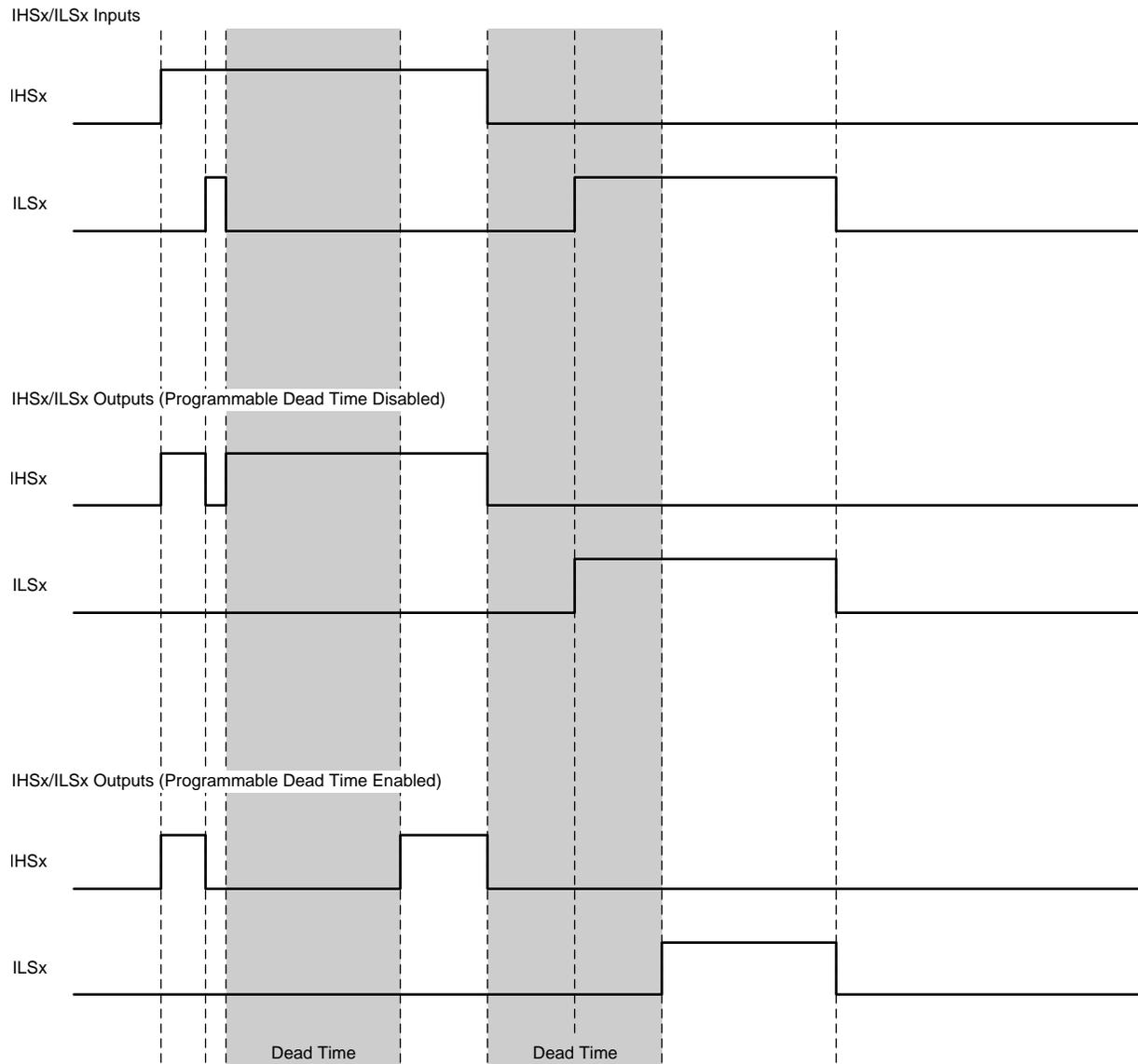


Figure 7. Driver Output During Input Failures

The dead time can be programmed in eight steps between 200 ns and 3000 ns in configuration register 0, bits 2:0. The programmed dead time is valid for all three power-stages. An internal 10 MHz oscillator is used as a time reference for creating the dead-time steps.

The dead time can be disabled in the configurable safety mode (see [Configurable Safety Mode](#)) when operating in direct mode. PWM mode does not support disabling the programmable dead time.

**Boost Undervoltage Error**

If the boost converter output voltage is below the undervoltage threshold level  $V_{VBOOST,UV}$  (11 V–11.9 V) for  $t_{BCSD}$  (5  $\mu$ s–6  $\mu$ s), the boost undervoltage flag is set accordingly in SPI status register 1 (STAT1). Depending on the configured safety mode (see [Configurable Safety Mode](#)), all gate-driver outputs are pulled low, and the ERR pin is pulled low.

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### VS Undervoltage Shutdown

If the VS voltage drops below the undervoltage threshold level  $V_{VS,UV}$  (4.5 V–4.75 V) for  $t_{VS,SHD}$  (5  $\mu$ s–6  $\mu$ s), the VS undervoltage flag is set in SPI status register 1 (STAT1), the gate-driver outputs are pulled low, and the ERR pin is pulled low. This happens regardless of the configured safety mode (see [Configurable Safety Mode](#)). The SPI interface works down to 3 V. Below 3 V on VS, internal reset occurs.

### VS Overvoltage Error

If the VS voltage exceeds the overvoltage threshold level  $V_{VS,OV}$  (30 V–30.5 V) for  $t_{VS,SHD}$  (5  $\mu$ s–6  $\mu$ s), the VS overvoltage flag is set in SPI status register 1 (STAT1). Depending on the configured safety mode (see [Configurable Safety Mode](#)), all gate-driver outputs are pulled low, and the ERR pin is pulled low.

### VS Comparator Check

The VS undervoltage and overvoltage comparators can be checked by using the loss of clock (LOC) test/VS comparator bit in configuration register 0 (CFG0). As long as this bit is set the comparators toggle and flag the undervoltage and the overvoltage at the same time. The error handling is active, so the bridges shut down and the ERR pin is pulled low. To reset the flags the LOC test /VS comparator bit needs to be reset and then the flags need to be read via SPI. After this, the ERR pin goes up again. This self-check is combined with the loss of clock self-test (see [Loss of Clock](#)).

### Overtemperature Warning and Shutdown

The thermal overload detection and protection of the device is based on five temperature sensors and two thresholds  $T_{msd1}$  (thermal warning) and  $T_{msd2}$  (thermal global reset):

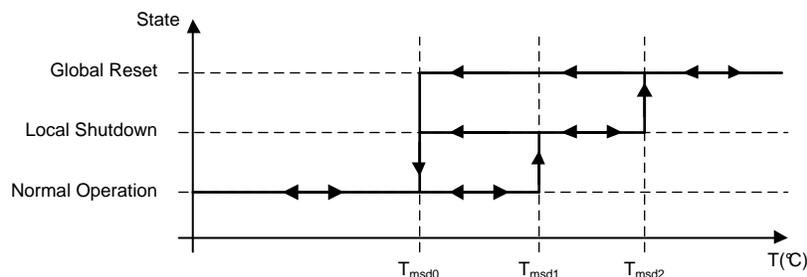


Figure 8. Thermal Shutdown

#### Normal operation of the device:

- Gate-drivers and boost converter are fully operational.

#### Thermal warning – overtemperature warning flag is set to 1:

- Thermal warning, stored in overtemperature warning bit in status register 0 (STAT0). This bit is reset after a read out of this register by the MCU.

#### Global reset - device in shutdown:

- An internal reset is generated.
- The boost converter is stopped.
- However, the temperature monitor block monitors the temperature and does not release the reset until the temperature drops below  $T_{msd0}$ .
- Thermal hysteresis avoids any oscillation between shutdown and restart.
- The overtemperature shutdown is filtered with  $t_{SHDOWN}$  (no unwanted shutdown by noise).

### SPI Error

If the DRV3201-Q1 receives an invalid write or read access, the SPI OK bit in status register 1 (STAT1) is set to 0. This bit is set to 1 after a read out of this register by the MCU.

### EEPROM CRC Check

After each wake up to active mode, the DRV3201-Q1 performs an EEPROM CRC check. If the calculated CRC8 checksum does not match the CRC8 checksum stored in the EEPROM, the EEPROM Data CRC Failed flag is set in status register 1 (STAT1).

### Configuration Data CRC Check

The DRV3201-Q1 offers a security feature to permanently ensure configuration integrity employing a CRC8 checksum mechanism. The MCU can start a CRC8 checksum calculation within the DRV3201-Q1 over all configuration registers by setting bit 0 in the CRC control register (CRCCTL) to 1. This bit stays set until the CRC calculation is finished. There may not be any write access while the CRC engine is running, otherwise the CRC8 checksum becomes corrupt. The CRC8 checksum value calculated by the DRV3201-Q1 is stored in the CRC calculated checksum register (CRCCALC).

The MCU itself can also calculate the expected CRC8 checksum value, based on the vector given below, and store this expected value in the CRC expected checksum register (CRCEXP). This should be done before the MCU initiates the CRC8 checksum calculation within the DRV3201-Q1. After the DRV3201-Q1 does the CRC calculation, if the expected CRC stored in the CRCEXP register does not match the calculated CRC in CRCCALC register, the Configuration Data CRC Failed flag is set in status register 1 (STAT1).

The MCU may then read back all configuration registers to search for the bit error and perform corrective actions.

The CRC8 calculation mechanism is a generic one with following presets:

- The polynomial used is: (0 1 2 8)
- Initial value is: 11111111

See [Table 3](#) for CRC data vector.

**Table 3. CRC Data Vector**

Bit Number	CRC8 Data Bus Values
[47:40]	CFG0
[39:32]	CFG1
[31:28]	CFG2
[27:22]	CURR0
[21:16]	CURR1
[15:10]	CURR2
[ 9: 4]	CURR3
[ 3: 0]	0000

### Loss of Clock

If the internal clock gets stuck, the loss of clock monitor pulls the ERR pin low. During a test of this block the ERR is also low. This self-check is combined with the VS comparator self-test (see [VS Comparator Check](#))

### Configurable Safety Mode

The DRV3201-Q1 can work in two different safety modes controlled by the external pin CSM, as described in [Table 4](#). This pin can be read back via SPI register RB0.

**Table 4. Safety Modes**

CSM	Description
LOW	Full safety mode: All internal protection features are activated.

**Table 4. Safety Modes (continued)**

CSM	Description
HIGH	Configurable safety mode: Protective actions as selected in configuration register CFG_REG_1 are enabled and they set diagnostic flags, deselected actions only set diagnostic flags without protective action. With this mode the device can be used outside the normal operation range but below Absolute Maximum Range (see <a href="#">ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup></a> ) under responsibility of user.

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal, unless otherwise specified.

Table 5 defines the protective actions taken on certain error conditions. When the device is in full safety mode, all internal protection features are activated, and all protective actions listed below are taken if the respective error condition is detected. When the device is in configurable safety mode (CSM), the error conditions for which CSM is available, the protective action and ERR pin indication (see [Error Indication on ERR Pin](#)) can be configured with the corresponding bit in CFG1. The diagnostic flags are always set if the respective error condition is present, regardless of the CSM setting.

**Table 5. Error Conditions and Protective Actions**

Error Condition	Protective Action	Recovery	Selectable Through CFG_REG_1 in CSM	Error Indication ERR Pin
VS undervoltage	Switch all gate-driver outputs to low (active pulldown)	Flags are cleared with MCU reading the status register or through RESET. If the failure remains after read out of the register, it is immediately be reported again.	No	Always
VS overvoltage			Yes	Selectable by CFG_REG_1
Boost converter undervoltage			Yes	
HS VDS error			Yes	
LS VDS-error			Yes	
Programmable dead time window failure	Enforce programmable dead time		Yes	
Shoot through protection violated	Switch high-side and low-side gate-driver outputs of affected power-stage to low (active pulldown). If enabled, enforce dead time to high-side and low-side.		No	Always
SPI error	SPI command is ignored		No	None
Configuration data CRC error	Reported via SPI		No	None
EEPROM data CRC error		No	None	
Overtemperature first threshold			No	Always
Overtemperature second threshold	Shutdown of device	After thermal recovery device performs power on reset	No	Always
LOC error	ERR pin low		No	Always

**Error Indication on ERR Pin**

The ERR pin is an indicator for a detected error condition. It may act as interrupt to the external MCU, after which the MCU reads all status registers to determine which error condition is detected. After entering active mode this pin remains high as long as no error condition is detected, in case of a detected error condition the ERR pin goes low. Error reporting occurs according to [Table 6](#).

**Table 6. Error Reporting in the Safety Modes**

CSM	ERR pin configuration (CFG1)	Description
LOW	Do not care	All error conditions are flagged on ERR pin

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**Table 6. Error Reporting in the Safety Modes (continued)**

CSM	ERR pin configuration (CFG1)	Description
HIGH	1	ERR pin only shows errors for protective actions that are enabled in CSM
	0	All error conditions are flagged on ERR pin

The ERR pin goes up again after a read out of the respective error flag in the status register once the respective violation condition disappears. In case the MCU reads out the respective error flag in the status register while the respective error condition is still present, the ERR pin shows a short positive pulse (pulse width typically 100 ns).

This behavior helps show the distinction between a loss of clock error and a VS undervoltage or overvoltage error flag during self-tests of these safety features. After activation of these self-tests in configuration register 0 (CFG0) bit 6, the ERR pin goes down. After an MCU read out of the VS undervoltage/overvoltage flags in status register 1 (STAT1) bits 1:0, the ERR pin should stay low if the loss of clock self-test is working properly. If the ERR pin shows a positive pulse (pulse width typically 100 ns), this is an indication of a failure in the loss of clock self-test.

### Additional Safety Features

#### *IHSx/ILSx Input Readback/Edge Counter*

To verify the signal path to the DRV3201-Q1, the device allows reading back the logic level of all IHSx and ILSx inputs from the RB0 address. These values directly reflect the state of the pin and are not registered. It is required to ensure that the state of the IHSx and ILSx pins do not change while reading back their levels via SPI.

IHSx/ILSx Input Readback remains operational even if PWM Mode is chosen. In this case the ILSx Readback may be used to read any logic level signal.

The edge counter allows a more robust and less time critical verification of the ILSx/IHSx signal chain and may be more convenient to use during normal operation. This counter can be used to count the number of edges on one or more IHSx/ILSx inputs. The MCU selects the inputs to be observed and arms the counter by writing to the SPI register RB1. When the start bit is removed the counter stops counting edges. The obtained counter value can be read from the SPI register RB2 and it resets by setting the CLEAR bit in SPI register RB1.

When the counter has reached its maximum value of 255 it stops counting and remains in this state.

IHSx/ILSx edge counter remains operational even if PWM Mode is chosen, and in this case it may be used to count edges at any connected input.

#### *Gate-Source Voltage Monitoring*

The DRV3201-Q1 provides a gate-source voltage monitoring feature for the external MOSFETs. For each external MOSFET, the VGS is monitored by a comparator with 1 V as a lower threshold, and 9 V as a higher threshold.

For each external MOSFET, a status flag is set in SPI status register 2 (STAT2), bits 0:5. Each status bit is set to 1 when the respective VGS rises above 9 V and they are set to 0 when the respective VGS drops below 1 V. This feature is intended for diagnostic use after startup to turn on/off the external MOSFETs and check the respective status bits.

#### **Ultima Ratio Support**

Under certain circumstances it may be required to turn on all FETs simultaneously, which is supported by this device. However, to minimize risk of accidental triggering two requirements need to be satisfied:

1. The MCU is required to perform an unlock sequence of three different consecutive SPI transfers.
2. When the last SPI command is sent all IHSx and ILSx inputs need to be at a high level already.

This feature is only available when operating in direct mode.

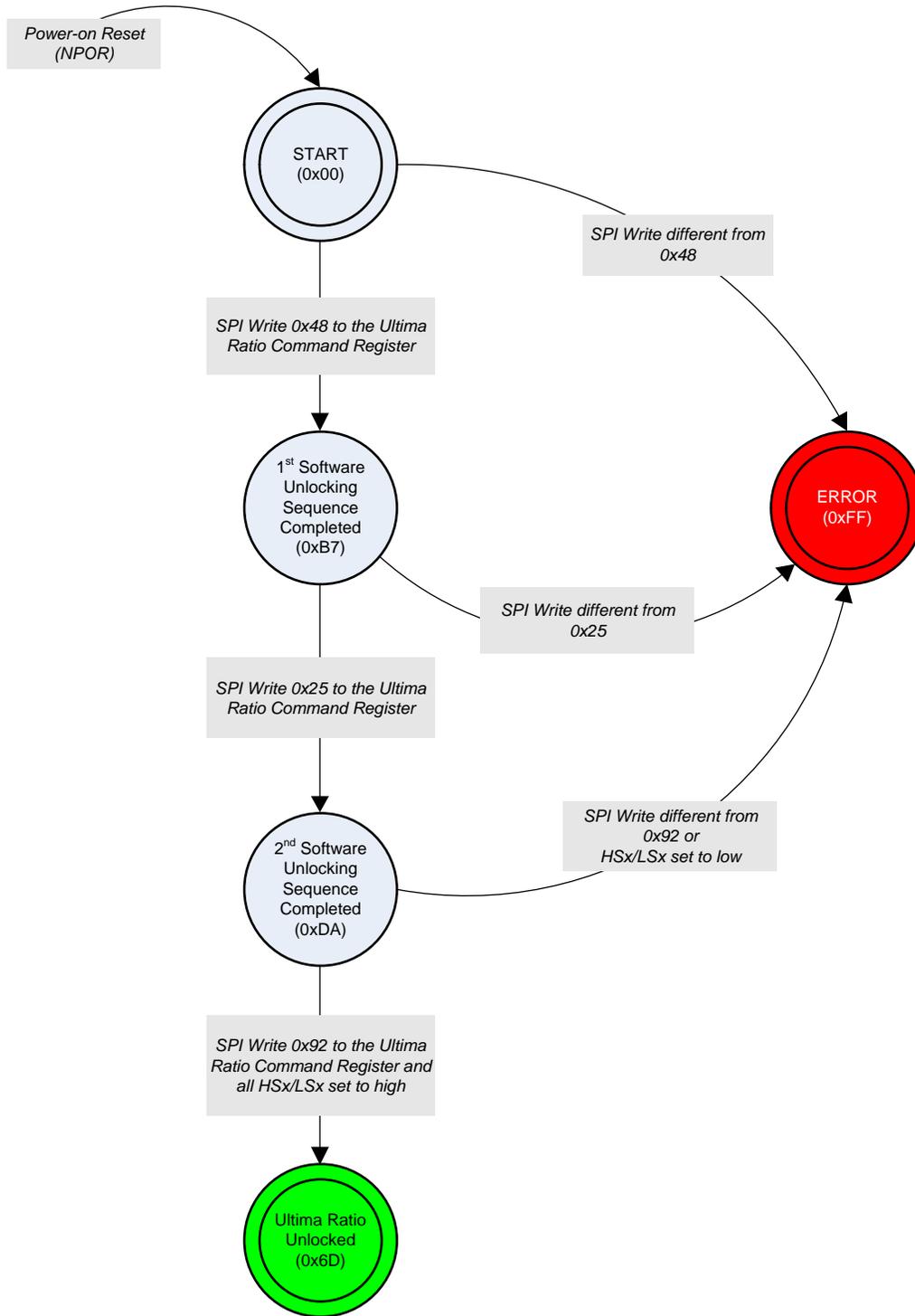


Figure 9. State Diagram for Unlocking Ultima Ratio

**CURRENT MEASUREMENT**

The two channel current measurement is measured by the voltage drop across two external shunt resistors. It contains one shift buffer, two first and two second stages.

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### Shift Buffer

The DRV3201-Q1 offers a unity gain amplifier that is normally used to support a shift voltage with lower output impedance. This allows each current sense path to handle negative common-mode voltages across the external shunt resistor. The shift voltage is applied externally on the RI pin, with the actual shift voltage buffered on the RO pin.

The RI input pin is a high-impedance input to a MOS gate with internal ESD protection to ground. There is no reverse pullup path present to any supply (fail-safe ESD structure).

### Two First Stage Amplifiers

A first stage operational amplifier operates with an external resistor network for higher flexibility to adjust the current measurement to the application requirements.

In the recommended application, a shift voltage that may be based on an external reference (e.g. an external voltage regulator) can be added to move the transfer curve. Each channel of the first amplifier has its own output going to the input of the MCU ADC.

The input of the first stage is high voltage compatible, so the device can be used to measure the voltage drop across the low-side MOSFET for low requirement applications. The maximum output voltage of the O1 and O2 pins is clamped to the ADREF voltage.

The input pins INx and IPx pin are high-impedance inputs to a MOS gate with internal ESD protection to ground. There is no reverse pullup path present to any supply (fail-safe ESD structure).

### Two Second Stage Amplifiers

The second stage amplifiers with a separately programmable gain enable a higher resolution measurement at low current. They can be directly connected to inputs of the MCU ADC.

The gain of the second stage amplifiers is programmable by SPI in steps two, four, six and eight using the CFG2 register.

The maximum output voltage of the O3 and O4 pins is clamped to the ADREF voltage.

### ADREF Voltage Clamp

The maximum output voltage of pins O1–O4 is clamped to the voltage applied to ADREF by an active clamp. The ADREF voltage is the reference supply voltage for the ADC in the MCU, so the outputs O1–O4 have a maximum signal range related to the input range of the ADC in the MCU. The active clamp consumes a maximum of 100  $\mu$ A from the ADREF pin.

### Current Sense Application Circuit

The standard configuration for the current sense amps are given in [Figure 10](#).

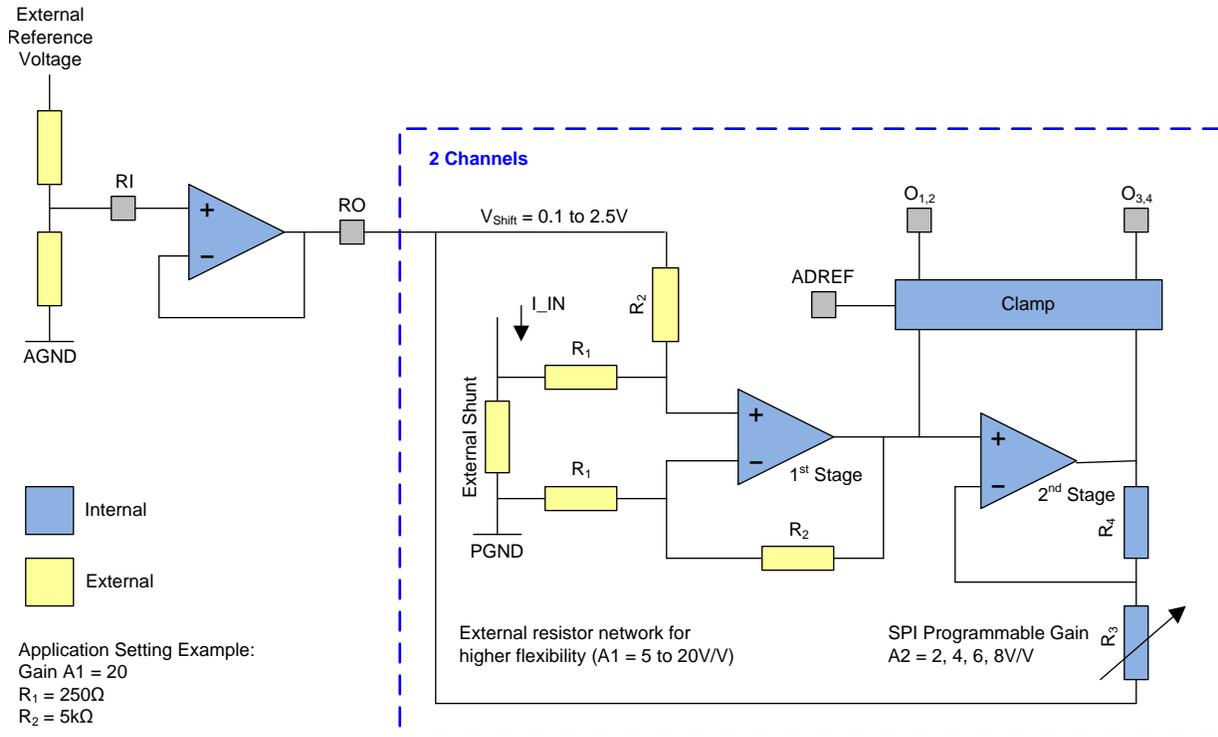


Figure 10. Application Circuit for Current Sense

The output voltage at O1/2 is: 
$$O_{1/2} = I_{RS} \frac{R_2}{R_1} + V_{RO}$$

The output voltage at O3/4 is: 
$$O_{3/4} = g \times (O_{1/2} - V_{RO}) + V_{RO}$$
 where g is the SPI adjusted gain in the second stage.

**PHASE COMPARATORS**

The device contains three real time phase comparators usable for sensorless commutation and diagnostics. Each comparator is switching at typically 75% and 25% of the supply voltage, and has an individual digital output going to the MCU. The phase comparators are always active as long as EN is high.

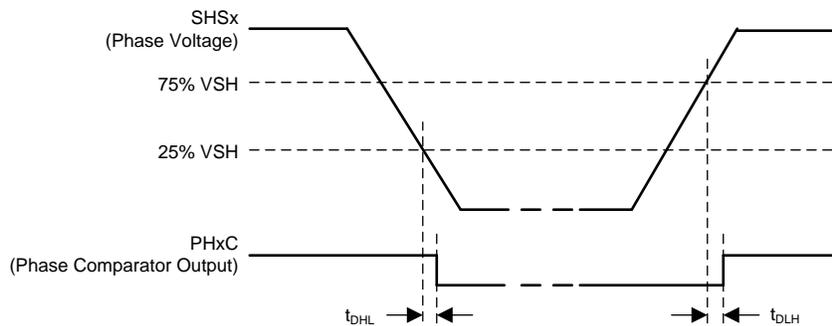


Figure 11. Phase Comparator Rise and Fall Thresholds

**Phase Comparators Application Diagram**

The phase comparator configuration is given in Figure 12.

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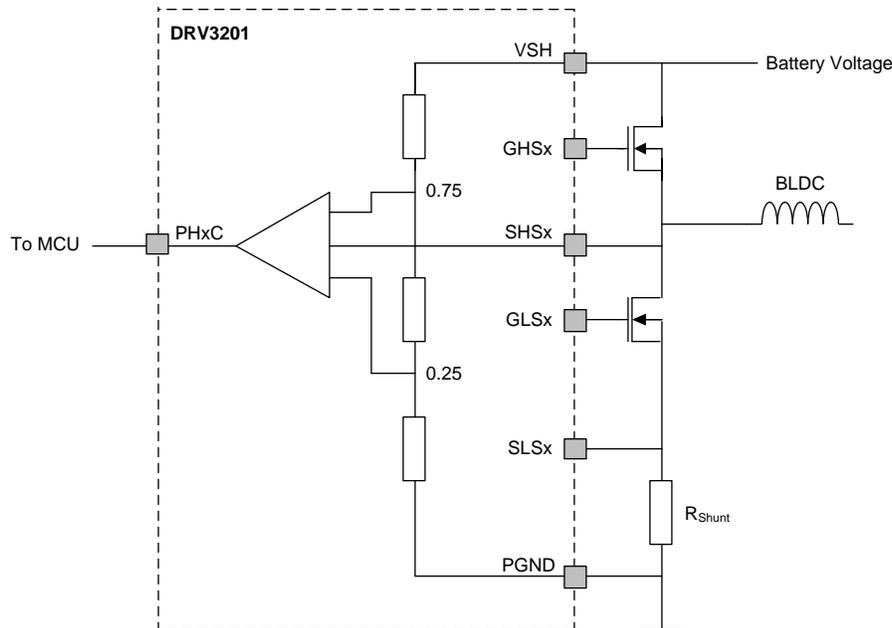


Figure 12. Application Diagram for Phase Comparators

The phase comparators allow:

- Real time observation of the phase switching on node SHSx
- Measurement of the time between the Input IHSx/ILSx and the phase comparator output PHxC
- Verification of time drift in previous measurements and/or other driver-stages

As Figure 12 shows, the VSH and PGND pins are used as sense inputs to create the high-side and low-side threshold levels for the phase comparators. Connect the VSH pin externally to the star-point of the positive supply of the power-stages. The PGND pin is to be connected to the power-ground star-point of the power-stages. The total resistance of the internal voltage divider is typically 248 k $\Omega$ .

## BOOST CONVERTER

The boost converter is based on a burst mode fixed frequency controller. During the on-time, the internal low-side boost FET is turned on until the current limit level is detected. The off-time is calculated proportionally from an independent 2.5 MHz time-reference by sensing the supply voltage VS and the output voltage VBOOST. A hysteretic comparator (low-level VBOOST-VS = 14 V, high level VBOOST-VS = 16 V) determines starting/stopping the burst pulsing. The nominal switching frequency during the burst pulsing is 2.5 MHz.

The maximum current in the coil can be adjusted by the resistor Rboost\_shunt such that the maximum coil current is limited to 0.1 V/Rboost\_shunt. This current limit is used by the controller to switch off the internal low-side boost FET. It is recommended to choose a coil with a current saturation level of at least 30% above the current limit level set with the resistor Rboost\_shunt.

A second internal current limit is implemented that triggers at higher currents and acts as a second level of protection for the internal low-side boost FET in case the resistor R1 is shorted. If the Rboost\_shunt is shorted, the second current limit is used by the controller to switch off the internal low-side boost FET. Since the second internal current limit is higher than the normal current limit set by Rboost-shunt and only meant for protecting the internal boost FET, the external coil may saturate if the second internal current limit becomes active. To allow the external MCU to detect this possible failure condition, the second internal current limit sets the boost undervoltage flag (register STAT1, bit 2). This causes a shutdown of the gate-drivers depending on the configured safety mode.

To reduce noise level on the chip the boost converter can be switched off during sensitive current measurements with the B\_EN pin. As long as the disable time interval is short enough, the boost output capacitor can keep the boost output voltage high enough. When the boost converter is disabled, the boost undervoltage monitor is active to ensure the driver-stages are still operating correctly. During the boost undervoltage condition, the boost switching frequency folds back to around half the normal operating frequency. This does not affect the current limit.

**Application Circuit for Boost Converter**

The recommended application for the boost converter is given in Figure 13. For the best performance, a Schottky diode and a 22 μH coil is required. The current limit for the internal FET (and the maximum current in the coil) can be adjusted and in the recommended application it is set to  $0.1 \text{ V}/0.33 \Omega = 300 \text{ mA}$ .

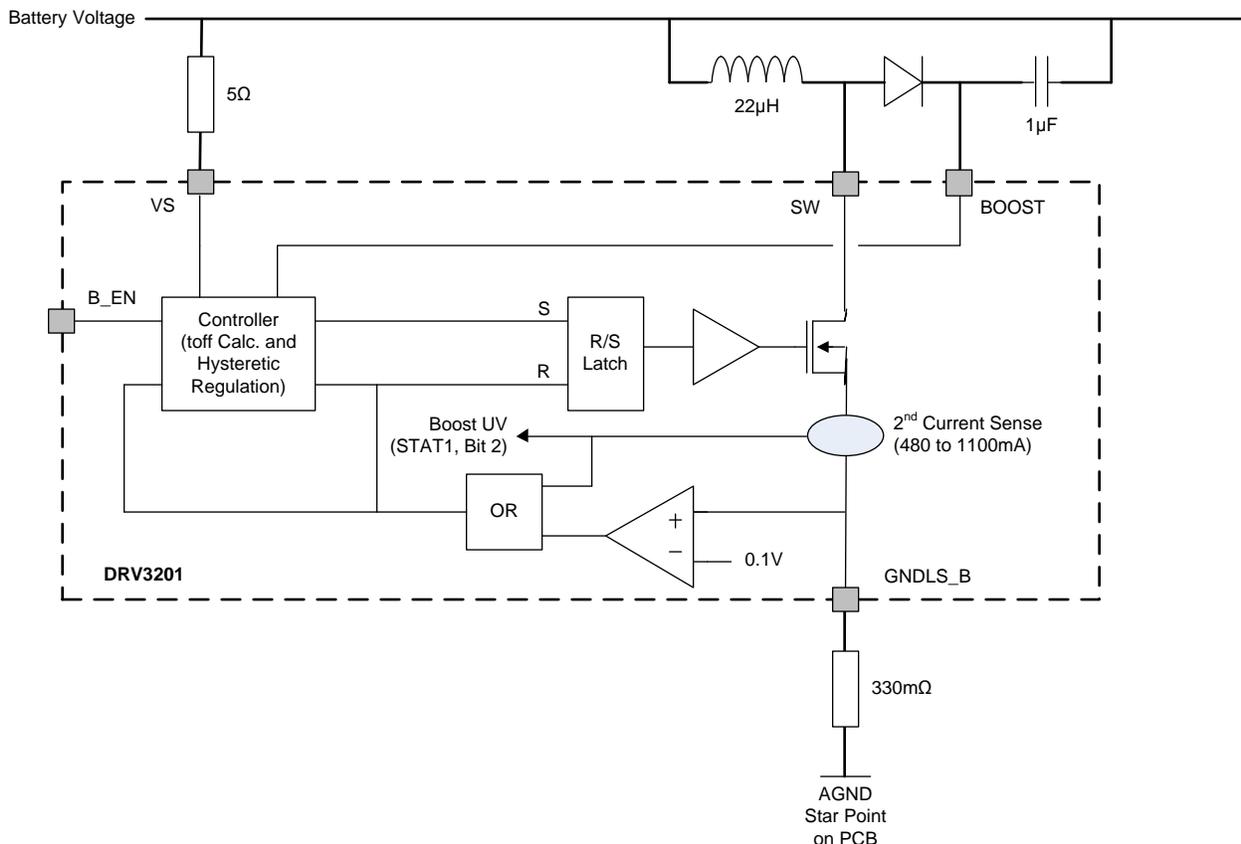


Figure 13. Recommended Application Circuit for Boost Converter

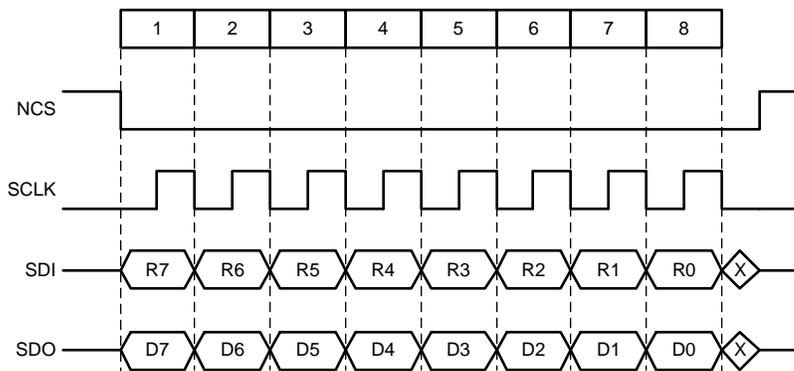
**SPI INTERFACE**

The SPI slave interface is used for serial communication with external SPI master (external MCU). The SPI communication starts with the NCS falling edge, and ends with NCS rising edge. The NCS high level keeps SPI slave interface in reset state, and SDO output 3-stated.

**Address Mode Transfer**

The address mode transfer is an 8-bit protocol. Both SPI slave and SPI master transmit the MSB first.

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NOTE: SPI Master (MCU) and SPI Slave (DRV3201) sample received data on the falling SCLK edge, and transmit on rising SCLK edge

Figure 14. Single 8-bit SPI Frame/Transfer

After the NCS falling edge, the first word of 7 bits are address bits followed by the RW bit. During the first address transfer, the device returns the STAT1 register on SDO. Each complete 8-bit frame is processed. The bits are ignored if NCS goes high before a multiple of 8 bits is transferred.

**SPI Address Transfer Phase**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	RW

FIELD NAME	BIT DEFINITION
ADDR [6:0]	Register Address
RW	RW = 1: Write access
	RW = 0: Read access

When RW = 0, the SPI master performs a read access to the selected register. During the following SPI transfer, the device returns the requested register read value on SDO, and interprets SDI bits as a next address transfer. When RW = 1, the master performs a write access on the selected register. The slave updates the register value during the next SPI transfer (if followed immediately) and returns the current register value on SDO.

**SPI Data Transfer Phase**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

FIELD NAME	BIT DEFINITION
DATA [7:0]	Data value for write access (8-bit)

The table shows a data value encoding scheme during a write access. It is possible to mix the two access modes (write and read access) during one SPI communication sequence (NCS = 0). The SPI communication can be terminated after a single 8-bit SPI transfer by asserting NCS = 1. The device returns STAT1 register (for the very first SPI transfer after power-up) or current register value addressed during the SPI transfer address phase.

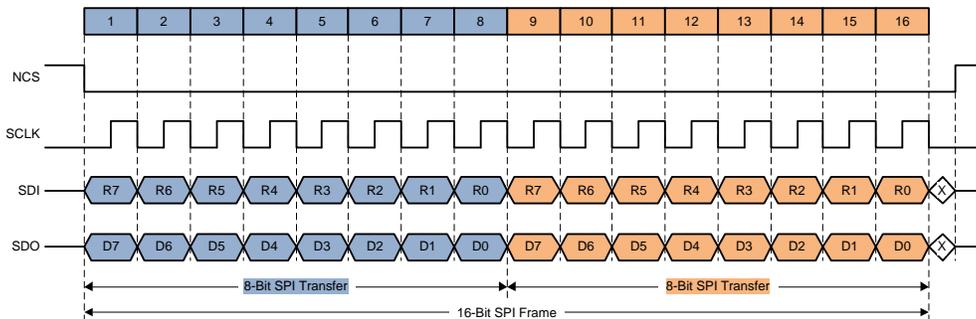
**Device Data Response**

Bit	R7	R6	R5	R4	R3	R2	R1	R0
Function	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

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FIELD NAME	BIT DEFINITION
REG [7:0]	Internal register value

All unused bits are set to zero.



NOTE: SPI Master (MCU) and SPI Slave (DRV3201) sample received data on the falling SCLK edge, and transmit on rising SCLK edge

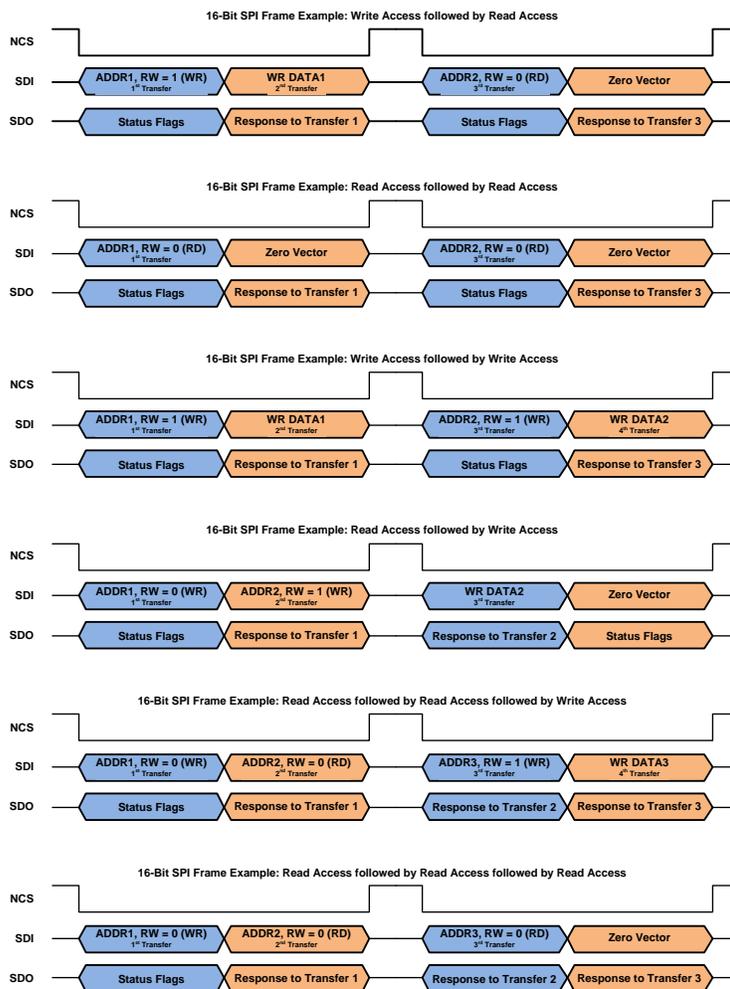


Figure 15. SPI Frame examples

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**Register Address Map**

Address	Name	RW	Reset Value
0x00	Reserved		
0x01	Configuration Register 0 (CFG0)	RW	8'h3F
0x02	Configuration Register 1 (CFG1)	RW	8'h3F
0x03	Configuration Register 2 (CFG2)	RW	4'h0
0x04	HS1/2 Slope Register (CURR0)	RW	6'h3F
0x05	LS1/2 Slope Register (CURR1)	RW	6'h3F
0x06	HS3 Slope Register (CURR2)	RW	6'h3F
0x07	LS3 Slope Register (CURR3)	RW	6'h3F
0x08-0x0F	Reserved		
0x10	Status Register 0 (STAT0)	RO	8'h00
0x11	Status Register 1 (STAT1)	RO	8'h00
0x12	Status Register 2 (STAT2)	RO	6'h00
0x13-0x1F	Reserved		
0x20	CRC Control Register (CRCCTL)	RW	1'h0
0x21	CRC Calculated (CRCCALC)	RO	8'h0
0x22	CRC Expected (CRCEXP)	RW	8'h0
0x23	HS/LS Read Back (RB0)	RO	6'h0
0x24	HS/LS Count Control (RB1)	RW	6'h0
0x25	HS/LS Count (RB2)	RO	8'h0
0x26-0x2F	Reserved		
0x30	Ultima Ratio Command (UR)	RW	8'h0
0x31-7F	Reserved		

**Detailed Register Definitions**
**Table 7. Configuration Register 0 (CFG0) (Addr. 0x01)**

Bits	R/W	Reset	Definition
7	RW	1'h0	Current capability 1: Reduced current mode (all gate charge/discharge currents are 25%) 0: Full current mode
6	RW	1'h0	Loss of clock detection test/VS comparator test If this bit is set, the clock for LOC monitor is permanently set to high. Additionally, the VS comparators show a VS undervoltage and a VS overvoltage at the same time in status register 1 (STAT1), bits 1:0. Both LOC and VS undervoltage/overvoltage are indicated on the ERR pin. A way to distinguish between LOC and VS undervoltage/overvoltage is described in <a href="#">VS Comparator Check</a> . Once the bit is cleared, the error-flag disappears after read out.
5:3	RW	3'h7	VDS monitoring scale factor VSCTH/VDS threshold 000: 0 001: 1/7 010: 2/7 011: 3/7 100: 4/7 101: 5/7 110: 6/7 111: 1 (Voltage follower)
2:0	RW	3'h7	Programmable dead time 000: 200-300 ns 001: 300-400 ns 010: 500-600 ns 011: 900-1000 ns 100: 1400-1500 ns 101: 1900-2000 ns 110: 2400-2500 ns 111: 2900-3000 ns

**Table 8. Configuration Register 1 (CFG1) (Addr. 0x02)**

Bits	R/W	Reset	Definition
7	RW	1'h0	0: Adjustable HS/LS currents for rising/falling edges according to registers CURR0–3 1: Unlimited HS/LS currents for rising/falling edges
6	RW	1'h0	Set PWM mode All gate-drivers can be driven with 3 PWM signals
5	RW	1'h1	ERR pin configuration In CSM, ERR pin only shows errors that are actually handled in CSM if this bit is set or else all errors are flagged
4	RW	1'h1	Enable LS VDS error handling in CSM
3	RW	1'h1	Enable HS VDS error handling in CSM
2	RW	1'h1	Enable programmable dead time in CSM
1	RW	1'h1	Enable boost undervoltage handling in CSM
0	RW	1'h1	Enable VS overvoltage handling in CSM

**Table 9. Configuration Register 2 (CFG2) (Addr. 0x03)**

Bits	R/W	Reset	Definition
7:4	RO	1'h0	Reserved
3:2	RW	2'h0	Current amplifier gain for second stage second amplifier (O4/O2) 00: 2 01: 4 10: 6 11: 8
1:0	RW	2'h0	Current amplifier gain for second stage first amplifier (O3/O1) 00: 2 01: 4 10: 6 11: 8

**Table 10. HS1/2 Slope Register (CURR0) (Addr. 0x04)**

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust HS0/1 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A
2:0	RW	3'h7	Adjust HS0/1 current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

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**Table 11. LS1/2 Slope Register (CURR1) (Addr. 0x05)**

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust LS0/1 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A
2:0	RW	3'h7	Adjust LS0/1 current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

**Table 12. HS3 Slope Register (CURR2) (Addr. 0x06)**

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust HS2 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1A
2:0	RW	3'h7	Adjust HS2 current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

**Table 13. LS3 Slope Register (CURR3) (Addr. 0x07)**

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust LS2 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

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**Table 13. LS3 Slope Register (CURR3) (Addr. 0x07) (continued)**

Bits	R/W	Reset	Definition
2:0	RW	3'h7	Adjust LS2 current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

**Table 14. Status Register 0 (STAT0) (Addr. 0x10)**

Bits	R/W	Reset	Definition
7	RO	1'h0	Reserved
6	RO	1'h0	Over temperature warning
5	RO	1'h0	HS2 VDS error
4	RO	1'h0	HS1 VDS error
3	RO	1'h0	HS0 VDS error
2	RO	1'h0	LS2 VDS error
1	RO	1'h0	LS1 VDS error
0	RO	1'h0	LS0 VDS error

**Table 15. Status Register 1 (STAT1) (Addr. 0x11)**

Bits	R/W	Reset	Definition
7	RO	1'h1	SPI OK flag
6	RO	1'h0	Configuration data CRC failed
5	RO	1'h0	EEPROM data CRC failed
4	RO	1'h0	Programmable dead time violated
3	RO	1'h0	Shoot through protection violated
2	RO	1'h0	Boost undervoltage
1	RO	1'h0	VS overvoltage
0	RO	1'h0	VS undervoltage

**Table 16. Status Register 2 (STAT2) (Addr. 0x12)**

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5	RO	1'h0	HS2 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
4	RO	1'h0	HS1 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
3	RO	1'h0	HS0 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
2	RO	1'h0	LS2 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
1	RO	1'h0	LS1 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
0	RO	1'h0	LS0 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)

**Table 17. CRC Control Register (CRCCTL) (Addr. 0x20)**

Bits	R/W	Reset	Definition
7:1	RO	7'h0	Reserved
0	RO	1'h0	Starts configuration data CRC8 calculation. Bit gets cleared when calculation is finished To perform CRC check: 1. Calculate CRC checksum 2. Store calculated checksum in CRCEXP register 3. Set bit 0 CRC control register (CRCCTL) to 1 4. Bit gets cleared when calculation is finished 5. Failing checksum is indicated in STAT1 register 6. Calculated checksum can be read from CRCCALC register

**Table 18. CRC Calculated Checksum Register (CRCCALC) (Addr. 0x21)**

Bits	R/W	Reset	Definition
7:0	RO	8'h0	Checksum generated by internal CRC engine

**Table 19. CRC Expected Checksum Register (CRCEXP) (Addr. 0x22)**

Bits	R/W	Reset	Definition
7:0	RW	8'h0	Checksum externally calculated by microcontroller

**Table 20. Input Read Back (RB0) (Addr. 0x23)**

Bits	R/W	Reset	Definition
7	RO	1'h0	Reserved
6	RO	1'h0	CSM input
5	RO	1'h0	LS2 input
4	RO	1'h0	LS1 input
3	RO	1'h0	LS0 input
2	RO	1'h0	HS2 input
1	RO	1'h0	HS1 input
0	RO	1'h0	HS0 input

**Table 21. HS/LS Count Control (RB1) (Addr. 0x24)**

Bits	R/W	Reset	Definition
7	RW	1'h0	Clear edge counter This bit has priority over 6 down to 0
6	RW	1'h0	Start/stop counter 0: Counter stopped 1: Counter running
5	RW	1'h0	Enable LS2 edge count
4	RW	1'h0	Enable LS1 edge count
3	RW	1'h0	Enable LS0 edge count
2	RW	1'h0	Enable HS2 edge count
1	RW	1'h0	Enable HS1 edge count
0	RW	1'h0	Enable HS0 edge count

**Table 22. HS/LS Count (RB2) (Addr. 0x25)**

Bits	R/W	Reset	Definition
7:0	RO	8'h0	HS/LS edge count Counter stops counting at 0xFF

**Table 23. Ultima Ratio Command (UR) (Addr. 0x30)**

Bits	R/W	Reset	Definition
7:0	RO	8'h0	Ultima ratio command See specification for command sequence

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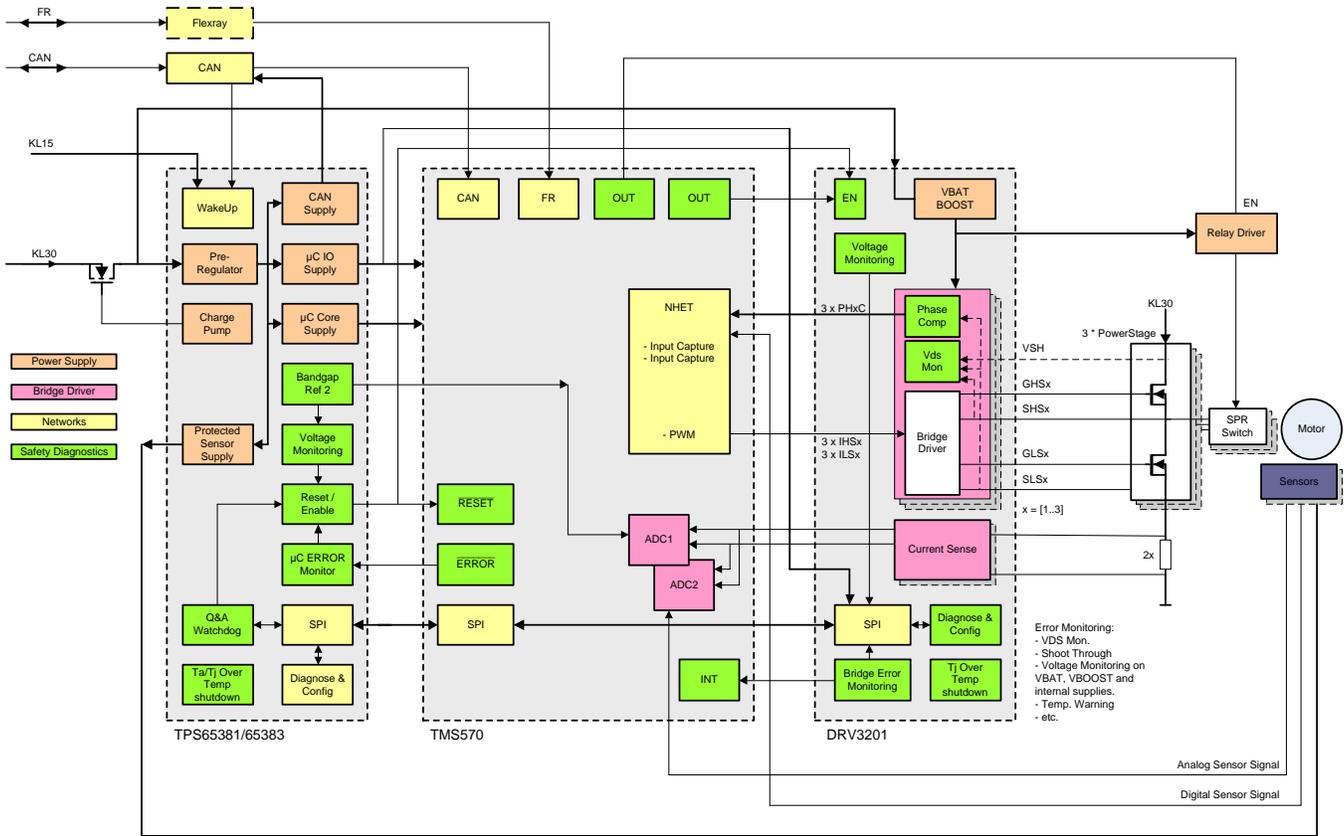
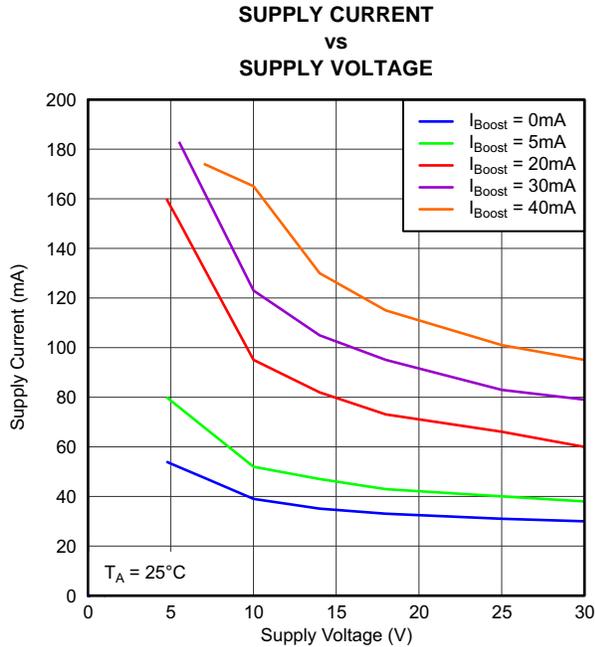


Figure 17. Electrical Power Steering Example

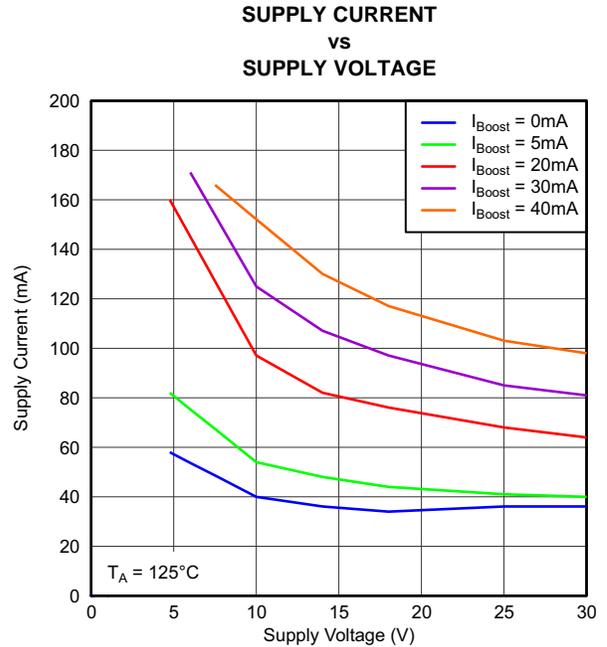
**POWER CONSUMPTION**

The DRV3201-Q1 has been designed to drive six external power FETs with 250 nC gate charge at 30 kHz PWM frequency. The necessary current for charging the gates of these external power FETs is delivered by the boost converter. The three internal high-side gate-drivers and the three internal low-side gate-drivers are supplied out of the boost converter. The following graphs show the total supply current consumption against the supply voltage for varying boost load current.

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G001



G002

Figure 18. Supply Current vs. Supply Voltage for Varying Boost Load Current at  $T_A = 25^\circ\text{C}$

Figure 19. Supply Current vs. Supply Voltage for Varying Boost Load Current at  $T_A = 125^\circ\text{C}$

In these graphs, the quiescent current consumption from the boost converter taken by the non-switching gate-drivers is taken into account (see, parameter  $R_{GSa2}$  in [ELECTRICAL CHARACTERISTICS](#)). However, the current consumption from the boost converter due to gate-driver switching is not taken into account. This gate-driver switching current, which forms the actual load current of the boost converter, consists of two components: the internal gate-driver switching currents, and the external FET gate charging currents.

The switching current from the internal gate-drivers (without the external power FETs) is given in parameter  $V_{GS,HS,high}$  in [ELECTRICAL CHARACTERISTICS](#), for 30 kHz PWM frequency and all six gate-drivers.

The total load current  $I_{boost}$  is given by the sum of [Equation 1](#) and [Equation 2](#):  
 rivers switching. The expected current consumption from the boost converter due to switching gate-drivers (without the external power FETs) can be calculated as follows:

$$I_{boost,sw} = \frac{f_{PWM} \cdot \#FETs \cdot I_{boost,swmax}}{30 \text{ kHz} \cdot 6} = \frac{f_{PWM} \cdot \#FETs \cdot 3 \text{ mA}}{30 \text{ kHz} \cdot 6} \quad (1)$$

The switching current formed by charging the gates of the external FETs at the given PWM frequency can be calculated as follows:

$$I_{boost,sw} = f_{PWM} \cdot \#FETs \cdot Q_{gate} \quad (2)$$

$$I_{boost} = I_{boost,sw} + I_{boost,qg} \quad (3)$$

Calculation example 1:

$$f_{PWM} = 25 \text{ kHz}$$

$$Q_{gate} = 250 \text{ nC}$$

Number of FETs = 6

$$I_{boost,sw} = 25 \text{ kHz} \cdot 6 \cdot 3 \text{ mA} / 30 \text{ kHz} \cdot 6 = 2.5 \text{ mA}$$

$$I_{boost,qg} = 25 \text{ kHz} \cdot 6 \cdot 250 \text{ nC} = 37.5 \text{ mA}$$

$$I_{boost} = 2.5 \text{ mA} + 37.5 \text{ mA} = 40 \text{ mA}$$

Using the  $I_{BOOST} = 40 \text{ mA}$  from [Figure 18](#) and [Figure 19](#), the total current consumption from VS is 130 mA at  $T_A = 25^\circ\text{C}$  and for  $T_A = 125^\circ\text{C}$ . This gives a total power consumption of 1.82 Watt at  $T_A = 25^\circ\text{C}$  and at  $T_A = 125^\circ\text{C}$  for VS = 14 V.

Calculation example 2:

$$f_{PWM} = 20\text{kHz}$$

$$Q_{gate} = 200\text{nC}$$

Number of FETs = 6

$$I_{boost,sw} = 20\text{ kHz} \cdot 6 \cdot 3\text{ mA} / 30\text{ kHz} \cdot 6 = 2\text{ mA}$$

$$I_{boost,qg} = 20\text{ kHz} \cdot 6 \cdot 200\text{ nC} = 24\text{ mA}$$

$$I_{boost} = 2\text{ mA} + 24\text{ mA} = 27\text{ mA}$$

To estimate the total current consumption from the VS battery supply, the curve IBOOST = 30 mA from Figure 14 and Figure 15 can be used. From this curve, it follows that for VS = 14 V, the total current consumption from VS is 105 mA at TA = 25°C respectively 107 mA at TA = 125°C. This gives a total power consumption of 1.47 Watt at TA = 25°C respectively, 1.50 Watt at TA = 125°C for VS = 14 V.

From these examples, it can be seen how the gate-charge and the PWM frequency impact the load current for the boost converter and the total battery current consumption in Figure 18 and Figure 19. The total power consumption can be calculated from this.

### BOOST CONVERTER

The output current capability of the boost converter can be configured with the external Rshunt\_boost resistor to 0.1 V/Rshunt\_boost (please note that this resistor needs to be able to conduct the boost switching current). The output current capability can be dimensioned to the needed current determined by the PWM switching frequency and the gate-charge of the external power FETs. It is recommended to choose a coil having a current saturation level of at least 30% above the current limit level set with the resistor Rboost\_shunt. The operation principle of the boost converter is based on a burst mode fixed frequency controller. During the on-time, the internal low-side boost FET is turned on until the current limit level is detected. The off-time is calculated proportionally from a 2.5 MHz time-reference by sensing the supply voltage VS and the output voltage VBOOST. The formula for the calculated off-time is given in Equation 4, with fboost = 2.5 MHz.

$$t_{off} = \frac{VS}{V_{BOOST} \cdot f_{BOOST}} \tag{4}$$

For steady state, the current in the coil looks like Figure 20.

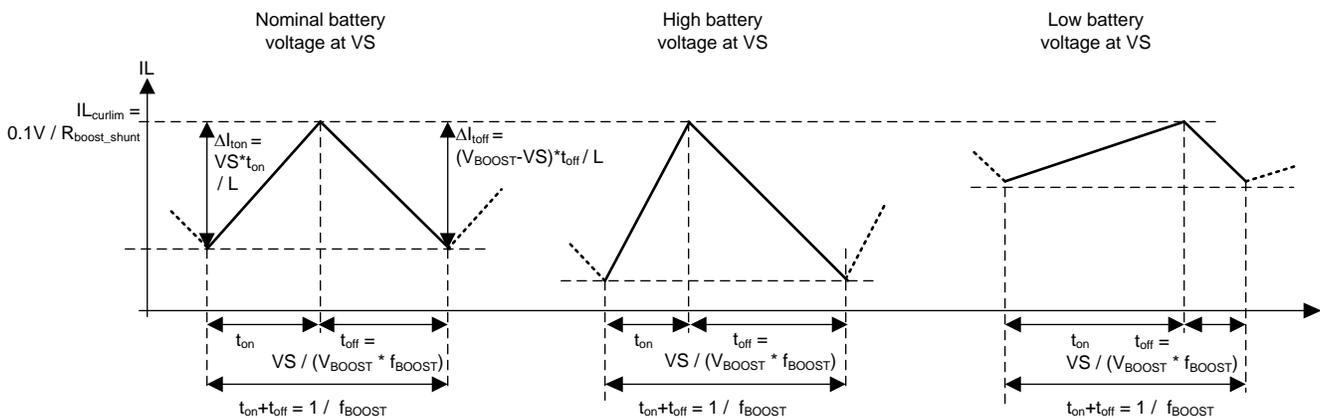


Figure 20. Coil Current Waveforms in Steady State for Nominal, High and Low Battery Voltage

From this figure, the ripple current and the boost output current can be calculated as follows:

$$I_{ripple} = \frac{VS}{L \cdot f_{BOOST}} \cdot \left(1 - \frac{VS}{V_{BOOST}}\right) = \frac{(V_{BOOST} - VS) \cdot VS}{L \cdot f_{BOOST} \cdot V_{BOOST}} \tag{5}$$

$$I_{BOOST} = \frac{VS}{V_{BOOST}} \cdot I_{curlim} - \frac{1}{2} \cdot \left(\frac{(V_{BOOST} - VS) \cdot VS}{L \cdot f_{BOOST} \cdot V_{BOOST}}\right) \tag{6}$$

$$f_{\text{BOOST}} = 2.5 \text{ MHz}; (V_{\text{BOOST}} - V_S) = 15 \text{ V}; I_{L_{\text{curlim}}} = \left( \frac{0.1 \text{ V}}{R_{\text{shunt\_boost}}} \right) \quad (7)$$

As can be seen from Equation 6, the boost output current capability for a given  $I_{L_{\text{curlim}}}$  is the lowest for the minimum supply voltage  $V_S$ . The boost output current capability should be dimensioned (by setting  $I_{L_{\text{curlim}}}$  with external  $R_{\text{shunt\_boost}}$ ) so the needed output current (based on PWM frequency and gate-charge of the external power FETs) can be delivered at the needed minimum supply voltage for the application. The following equation gives  $I_{L_{\text{curlim}}}$  as a function of  $I_{\text{BOOST}}$  and  $V_S$ :

$$I_{L_{\text{curlim}}} = I_{\text{BOOST}} \cdot \frac{V_{\text{BOOST}}}{V_S} + \frac{1}{2} \cdot \left( \frac{(V_{\text{BOOST}} - V_S) \cdot V_S}{L \cdot f_{\text{BOOST}} \cdot V_{\text{BOOST}}} \right) \quad (8)$$

To set the  $I_{L_{\text{curlim}}}$ , the minimum application supply should be used in this equation and  $I_{\text{BOOST}}$  according to Equation 3. The minimum application supply voltage the DRV3201-Q1 can support is 4.75 V.

As shown in Equation 6, the boost output current capability increases for higher supply voltage  $V_S$ . If the boost output current capability is dimensioned so it can deliver the necessary output current for the minimum supply voltage, it actually delivers more current than needed for nominal supply voltage and the boost voltage increases. Therefore, a hysteretic comparator (low level  $V_{\text{BOOST}} - V_S = 14 \text{ V}$ , high level  $V_{\text{BOOST}} - V_S = 16 \text{ V}$ ) determines starting/stopping the burst pulsing as shown in Figure 21.

The nominal switching frequency during the burst pulsing is 2.5 MHz once the boost has reached steady state. During startup of the boost, the internal time reference is slower by a factor of three, resulting in three times longer off-times to allow the coil current to decrease sufficiently compared to Equation 4.

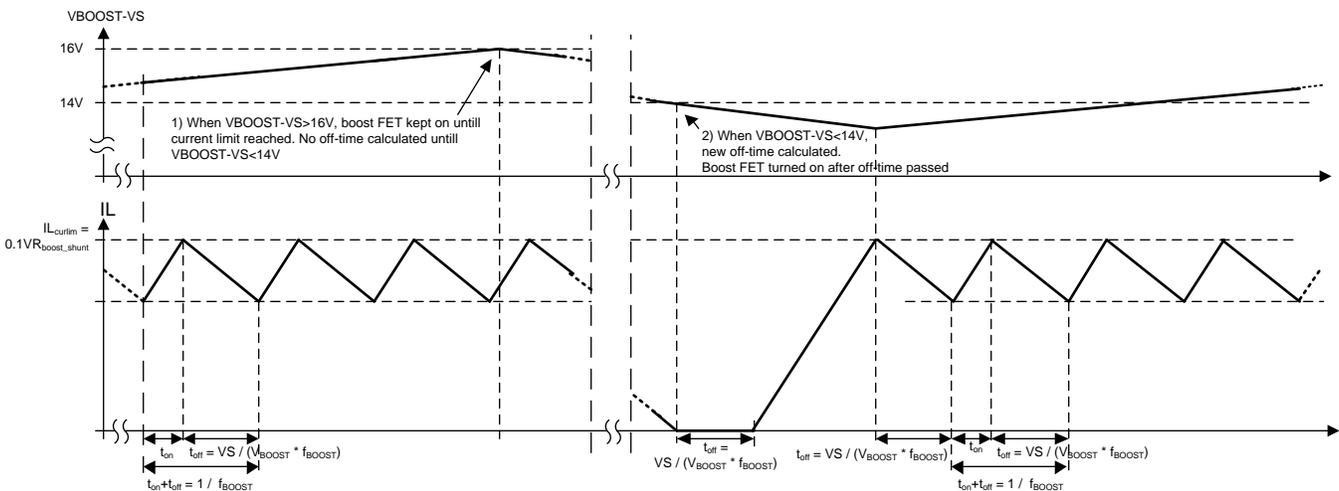


Figure 21. Boost Waveforms Showing Burst Pulsing Controlled by Hysteretic Comparator Levels

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
DRV3201QPAPQ1	PREVIEW	HTQFP	PAP	64	160	TBD	Call TI	Call TI	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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