

DS125BR210 Ultra Low Power 12.5 Gbps 2-Channel Repeater with Input Equalization and Output De-Emphasis

Check for Samples: [DS125BR210](#)

FEATURES

- **Comprehensive Family, Proven System Interoperability**
 - **DS125BR111 : 1-lane, Bi-directional Repeater**
 - **DS125BR210 : 2-channel, Uni-directional Repeater**
 - **DS125BR401 : 4-lane, Bi-directional Repeater**
 - **DS125BR800 : 8-channel, Uni-directional Repeater**
 - **DS125MB203 : 2-port, 2:1/1:2 Mux/Switch**
 - **DS125DF410 : 4-channel, Uni-directional Retimer w/CDR**
- **Low 65 mW/channel (typ) Power Consumption, with Option to Power Down Unused Channels**
- **Transparent Management of Link Training Protocol for PCIe, SAS, 10G-KR**
- **Advanced Signal Conditioning Features**
 - **Receive Equalization up to 30 dB at 6.25 GHz**
 - **Transmit De-emphasis up to -12 dB**
 - **Transmit Output Voltage Control: 700 mV to 1300 mV**
- **Programmable via Pin Selection, EEPROM or SMBus Interface**
- **Single Supply Voltage: 2.5V or 3.3V (Selectable)**
- **-40 to 85°C Operating Temperature Range**
- **5 kV HBM ESD Rating**
- **Flow-thru Pinout: 24-pin WQFN (4 mm x 4 mm, 0.5 mm pitch)**
- **Supported Protocols**
- **SAS-3/2/1, SATA, Fibre Channel (up to 10GFC)**

- **PCIe Gen-3/2/1, 10G-KR, 10GbE, XAUI, RXAUI**
- **sRIO, Infiniband, Interlaken, CPRI, OBSAI**
- **Other Proprietary Interface up to 12.5 Gbps**

DESCRIPTION

The DS125BR210 is an extremely low power, high performance multi-protocol repeater/redriver designed to support 2 channels of SAS-3/2/1, PCIe Gen-3/2/1, 10G-KR and other high speed interface serial protocols up to 12.5 Gbps. The receiver's continuous time linear equalizer (CTLE) provides a boost of up to +30 dB at 6.25 GHz (12.5 Gbps) in each of its two channels and is capable of opening an input eye that is completely closed due to inter symbol interference (ISI) induced by interconnect medium such as 30"+ backplane traces or 8m+ copper cables, hence enabling host controllers to ensure an error free end-to-end link. The transmitter provides a de-emphasis boost of up to -12 dB and output voltage amplitude control from 700 mV to 1300 mV to allow maximum flexibility in the physical placement within the interconnect channel.

When operating in SAS-3, 10G-KR and PCIe Gen-3 mode, the DS125BR210 transparently allows the host controller and the end point to optimize the full link and negotiate transmit equalizer coefficients. This seamless management of the link training protocol ensures guaranteed system level interoperability with minimum latency. With a low power consumption of 65 mW/channel (typ) and option to turn-off unused channels, the DS125BR210 enables energy efficient system design. A single supply of 3.3v or 2.5v is required to power the device.

The programmable settings can be applied easily via pins, software (SMBus/I2C) or loaded via an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.



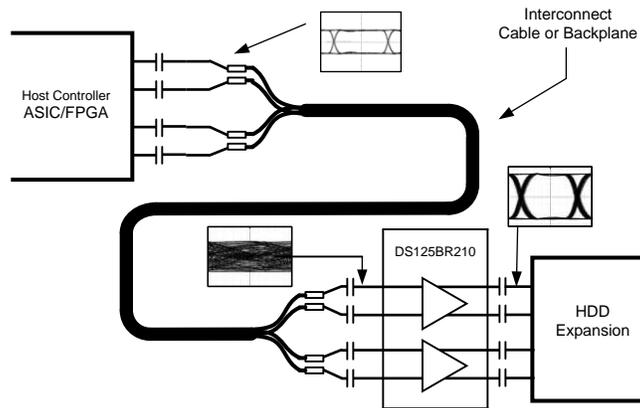
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



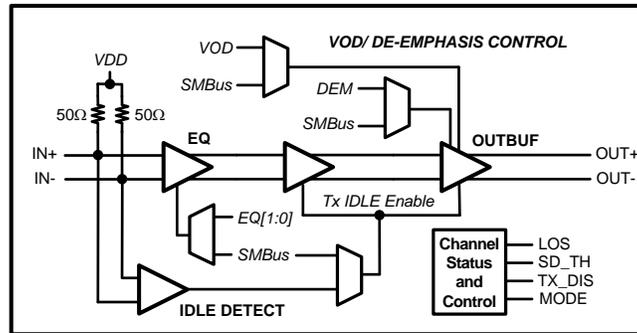
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Typical Application

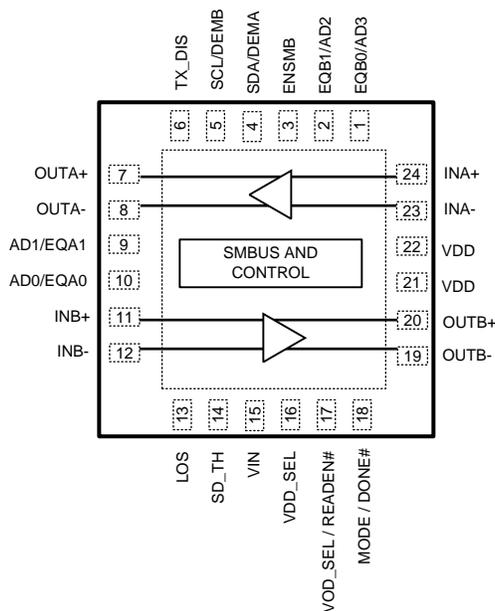


Block Diagram - Detail View Of Channel (1 Of 2)



PRODUCT PREVIEW

Pin Diagram



The center DAP on the package bottom is the device GND connection. This pad must be connected to GND through multiple (minimum of 4) vias to ensure optimal electrical and thermal performance.

Figure 1. DS125BR210 Pin Diagram 24 lead, Top View

NOTE

Above 24-lead WQFN graphic is a TOP VIEW, looking down through the package.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DS125BR210SQ/NOPB	PREVIEW	WQFN	RTW	24	1	TBD	Call TI	Call TI	
DS125BR210SQE/NOPB	PREVIEW	WQFN	RTW	24	1	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

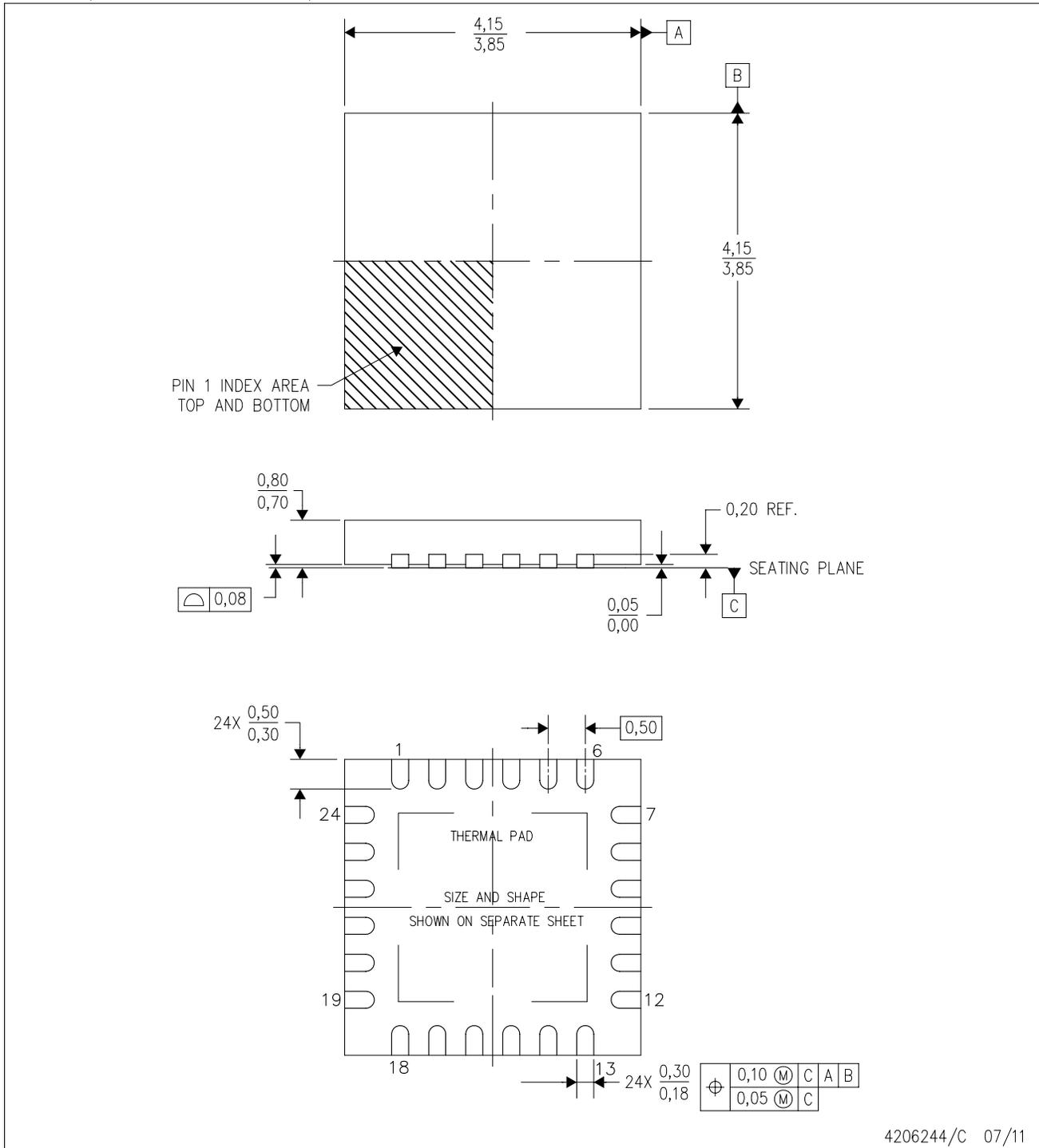
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RTW (S-PWQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4206244/C 07/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

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