

DS3487 Quad TRI-STATE Line Driver

Check for Samples: [DS3487](#)

FEATURES

- Four Independent Drivers
- TRI-STATE Outputs
- Fast Propagation Times (typ 10 ns)
- TTL Compatible
- 5V Supply
- Output Rise and Fall Times Less than 15 ns
- Pin Compatible with DS8924 and MC3487

DESCRIPTION

The DS3487 quad RS-422 driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs.

Block and Connection Diagrams

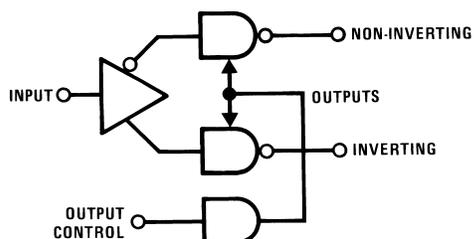
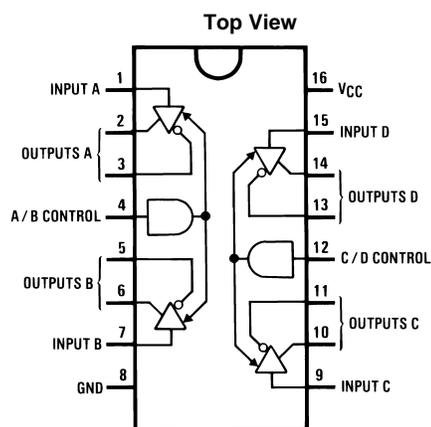


Figure 1. Block Diagram


Figure 2. PDIP Package
See Package Number D0016A or NFG0016E

Truth Table⁽¹⁾

Input	Control	Non-Inverting	Inverting
	Input	Output	Output
H	H	H	L
L	H	L	H
X	L	Z	Z

- (1) L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	-65°C to +150°C
Maximum Power Dissipation ⁽³⁾ at 25°C	
PDIP Package	1476 mW
SOIC Package	1051 mW
Lead Temperature	
(Soldering, 4 seconds)	260°C

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Derate PDIP molded package 11.9 mW/°C above 25°C. Derate SOIC package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3487	0	+70	°C

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Parameter		Test Conditions	Min	Typ	Max	Units	
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{IL}	Input Low Current	$V_{IL} = 0.5V$			-200	μA	
I_{IH}	Input High Current	$V_{IH} = 2.7V$			50	μA	
		$V_{IH} = 5.5V$			100	μA	
V_{CL}	Input Clamp Voltage	$I_{CL} = -18 mA$			-1.5	V	
V_{OL}	Output Low Voltage	$I_{OL} = 48 mA$			0.5	V	
V_{OH}	Output High Voltage	$I_{OH} = -20 mA$	2.5			V	
I_{OS}	Output Short-Circuit Current		-40		-140	mA	
I_{OZ}	Output Leakage Current (TRI-STATE)	$V_O = 0.5V$			-100	μA	
		$V_O = 5.5V$			100	μA	
I_{OFF}	Output Leakage Current Power OFF	$V_{CC} = 0V$	$V_O = 6V$			100	μA
			$V_O = -0.25V$			-100	μA
$ V_{OS} - \overline{V_{OS}} $	Difference in Output Offset Voltage				0.4	V	
V_T	Differential Output Voltage		2.0			V	
$ V_T - \overline{ V_T }$	Difference in Differential Output Voltage				0.4	V	
I_{CC}	Power Supply Current	Active		50	80	mA	
		TRI-STATE		35	60	mA	

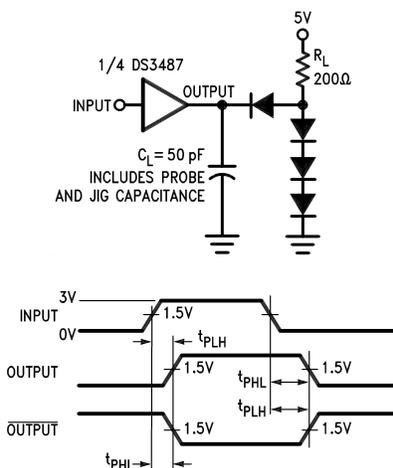
- (1) Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ C$.
- (2) All currents into device pins are positive, all currents out of device pins as negative. All voltages are referenced to ground unless otherwise specified.
- (3) Only one output at a time should be shorted.
- (4) Symbols and definitions correspond to EIA RS-422, where applicable.

Switching Characteristics

$V_{CC} = 5V, T_A = 25^\circ C$

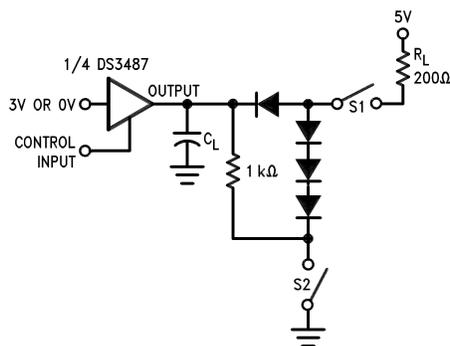
Parameter		Test Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	$R_L = 200\Omega, C_L = 50\text{ pF}$		17	25	ns
t_{PLZ}	Enable to Output	$R_L = 200\Omega, C_L = 50\text{ pF}$		15	25	ns
t_{PZH}	Enable to Output	$R_L = \infty, C_L = 50\text{ pF}, S1\text{ Open}$		11	25	ns
t_{PZL}	Enable to Output	$R_L = 200\Omega, C_L = 50\text{ pF}, S2\text{ Open}$		15	25	ns

AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS

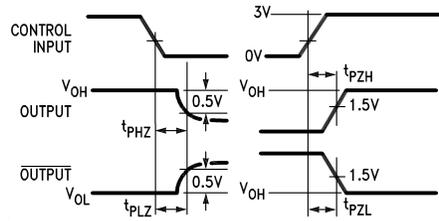


Input pulse: $f = \text{MHz}, 50\%; t_r = t_f \leq 15\text{ ns}$.

Figure 3. Propagation Delays

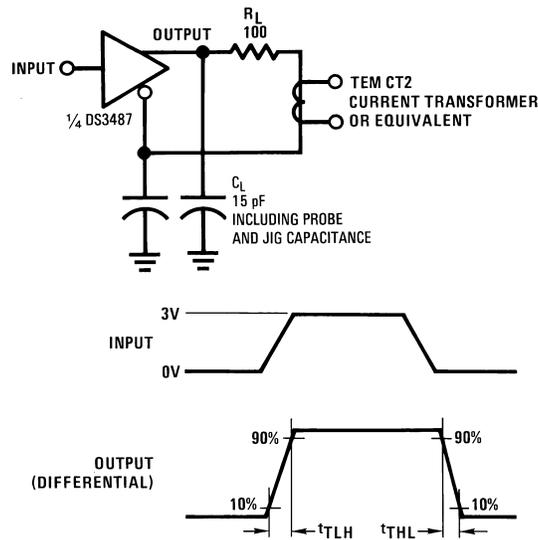


S1 and S2 closed except as noted.
 C_L includes probe and jig capacitance.



Input pulse: $f = \text{MHz}$, 50%; $t_r = t_f \leq 15 \text{ ns}$.
 S1 = open for t_{PZH}
 S2 = open for t_{PLZ}

Figure 4. TRI-STATE Enable and Disable Delays



Input pulse: $f = \text{MHz}$, 50%; $t_r = t_f \leq 15 \text{ ns}$.

Figure 5. Differential Rise and Fall Times

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS3487M	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	DS3487M	Samples
DS3487M/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS3487M	Samples
DS3487MX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	DS3487M	Samples
DS3487MX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS3487M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

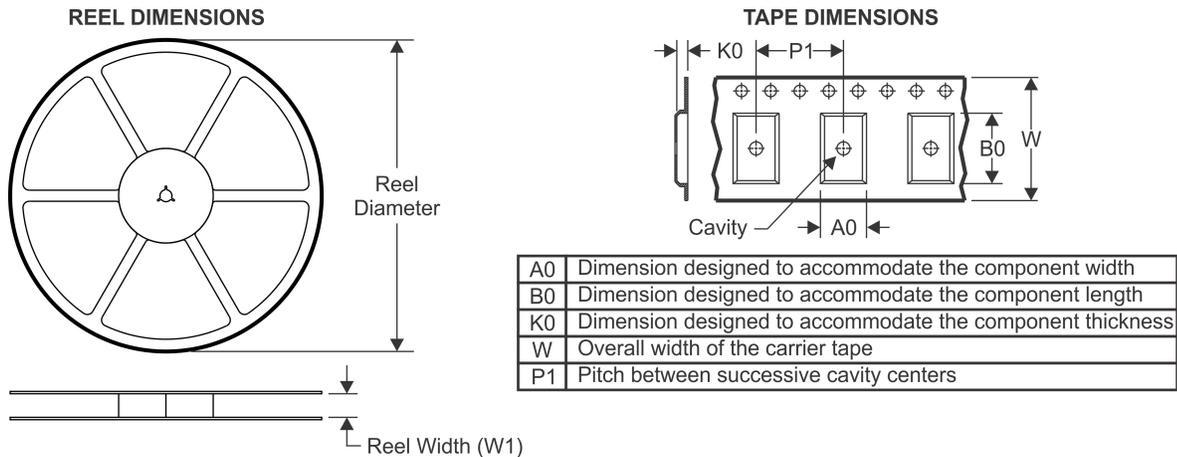
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

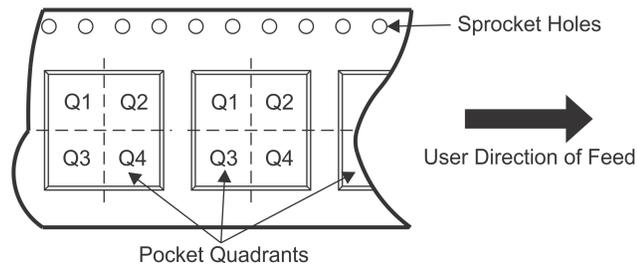
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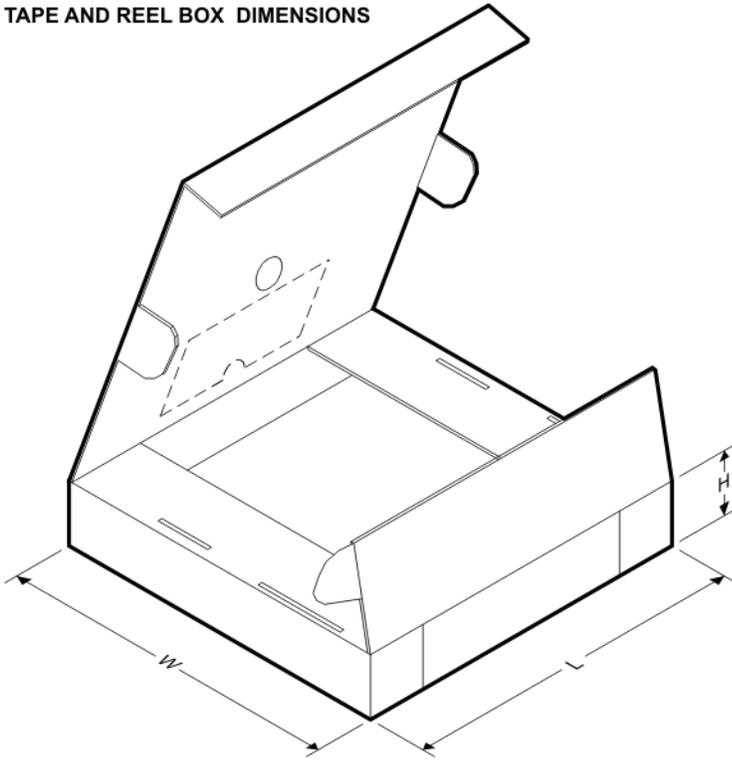


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3487MX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS3487MX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

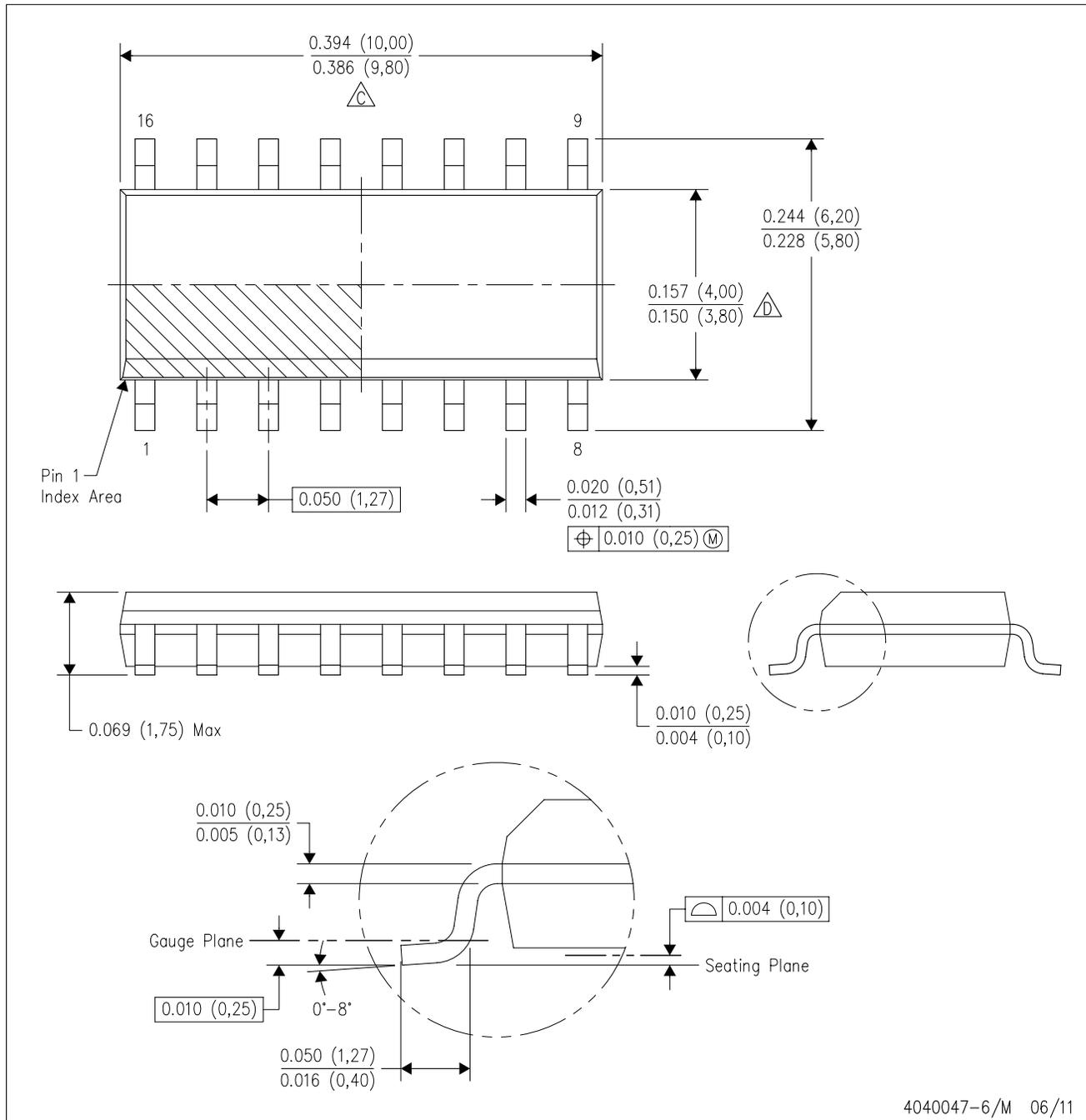
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3487MX	SOIC	D	16	2500	367.0	367.0	35.0
DS3487MX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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