National Semiconductor

DS1652/DS3650/DS3652
Quad Differential Line Receivers

General Description

The DS3650 and DS1652/DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS1652/DS3652 offers open collector outputs providing implied "AND" operation.

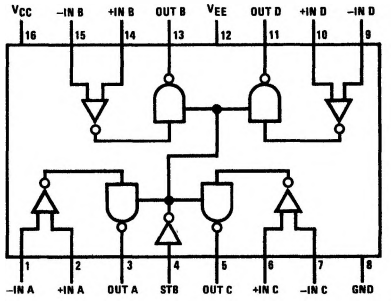
The DS1652/DS3652 can be used for address decoding as illustrated below. All outputs of the DS1652/DS3652 are tied together through a common resistor to 5V. In this configuration, the DS1652/DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

Features

- High speed
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS3650M, DS3652M or DS3650N
See NS Package Number M16A or N16A

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS1652J
See NS Package Number J16A

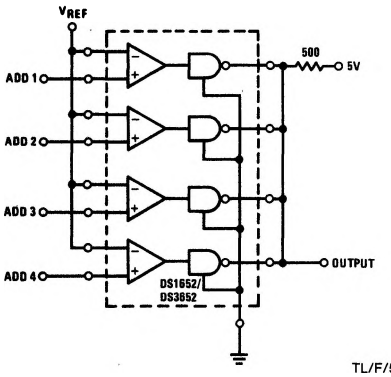
Truth Table

Input	Strobe	Output	
		DS3650	DS1652/ DS3652
$V_D \geq 25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

Typical Applications

Implied "AND" Gating



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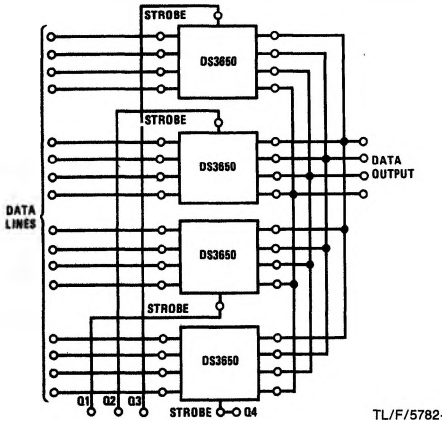
Wired "OR" Data Selecting Using TRI-STATE Logic



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltages	
V_{CC}	+7.0 V_{DC}
V_{EE}	−7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.8 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1652	4.5	5.5	V_{DC}
DS3650, DS3652	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}			
DS1652	−4.5	−5.5	V_{DC}
DS3650, DS3652	−4.75	−5.25	V_{DC}
Operating Temperature, T_A			
DS1652	−55	+125	°C
DS3650, DS3652	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range Input to GND, V_{IR}	−5.0	+3.0	V_{DC}

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max				±25.0	mV
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)}$ = 2.4V, DS1652			100	µA
			$V_{IH(S)}$ = 2.4V, DS3650, DS3652			40	µA
			$V_{IH(S)}$ = V_{CC}			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)}$ = 0.4V			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS3650	2.4			V
I_{CEX}	High Level Output Leakage Current	*(Figure 1)*	DS1652, DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*	DS3650, DS3652			0.45	V
			DS1652			0.50	
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS3650			40	µA

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}	*(Figure 2)*			−17	−30	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650, DS3652 and the −55°C to +125°C range for the DS1652. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

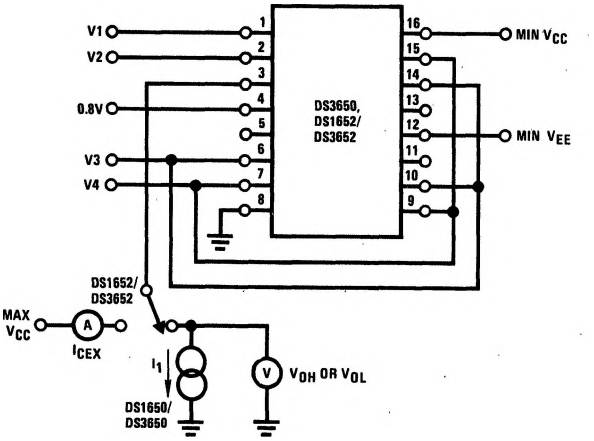
Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1652 and the DS3650, DS3652 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Characteristics (V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS3650		21	25	ns
			DS1652/DS3652		20	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS3650		20	25	ns
			DS1652/DS3652		22	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS3650		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS3650		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS1652/DS3652		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS1652/DS3652		13	25	ns

Electrical Characteristic Test Circuits



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	V1		V2		V3		V4		I_1
	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	
V_{OH}	+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V		−0.4 mA −0.4 mA
I_{CEX}		+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V	
V_{OL}	+3.0V −2.975V	+3.0V −2.975V	+2.975V −3.0V	+2.975V −3.0V	GND −3.0V	GND −3.0V	+3.0V GND	+3.0V GND	+16 mA +16 mA

Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH} and V_{OL}

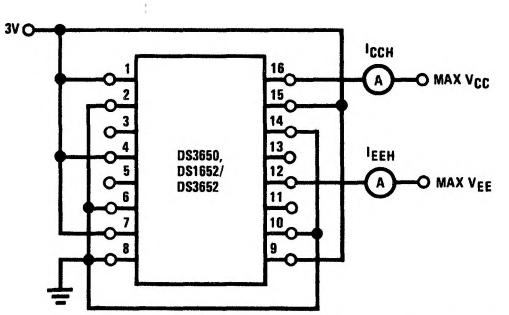

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FIGURE 2. I_{CCH} and I_{EEH}

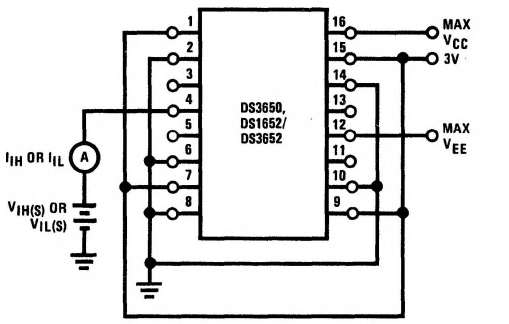

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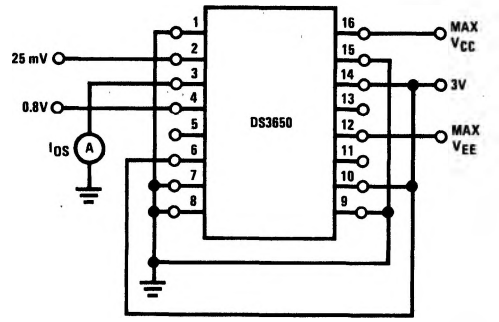
FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$

Electrical Characteristic Test Circuits (Continued)



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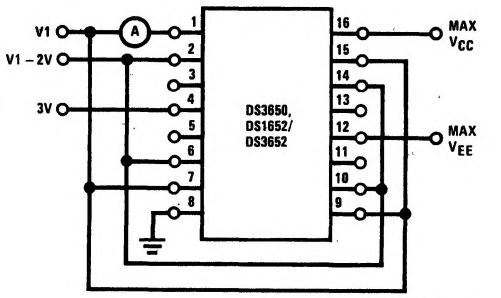
Note: Channel A shown under test, other channels are tested similiarly. Only one output shorted at a time.

FIGURE 4. I_{OS}



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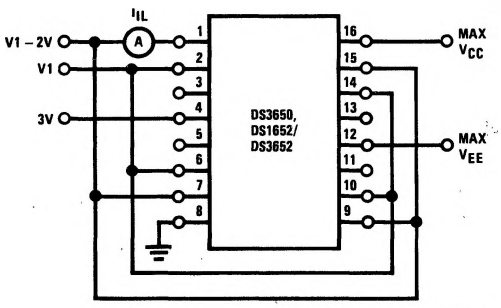
Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

FIGURE 5. I_{IH}



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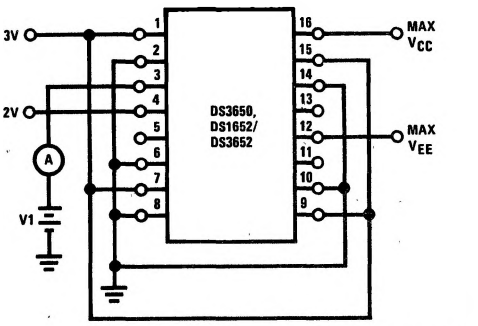
Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

FIGURE 6. I_{IL}



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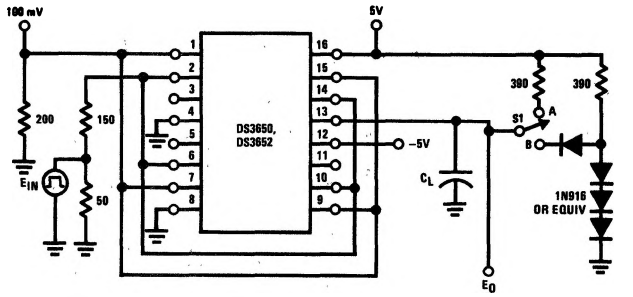
Note: Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

FIGURE 7. I_{OFF}

AC Test Circuits and Switching Time Waveforms



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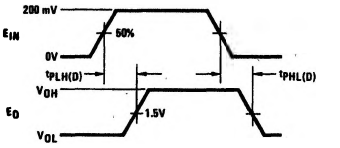

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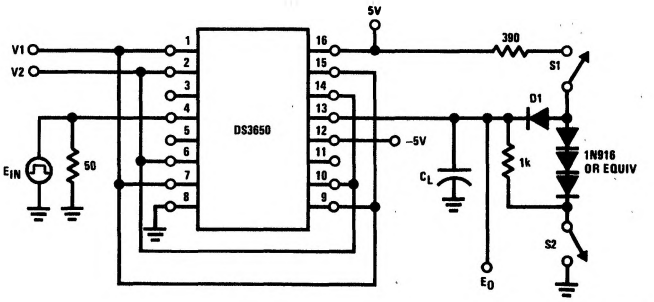
Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured
10% to 90%
PRR = 1 MHz
Duty Cycle = 50%

Note: Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for DS1652/DS3652
S1 at "B" for DS1650/DS3650
C_L = 15 pF total for DS1652/DS3652
C_L = 50 pF total for DS1650/DS3650

FIGURE 8. Receiver Propagation Dealy $t_{PLH(D)}$ and $t_{PHL(D)}$



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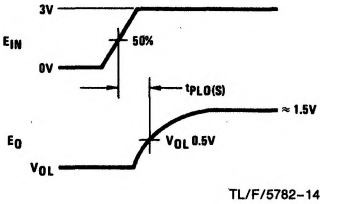

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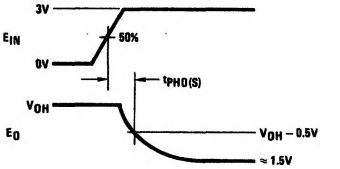

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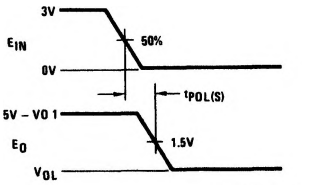
Note: Output of Channel B shown under test, other channels are tested similiarly.

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 50%



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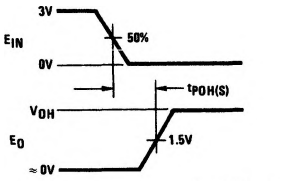

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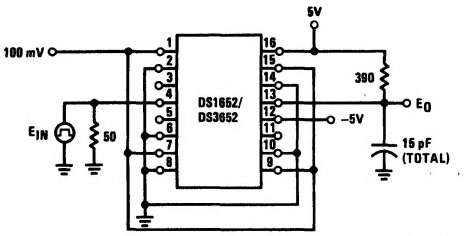
FIGURE 9. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

AC Test Circuits and Switching Time Waveforms (Continued)



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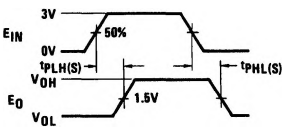

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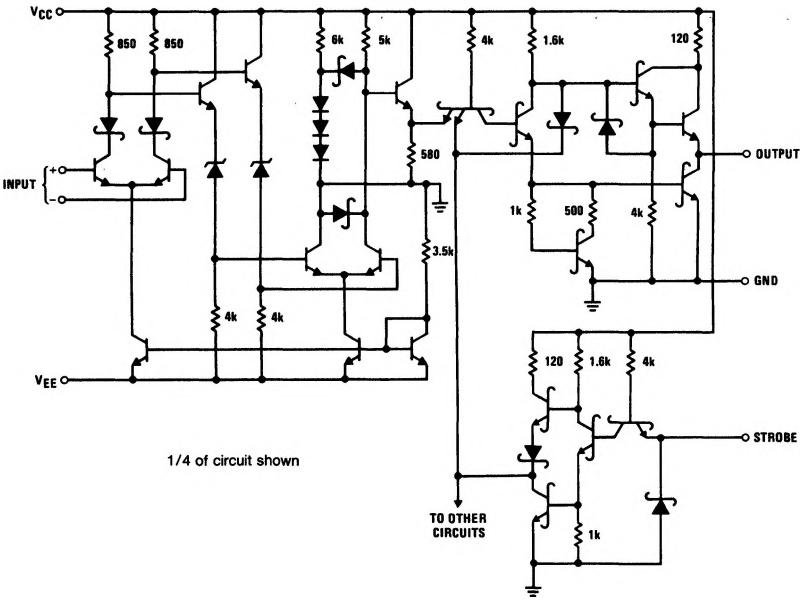
Note: Output of Channel B shown under test, other channels are tested similarly.

Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% and 90%
PRR = 1 MHz
Duty Cycle = 500 ns

FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

Schematic Diagrams

DS3650



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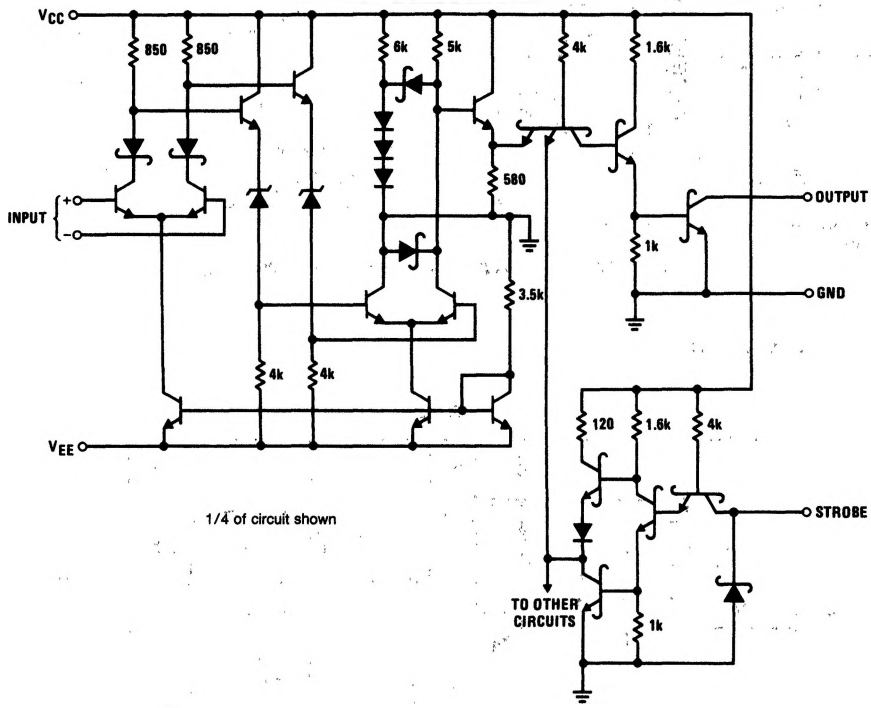
Schematic Diagrams (Continued)

DS1652/DS3652



1/4 of circuit shown

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