National Semiconductor

PRELIMINARY

DS36C200
Dual High Speed Bi-Directional Differential Transceiver

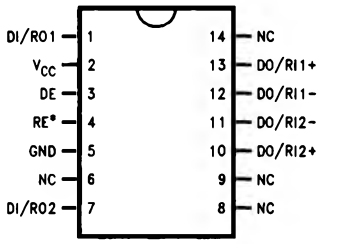
General Description

The DS36C200 is a dual transceiver device optimized for high data rate and low power applications. This device provides a single chip solution for a dual high speed bi-directional interface. Also, both control pins may be routed together for single bit control of datastreams. Both control pins are adjacent to each other for ease of routing them together. The DS36C200 is compatible with IEEE 1394 physical layer and may be used as an economical solution with some considerations. Please reference the application information on 1394 for more information. The device is in a 14-lead small outline package. The differential driver outputs provides low EMI with its low output swings typically 210 mV. The receiver offers ±100 mV threshold sensitivity, in addition to common mode noise protection.

Features

- Optimized for DSS to DVHS interface link
- IEEE 1394 signaling
- Operates above 100 Mbps
- Bi-directional transceivers
- 14-lead SOIC package
- Ultra low power dissipation
- ±100 mV receiver sensitivity
- Low differential output swing typical 210 mV

Connection Diagram



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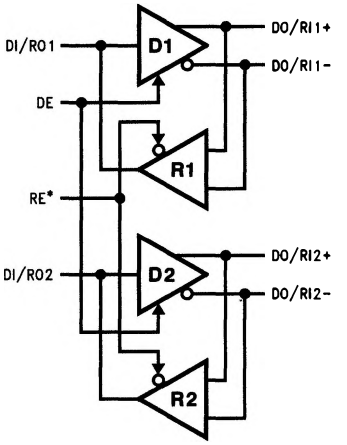
Order Number DS36C200M
See NS Package Number M14A

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Enable Input Voltage (DE, RE*)	−0.3V to (V_{CC} + 0.3V)
Voltage (DI/RO)	−0.3V to (V_{CC} + 0.3V)
Voltage (DO/RI±)	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation @ +25°C	
M Package	TBD mW
Derate M Package	TBD mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4 sec.)	+260°C
ESD Rating (HBM 1.5 kΩ, 100 pF) (Note 4)	≥2.5 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	0		2.4	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3 and 7)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
V_{OD}	Output Differential Voltage	R_L = 55Ω *Figure 1*	DO+, DO−	172	210	TBD	mV
ΔV_{OD}	V_{OD} Magnitude Change			0	4	35	mV
V_{OH}	Output High Voltage				1.36	1.6	V
V_{OL}	Output Low Voltage			0.9	1.15		V
V_{OS}	Offset Voltage			0.9	1.25	1.6	V
ΔV_{OS}	Offset Magnitude Change			0	5	25	mV
I_{OZD}	TRI-STATE® Leakage	V_O = V_{CC} or GND		0	±1	±10	μA
I_{OXD}	Power-Off Leakage	V_O = V_{CC} = GND = 0V		0	±1	±10	μA
I_{OSD}	Output Short Circuit Current				−6	−9	mA
DIFFERENTIAL RECEIVER CHARACTERISTICS							
V_{TH}	Input Threshold High		RI+, RI−			+100	mV
V_{TL}	Input Threshold Low			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, or 0V		−10	±1	+10	μA
V_{OH}	Output High Voltage	I_{OH} = −400 μA	RO	3.8	4.9		V
		Inputs Open		3.8	4.9		V
		Inputs Terminated, R_t = 55Ω		3.8	4.9		V
		Inputs Shorted, V_{OD} = 0V			4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA, V_{ID} = −200 mV			0.3	0.5	V
I_{OSR}	Output Short Circuit Current	V_{OUT} = 0V		−15	−60	−100	mA

Electrical Characteristics (Continued)

Over supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3 and 7)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V_{IH}	Input High Voltage		DI, DE RE*	2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{CC}$ or 2.4V			±1	±10	μA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			±1	±10	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA		−1.5	−0.8		V
I_{CCD}	Power Supply Current	No Load; DE = RE* = V_{CC}	V_{CC}		3	7	mA
		$R_L = 55\Omega$; DE = RE* = V_{CC}			10	TBD	mA
I_{CCR}		DE = RE* = 0V			5	7	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} amd V_{ID}.

Note 3: All typicals are given for $V_{CC} = +5.0$V and $T_A = +25$°C.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF) ≥ 2.5 kV
EIAJ (0Ω, 200 pF) ≥ TBD

Note 5: C_L includes probe and fixture capacitance.

Note 6: Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_O = 50\Omega$, $t_r \leq 1$ ns, $t_f \leq 1$ ns (0%–100%).

Note 7: The DS36C200 is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 55Ω, C_L = 50 pF *(Figures 2 and 3)*	1.5	3.4	6	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.5	3.50	6	ns
t_{SKD}	Differential Skew $\|t_{PHLD}-t_{PLHD}\|$		0.1	0.1	2	ns
t_{TLH}	Transition Time Low to High		0	0.5	2	ns
t_{THL}	Transition Time High to Low		0	0.5	2	ns
t_{PHZ}	Disable Time High to Z	R_L = 55Ω *(Figures 4 and 5)*	0.3	5	20	ns
t_{PLZ}	Disable Time Low to Z		0.3	5	20	ns
t_{PZH}	Enable Time Z to High		0.3	10	30	ns
t_{PZL}	Enable Time Z to Low		0.3	10	30	ns
DIFFERENTIAL RECEIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 50 pF, V_{ID} = 200 mV *(Figures 6 and 7)*	1.5	3.4	6	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.5	3.5	6	ns
t_{SKD}	Differential Skew $\|t_{PHLD}-t_{PLHD}\|$		0.1	0.1	2	ns
t_r	Rise Time		0	0.5	2.5	ns
t_f	Fall Time		0	0.5	2.5	ns
t_{PHZ}	Disable Time High to Z	C_L = 5 pF *(Figures 8 and 9)*	1	10	20	ns
t_{PLZ}	Disable Time Low to Z		1	10	20	ns
t_{PZH}	Enable Time Z to High		0.3	10	30	ns
t_{PZL}	Enable Time Z to Low		0.3	10	30	ns

Parameter Measurement Information

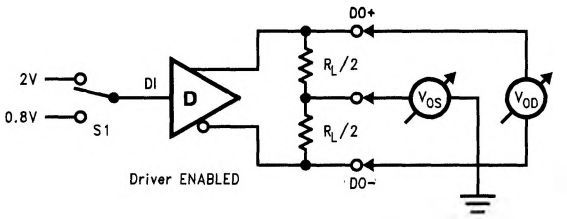

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FIGURE 1. Differential Driver DC Test Circuit

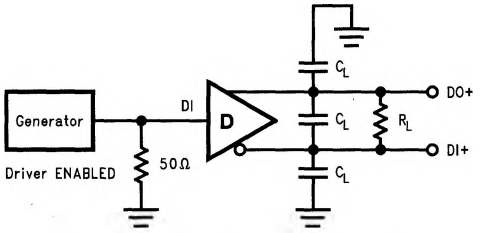

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FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

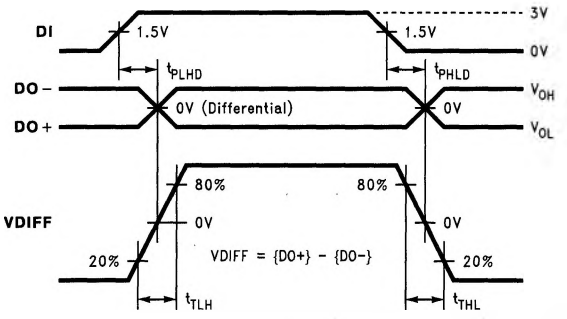

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FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (Continued)

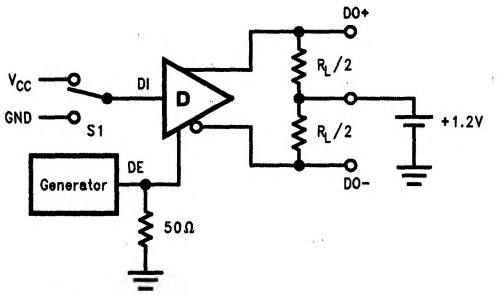

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FIGURE 4. Driver TRI-STATE Delay Test Circuit

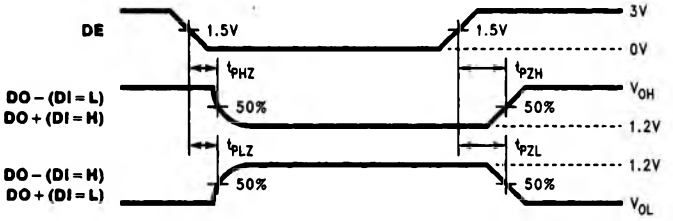

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FIGURE 5. Driver TRI-STATE Delay Waveforms

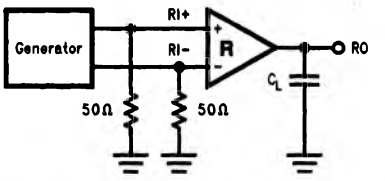

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FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit

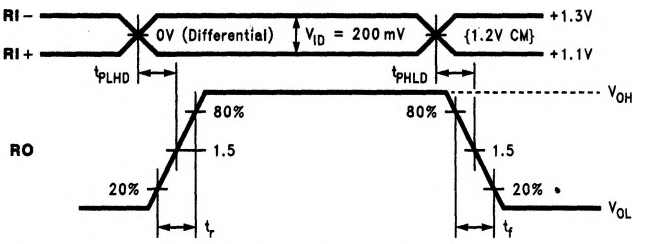

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FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (Continued)

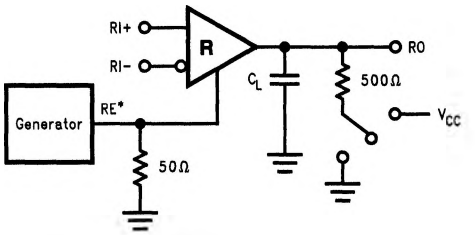

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FIGURE 8. Receiver TRI-STATE Delay Test Circuit

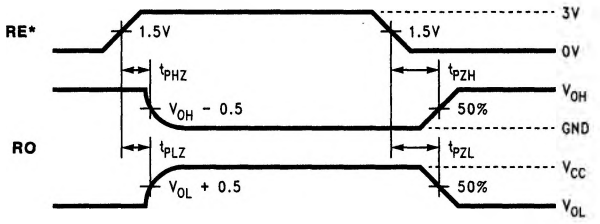

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FIGURE 9. Receiver TRI-STATE Delay Waveforms

Application Information

TRUTH TABLES

The DS36C200 has two enable pins DE and RE*, however, the driver and receiver should never be enabled simultaneously. Enabling both could cause multiple channel contention. It is recommended to route the enables together on the PC board. This will allow a single bit [DE/RE*] to control the chip. This DE/RE* bit toggles the DS36C200 between Receive mode and Transmit mode. When the bit is asserted HIGH the device is in Transmit mode. When the bit is asserted LOW the device is in Receive mode. The mode determines the function of the I/O pins: DI/RO, DO/RI+, and DO/RI−. Please note that some of the pins have been identified by its function in the corresponding mode in the three tables below. For example, in Transmit mode the DO/RI+ pin is identified as DO+. This was done for clarity in the tables only and should not be confused with the pin identification throughout the rest of this document. Also note that a logic low on the DE/RE* bit corresponds to a logic low on both the DE pin and the RE* pin. Similarly, a logic high on the DE/RE* bit corresponds to a logic high on both the DE pin and the RE* pin.

Receive Mode

Input(s)		Input/Output	
DE	RE*	[RI+] − [RI−]	RO
L	L	> +100 mV	H
L	L	< −100 mV	L
L	L	100 mV > & > −100 mV	X

Transmit Mode

Input(s)		Input/Output		
DE	RE*	DI	DO+	DO−
H	H	L	L	H
H	H	H	H	L
H	H	2 > & > 0.8	X	X

H = Logic high level

L = Logic low level

X = Indeterminant state

TABLE I. Device Pin Descriptions

Pin #	Name (In mode only)	Mode	Description
3	DE	Transmit	Driver Enable: When asserted low driver is disabled. And when asserted high driver is enabled.
1, 7	DI		TTL/CMOS driver input pins
10, 13	DO+		Noninverting driver output pin
11, 12	DO−		Inverting driver output pin
4	RE*	Receive	Receiver Enable: When asserted low receiver is enabled. And when asserted high receiver is disabled.
1, 7	RO		Receiver output pin
10, 13	RI+		Positive receiver input pin
11, 12	RI−		Negative receiver input pin
5	GND	Transmit and Receive	Ground pin
2	V_{CC}		Positive power supply pin, +5V ±10%

IEEE 1394

The DS36C200 drives and receives IEEE 1394 physical layer signal levels. The current mode driver is cabpable of driving a 55Ω load with V_{OD} between 172 mV and TBD mV. The DS36C200 is not designed to work with a link layer controller IC requiring full 1394 physical layer compliancy to the standard. No clock generator, no arbitration, and no encode/decode logic is provided with this device. For a 1394 link where speed sensing, bus arbitration, and other functions are not required, a controller and the DS36C200 will provide a cost effective, high speed dedicated link. This is shown in *Figure 10A*. In applications that require fully compliant 1394 protocol, a link layer controller and physical layer controller will be required as shown in *Figure 10B*. The physical layer controller supports up to three DC36C200 devices (not shown).

Application Information (Continued)

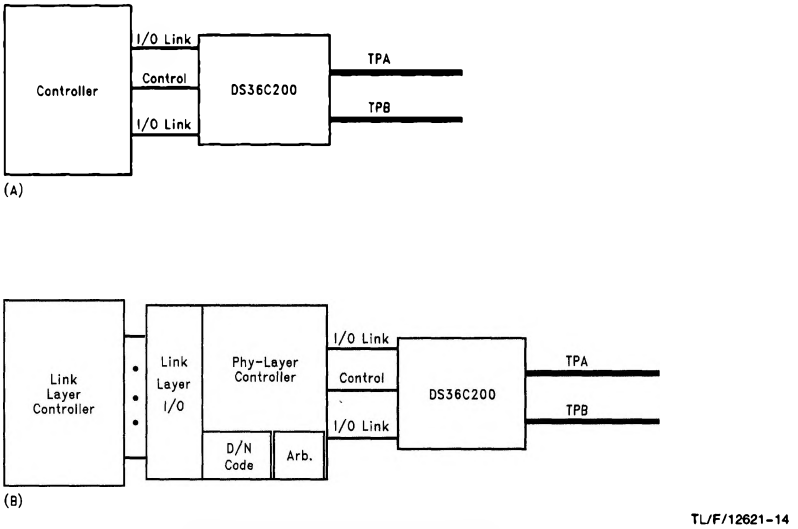

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FIGURE 10. (A) Dedicated IEEE 1394 Link
(B) Full IEEE 1394 Compliant Link

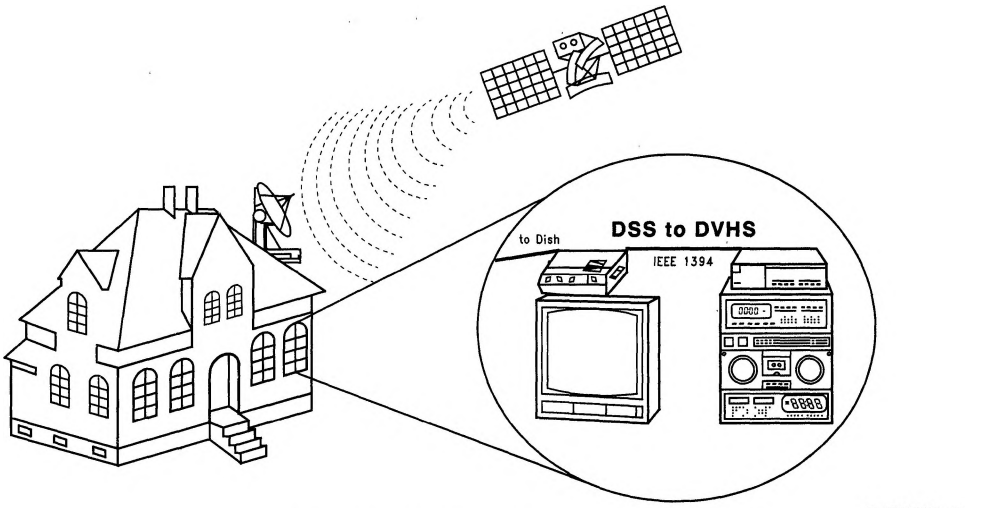

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FIGURE 11. Typical in Home Application

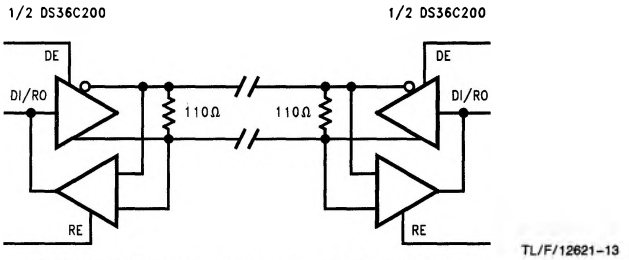

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FIGURE 12. Typical Interface Connection (Note 7)