

## DS3884A

### BTL Handshake Transceiver MIL-STD-883

#### General Description—(MIL Only)

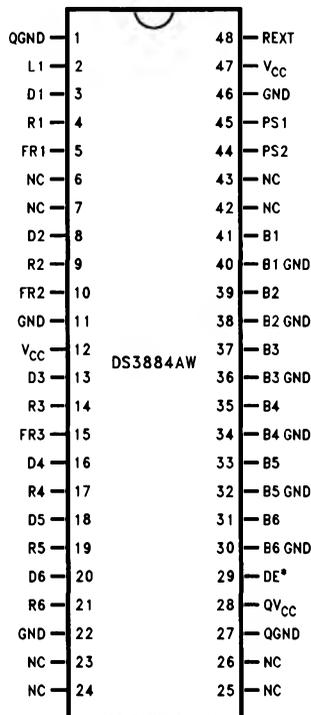
The DS3884A is pin to pin and functionally compatible with the DS3884. The DS3884A is a speed and power enhanced version of the DS3884. There are two minor differences between the DS3884 and DS3884A.

The external resistor used in the DS3884A is different from that used in the DS3884. REXT for the DS3884 is 6.2k while REXT for the DS3884A is 15 k $\Omega$ . The available filter settings for the DS3884A are 5 ns, 10 ns, 14 ns, 20 ns, while the settings for the DS3884 are 5 ns, 7.5 ns, 15 ns, and 25 ns.

#### Features

- Fast propagation delay
- 6-bit BTL transceiver
- Selective receiver glitch filtering (FR1–FR3)
- Meets 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80 mA
- TTL compatible driver and control inputs
- Separate TTL I/O
- Open collector bus-port outputs allow Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- Built in Bandgap reference with separate QV<sub>CC</sub> and QGND pins for precise receiver thresholds
- Individual Bus-port ground pins
- Product offered in glass sealed CERPAK

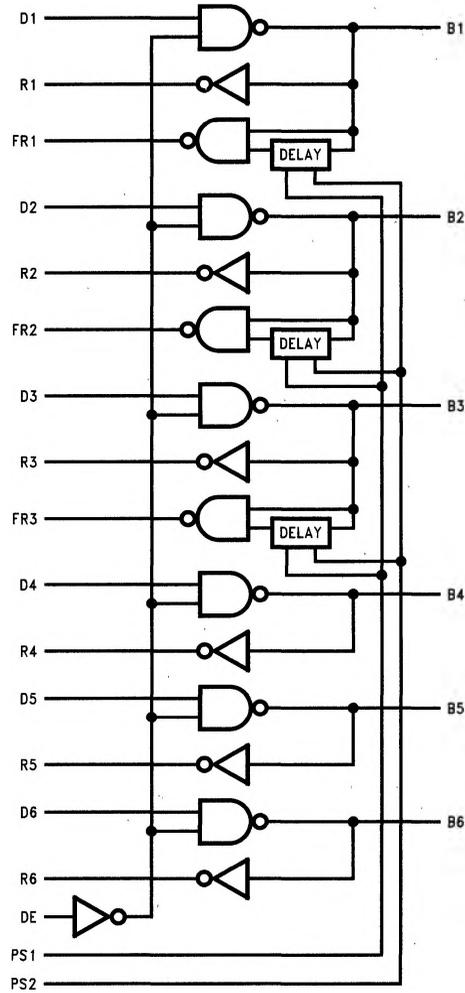
#### Connection Diagram



TL/F/11976-1

**Order Number DS3884AW/883**  
**See NS Package Number WA48A**

# Logic Diagram



TL/F/11976-2

## General Description (Continued)

The DS3884A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3884A is a BTL 6-bit Handshake Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL). Utilization of the DS3884A simplifies the implementation of all handshake signals which require Wired-OR glitch filtering. Three of the six bits have an additional parallel Wired-OR filtered receive output giving a total of nine receiver outputs. In Wired-OR applications, the glitch generated as drivers are released from the bus, is dependent upon the backplane and parasitic wiring components causing the characteristics of the glitch to vary in pulse width and amplitude. To accommodate this variation the DS3884A features two pins defined as PS1 and PS2 which allow selection of a 5 ns, 10 ns, 14 ns and 24 ns filter setting to optimize glitch filtering for a given situation. The REXT pin is issued in conjunction with the filtering circuitry and requires a 15 k $\Omega$  resistor to ground. For additional information on Wired-OR glitch, reference Application Note AN-774.

The DS3884A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state. The combined output capacitance of the driver and receiver input is typically less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The device's unique driver circuitry meets a maximum slew rate of 0.5V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level.

Separate QV<sub>CC</sub> and QGND pins are provided to minimize the effects of high current switching noise. Output pins FR1–FR3 are the filtered outputs and R1–R6 are the unfiltered outputs. All receiver outputs are fully TTL compatible.

The DS3884A supports live insertion as defined for Futurebus+ through the LI (Live Insertion) pin. To implement live

insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the V<sub>CC</sub> pin. The DS3884A also provides power up/down glitch free protection during power sequencing.

The DS3884A has two types of power connections in addition to the LI pin. They are the Logic V<sub>CC</sub> (V<sub>CC</sub>) and the Quiet V<sub>CC</sub> (QV<sub>CC</sub>). There are two V<sub>CC</sub> pins on the DS3884A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V<sub>CC</sub> bus internal to the device, a voltage difference should never exist between these pins and the voltage difference between V<sub>CC</sub> and QV<sub>CC</sub> should never exceed  $\pm 0.5V$  because of ESD circuitry. Additionally, the ESD circuitry between the V<sub>CC</sub> pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V<sub>CC</sub> + 0.5V.

There are three different types of ground pins on the DS3884A. They are the logic ground (GND), BTL grounds (B1GND–B6GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B1GND–B6GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exist on the DS3884A, it is important to note that any voltage difference between ground pins, QGND, GND or B1GND–B6GND should not exceed  $\pm 5V$  including power up/down sequencing.

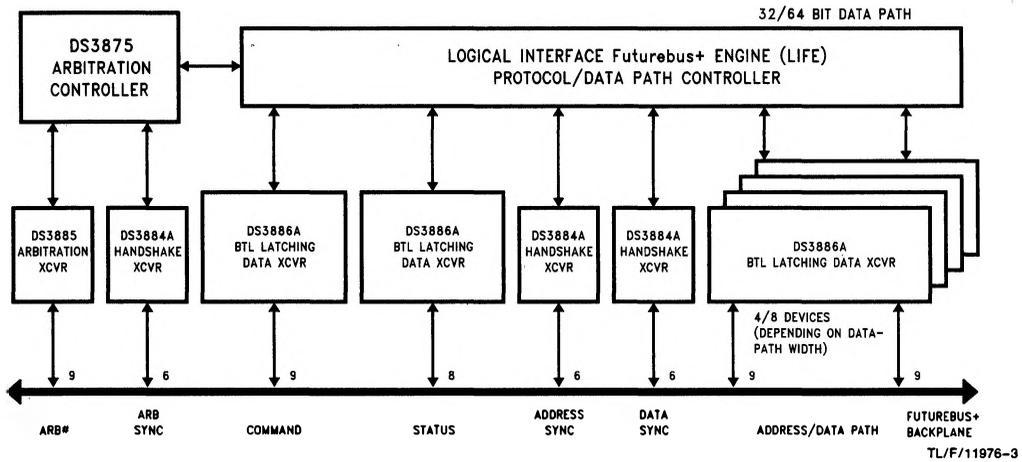
Additional transceivers included in the military Futurebus+ family are; the DS3885 BTL Arbitration Transceiver with arbitration competition logic for the AB<7:0>/ABP signal lines, and the DS3886A BTL 9-bit Latching Data Transceiver featuring edge triggered latches in the driver which may be bypassed during a fall-through mode and a transparent latch in the receiver.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjunction with the DS3884A and DS3885 transceivers.

The Logical Interface Futurebus+ Engine (LIFE) is a high performance Futurebus+ Protocol Controller designed for IEEE 896.1-1991. The LIFE will handle all handshaking signals between the Futurebus+ and the local bus interface. The Protocol Controller supports the Futurebus+ compelled mode data transfer as both master and slave. The Protocol Controller can be configured to operate in compliance to IEEE 896.2 Profile B mode. The LIFE is 896.5 compatible. The LIFE incorporates a DMA controller and 64-bit FIFO's for fast queuing.

All of the transceivers are offered in 48-pin Cerpak high density package styles.

# Typical Application



**Absolute Maximum Ratings** (Note 1)

The 883 specifications are written to reflect the Reliability Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Supply Voltage	6.5V
Control Input Voltage	6.5V
Driver Input and Receiver Output	5.5V
Receiver Input Current	± 15 mA
Bus Termination Voltage	2.4V
Power Dissipation at 125°C	0.58W

Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

**Recommended Operating Conditions**

Supply Voltage, $V_{CC}$	4.5V-5.5V
Bus Termination Voltage ( $V_T$ )	2.06V-2.14V
Operating Free Air Temperature	-55°C to +125°C

**DC Electrical Characteristics** (Notes 2 and 3)  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ 

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRIVER AND CONTROL INPUT: (Dn, DE*, PS1 and PS2)</b>						
$V_{IH}$	Minimum Input High Voltage		2.0			V
$V_{IL}$	Maximum Input Low Voltage				0.8	V
$I_I$	Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$			100	$\mu\text{A}$
$I_{IH}$	Input High Current	$V_{IN} = 2.4V$			40	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{IN} = 0.5V$			-100	$\mu\text{A}$
$V_{CL}$	Input Diode Clamp Voltage	$I_{CLAMP} = -12\text{ mA}$			-1.2	V
<b>DRIVER OUTPUT/RECEIVER INPUT: (Bn)</b>						
$V_{OLB}$	Output Low Bus Voltage (Note 5)	$Dn = 2.4V, DE^* = 0V,$ $I_{OL} = 80\text{ mA}$	0.75	1.0	1.1	V
$I_{OLBZ}$	Output Low Bus Current	$Dn = 0.5V, DE^* = 2.4V, Bn = 0.75V$			100	$\mu\text{A}$
$I_{OHBZ}$	Output High Bus Current	$Dn = 0.5V, DE^* = 2.4V, Bn = 2.1V$			100	$\mu\text{A}$
$I_{OLB}$	Output Low Bus Current	$Dn = 0.5V, DE^* = 0V, Bn = 0.75V$			220	$\mu\text{A}$
$I_{OHB}$	Output High Bus Current	$Dn = 0.5V, DE^* = 0V, Bn = 2.1V$			350	$\mu\text{A}$
$V_{TH}$	Receiver Input Threshold	$DE^* = 2.4V$	1.47	1.55	1.62	V
$V_{CLP}$	Positive Clamp Voltage	$V_{CC} = \text{Max or } 0V, I_{Bn} = 1\text{ mA}$	2.4	3.4	4.5	V
		$V_{CC} = \text{Max or } 0V, I_{Bn} = 10\text{ mA}$	2.9	3.9	5.0	V
$V_{CLN}$	Negative Clamp Voltage	$I_{CLAMP} = -12\text{ mA}$			-1.2	V
<b>RECEIVER OUTPUT: (FRn and Rn)</b>						
$V_{OH}$	Voltage Output High	$Bn = 1.1V, DE^* = 2.4V, I_{OH} = -2\text{ mA}$	2.4	3.2		V
$V_{OL}$	Voltage Output Low	$Bn = 2.1V, DE^* = 2.4V, I_{OL} = 24\text{ mA}$		0.35	0.5	V
		$Bn = 2.1V, DE^* = 2.4V, I_{OL} = 8\text{ mA}$		0.35	0.4	V
$I_{OS}$	Output Short Circuit Current	$Bn = 1.1V, DE^* = 2.4V$ (Note 4)	-40	-70	-100	mA
<b>SUPPLY CURRENT</b>						
$I_{CC}$	Supply Current: Includes $V_{CC}$ , $QV_{CC}$ and LI	$DE^* = 0.5V, \text{ All } Dn = 2.4V$		50	90	mA
		$DE^* = 2.4V, \text{ All } Bn = 2.1V$		50	80	mA
$I_{LI}$	Live Insertion Current	$DE^* = 2.4V, \text{ All } Dn = 0.5V$		1	3	mA
		$DE^* = 0.5V, \text{ All } Dn = 2.4V$		2	5	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

**DC Electrical Characteristics** (Notes 2 and 3)  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$  (Continued)

**Note 2:** All input and/or output pins shall not exceed  $V_{CC}$  plus 0.5V and shall not exceed the absolute maximum rating at anytime, including power-up and power-down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to  $QV_{CC}$  and  $V_{CC}$ . There is a diode between each input and/or output to  $V_{CC}$  which is forward biased when incorrect sequencing is applied. Alternatively, a current limiting resistor can be used when pulling-up the inputs to prevent damage. The current into any input/output pin shall be no greater than 50 mA. Exception, I1 and Bn pins do not have power sequencing requirements with respect to  $V_{CC}$  and  $QV_{CC}$ . Furthermore, the difference between  $V_{CC}$  and  $QV_{CC}$  should never be greater than 0.5V at any time including power-up.

**Note 3:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions:  $V_{CC} = 5V$  and  $T_A = 25^\circ\text{C}$  unless otherwise stated.

**Note 4:** Only one output should be shorted at a time, and duration of the short should not exceed one second.

**Note 5:** Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.

**AC Electrical Characteristics**  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$  (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRIVER</b>						
$t_{PHL}$	Dn to Bn Prop. Delay	$DE^* = 0V$ (Figures 1, 2)	1		7	ns
$t_{PLH}$			1		6	ns
$t_{PHL}$	DE* to Bn Enable Time	$Dn = 3V$ (Figures 1, 3)	2	4	9	ns
$t_{PLH}$	Disable Time		2	4	7	ns
$t_r$	Transition Time—Rise/Fall 20% to 80%	(Figures 1, 2)	1	2	3.5	ns
$t_f$			1	2	4.5	ns
SR	Skew Rate is Calculated from 1.3V to 1.8V	(Note 11)			0.5	V/ns
$t_{skew}$	Skew between Drivers in the Same Package	(Note 7)		1	5	ns
<b>RECEIVER</b>						
$t_{PHL}$	Bn to Rn Prop. Delay	$DE^* = 3V$ (Figures 4, 5)	2		6	ns
$t_{PLH}$			2		6	ns
$t_{skew}$	Skew between Receivers in Same Package	(Note 7)			3	ns
<b>FILTERED RECEIVER</b>						
$t_{PHL}$	Bn to FRn Prop. Delay	$PS1 = 0V$ $PS2 = 0V$ $DE^* = 3V$ (Figures 4, 5), $R_{EXT} = 15 k\Omega$	6	13	17	ns
		$PS1 = 0V$ $PS2 = 3V$ $DE^* = 3V$ (Figures 4, 5), $R_{EXT} = 15 k\Omega$	11	16	23	ns
		$PS1 = 3V$ $PS2 = 0V$ $DE^* = 3V$ (Figures 4, 5), $R_{EXT} = 15 k\Omega$	16	21	29	ns
		$PS1 = 3V$ $PS2 = 3V$ $DE^* = 3V$ (Figures 4, 5), $R_{EXT} = 15 k\Omega$	22	33	49	ns
$t_{PLH}$	Bn to FRn Prop. Delay	$DE^* = 3V$ (Figures 4, 5) (Note 8) $R_{EXT} = 15 k\Omega$	2		8	ns
$t_{GR}$	Glitch Rejection	$PS1 = 0V$ $PS2 = 0V$ $DE^* = 3V$ (Figures 4, 6), $R_{EXT} = 15 k\Omega$	5		16	ns
		$PS1 = 0V$ $PS2 = 3V$ $DE^* = 3V$ (Figures 4, 6), $R_{EXT} = 15 k\Omega$	10		21	ns
		$PS1 = 3V$ $PS2 = 0V$ $DE^* = 3V$ (Figures 4, 6), $R_{EXT} = 15 k\Omega$	14		27	ns
		$PS1 = 3V$ $PS2 = 3V$ $DE^* = 3V$ (Figures 4, 6), $R_{EXT} = 15 k\Omega$	20		47	ns

## AC Electrical Characteristics $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{CC} = 5\text{V} \pm 10\%$ (Note 6) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
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### FILTERED RECEIVER TIMING REQUIREMENTS

$t_s$	PSn to Bn	Set-Up Time	(Figure 7), $R_{EXT} = 15\text{ k}\Omega$	250		ns
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### PARAMETERS NOT TESTED

Output	Capacitance at Bn	(Note 9)		5		pF
$t_{NR}$	Noise Rejection	(Note 10)		1		ns

**Note 6:** Input waveforms shall have a rise/fall time of 3 ns.

**Note 7:**  $t_{skew}$  is an absolute value defined as differences seen in propagation delays between drivers in the same package with identical load conditions.

**Note 8:** Filtered receiver  $t_{PLH}$  is independent of filter setting.

**Note 9:** The parameter is tested using TDR techniques described in P1194.0 BTL Backplane Design Guide.

**Note 10:** This parameter is tested during device characterization. The measurements revealed that the part will reject 1 ns pulse width.

**Note 11:** Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5 $\Omega$  tied to +2.1V DC.

## Pin Descriptions

Pin Name	Number of Pins	Input/Output	Description
B1–B6	6	I/O	BTL receiver input and driver output
B1GND–B6GND	6	NA	Driver output ground reduces bounce due to high current switching of driver outputs (Note 12)
DE*	1	I	Driver Enable Low
D1–D6	6	I	TTL Driver Input
FR1–FR3	3	O	TTL Filtered Receiver Output
GND	3	NA	Ground reference for switching circuits. (Note 12)
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (Note 13)
NC	8	NA	No Connect
PS1, PS2	2	I	Pulse Width Selection pin determines glitch filter setting (Note 14)
R1–R6	6	O	TTL Receiver Output
REXT	1	NA	External Resistor pin. External resistor is used for internal biasing of filter circuitry. The 15 k $\Omega$ resistor shall be connected between REXT and GND. The resistor shall have a tolerance of 1% and a temperature coefficient of 100 ppm/ $^{\circ}\text{C}$ or better.
QGND	2	NA	Ground reference for receiver input bandgap reference and non-switching circuits (Note 12)
QV <sub>CC</sub>	1	NA	V <sub>CC</sub> supply for bandgap reference and non-switching circuits (Note 13)
V <sub>CC</sub>	2	NA	V <sub>CC</sub> supply for switching circuits (Note 13)

**Note 12:** The multiplicity of grounds reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low inductance (i.e., ground plane with power pins and many signal pins connected to the backplane ground). If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.

**Note 13:** The same considerations for ground are used for V<sub>CC</sub> in reducing lead inductance (see Note 12). QV<sub>CC</sub> and V<sub>CC</sub> should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV<sub>CC</sub> and V<sub>CC</sub>.

**Note 14:** See AC characteristics for filter setting.

### Truth Table

DE*	Dn	FRn	Rn	Bn
H	X	H	H	L
H	X	L	L	H
L	H	H	H	L
L	L	L	L	H

**Note 1:** X: High or low logic state

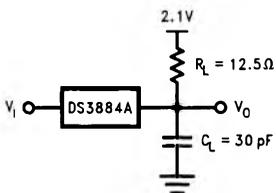
**Note 2:** L: Low state

**Note 3:** H: High state

**Note 4:** L-H: Low to high transition

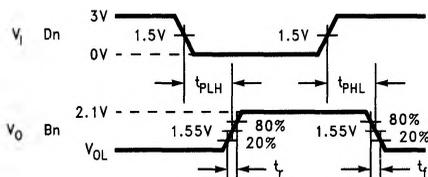
### Glitch Filter Table

PS1	PS2	Filter Setting
L	L	5 ns
L	H	10 ns
H	L	14 ns
H	H	20 ns



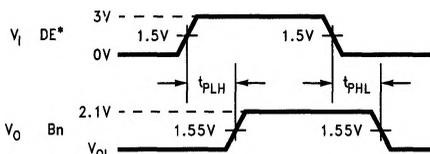
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**FIGURE 1. Driver Propagation Delay Set-Up**



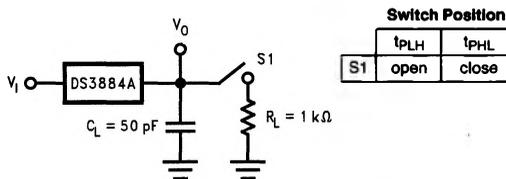
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**FIGURE 2. Driver: Dn to Bn**



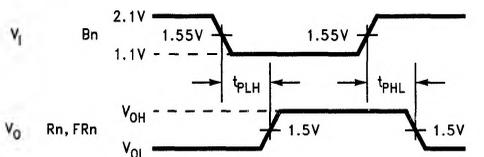
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**FIGURE 3. Driver: DE\* to Bn**



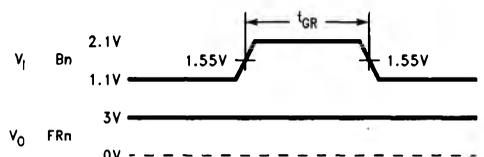
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**FIGURE 4. Receiver Propagation Delay Set-Up**



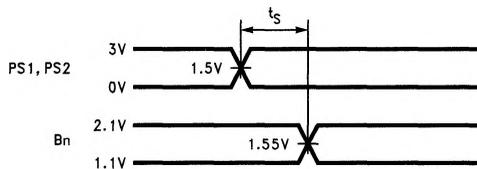
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**FIGURE 5. Receiver: Bn to FRn, Bn to Rn**



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**FIGURE 6. Receiver: tGR, FRn(min) = 2V**



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**FIGURE 7. Receiver: PSn to Bn**