National Semiconductor

DS3893A BTL TURBOTRANSCEIVER™

General Description

The TURBOTRANSCEIVER is designed for use in very high speed bus systems. The bus terminal characteristics of the TURBOTRANSCEIVER are referred to as "Backplane Transceiver Logic" (BTL). BTL is a new logic signaling standard that has been developed to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard eliminates the settling time delays, that severely limit the TTL bus performance, to provide significantly higher bus transfer rates.

The TURBOTRANSCEIVER is compatible with the requirements of the proposed IEEE 896 Futurebus draft standard. It is similar to the DS3896/97 BTL TRAPEZOIDAL Transceivers but the trapezoidal feature has been removed to improve the propagation delay. A stripline backplane is therefore required to reduce the crosstalk induced by the faster rise and fall times. This device can drive a 10Ω load with a typical propagation delay of 3.5 ns for the driver and 5 ns for the receiver.

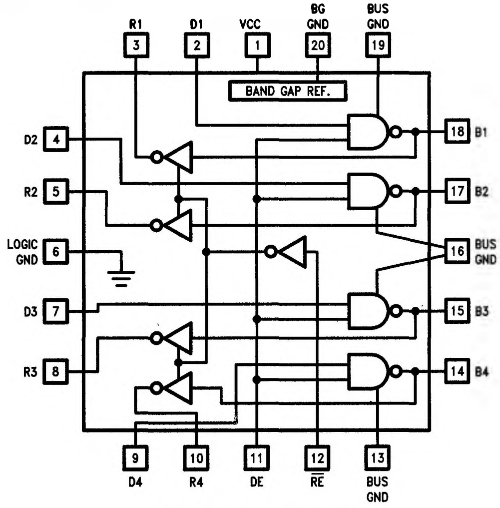
When multiple devices are used to drive a parallel bus, the driver enables can be tied together and used as a common control line to get on and off the bus. The driver enable delay is designed to be the same as the driver propagation delay in order to provide maximum speed in this configuration. The low input current on the enable pin eases the drive required for the common control line.

The bus driver is an open collector NPN with a Schottky diode in series to isolate the transistor output capacitance from the bus when the driver is in the inactive state. The active output low voltage is typically 1V. The bus is intended to be operated with termination resistors (selected to match the bus impedance) to 2.1V at both ends. Each of the resistors can be as low as 20Ω.

Features

- Fast single ended transceiver (typical driver enable and receiver propagation delays are 3.5 ns and 5 ns)
- Backplane Transceiver Logic (BTL) levels (1V logic swing)
- Less than 5 pF bus-port capacitance
- Drives densely loaded backplanes with equivalent load impedances down to 10Ω
- 4 transceivers in 20 pin PCC package
- Specially designed for stripline backplanes
- Separate bus ground returns for each driver to minimize ground noise
- High impedance, MOS and TTL compatible inputs
- TRI-STATE® control for receiver outputs
- Built-in bandgap reference provides accurate receiver threshold
- Glitch free power up/down protection on all outputs
- Oxide isolated bipolar technology

Connection and Logic Diagram



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Order Number DS3893AV
See NS Package Number V20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.5V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Driver Output Receiver Input Clamp Current	±15 mA
Power Dissipation at 70°C	900 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 3 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Bus Termination Voltage (V_T)	2.0	2.2	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics (Notes 2, 3 and 4) $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT: (DE, $\overline{RE}$, Dn)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_I	Input Leakage Current	DE = $\overline{RE}$ = Dn = V_{CC}			100	µA
I_{IH}	Input High Current	DE = $\overline{RE}$ = Dn = 2.5V			20	µA
I_{IL}	Dn Input Low Current	Dn = 0.5V, DE = V_{CC} = Max			−200	µA
	DE Input Low Current	DE = 0.5V, Dn = V_{CC} = Max			−500	µA
	$\overline{RE}$ Input Low Current	$\overline{RE}$ = 0.5V, V_{CC} = Max			−100	µA
V_{CL}	Input Diode Clamp Voltage	$I_{clamp} = -12$ mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT: (Bn)						
V_{OLB}	Output Low Bus Voltage	Dn = DE = V_{IH} *(Figure 2)* $R_T = 10\Omega$, $V_T = 2.2V$	0.75	1.0	1.2	V
		Dn = DE = V_{IH} *(Figure 2)* $R_T = 18.5\Omega$, $V_T = 2.14$	0.75	1.0	1.1	V
I_{ILB}	Output Bus Current (Power On)	Dn = DE = 0.8V, V_{CC} = Max Bn = 0.75V	−250		100	µA
I_{IHB}	Output Bus Current (Power Off)	Dn = DE = 0.8V, V_{CC} = 0V Bn = 1.2V			100	µA
V_{OCB}	Driver Output Positive Clamp	V_{CC} = Max or 0V, Bn = 1 mA			2.9	V
		V_{CC} = Max or 0V, Bn = 10 mA			3.2	V
V_{OHB}	Output High Bus Voltage	V_{CC} = Max, Dn = 0.8V *(Figure 2)* $V_T = 2.0V$, $R_T = 10\Omega$	1.90			V
V_{TH}	Receiver Input Threshold		1.47	1.55	1.62	V
RECEIVER OUTPUT: (Rn)						
V_{OH}	Voltage Output High	Bn = 1.2V, $I_{oh} = -3$ mA, $\overline{RE}$ = 0.8V	2.5V			V
V_{OL}	Voltage Output Low	Bn = 2V, I_{ol} = 6 mA, $\overline{RE}$ = 0.8V		0.35	0.5	V
I_{OZ}	TRI-STATE Leakage	V_o = 2.5V, $\overline{RE}$ = 2V			20	µA
		V_o = 0.5V, $\overline{RE}$ = 2V			−20	µA
I_{OS}	Output Short Circuit Current (Note 5)	Bn = 1.2V, V_o = 0V $\overline{RE}$ = 0.8V, V_{CC} = Max	−80	−120	−200	mA
I_{CC}	Supply Current	Dn = DE = $\overline{RE}$ = V_{IH}, V_{CC} = Max		70	95	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: Unused inputs should not be left floating. Tie unused inputs to either V_{CC} or GND thru a resistor.

Note 5: Only one output at a time should be shorted.

Switching Characteristics T_A = 0 to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER: (*Figures 3* and *6*)						
t_{PHL}	Driver Input to Output	V_T = 2V R_T = 10Ω, C_L = 30 pF, DE = 3V	1	3.5	7	ns
t_{PLH}	Driver Input to Output	V_T = 2V, R_T = 10Ω, C_L = 30 pF, DE = 3V	1	3.5	7	ns
t_r	Output Rise time	V_T = 2V, R_T = 10Ω, C_L = 30 pF, DE = 3V	1	2	5	ns
t_f	Output Fall Time	V_T = 2V, R_T = 10Ω, C_L = 30 pF, DE = 3V	1	2	5	ns
t_{skew}	Skew Between Drivers in Same Package	(Note 1)		1		ns
DRIVER ENABLE: (*Figures 3* and *6*)						
t_{PHL}	Enable Delay	V_T = 2V, R_T = 10Ω, C_L = 30 pF, Dn = 3V	1	3.5	7	ns
t_{PLH}	Disable Delay	V_T = 2V, R_T = 10Ω, C_L = 30 pF, Dn = 3V	1	3.5	7	ns
RECEIVER: (*Figures 4* and *7*)						
t_{PHL}	Receiver Input to Output	C_L = 50 pF, $\overline{RE}$ = DE = 0.3V, S3 Closed	2	5	8	ns
t_{PLH}	Receiver Input to Output	C_L = 50 pF, $\overline{RE}$ = DE = 0.3V, S3 Open	2	5	8	ns
t_{skew}	Skew Between Receivers in Same Package	(Note 1)		1		ns
RECEIVER ENABLE: (*Figures 5* and *8*)						
t_{ZL}	Receiver Enable to Output Low	C_L = 50 pF, R_L = 500, DE = 0.3V S2 Open Bn = 2V	2	6	12	ns
t_{ZH}	Receiver Enable to Output High	C_L = 50 pF, R_L = 500, DE = 0.3V S1 Open Bn = 1V	2	5	12	ns
t_{LZ}	Receiver Disable From Output Low	C_L = 50 pF, R_L = 500, DE = 0.3V S2 Open Bn = 2V	1	5	8	ns
t_{HZ}	Receiver Disable From Output High	C_L = 50 pF, R_L = 500, DE = 0.3V S1 Open Bn = 1V	1	4	8	ns

Note 1: t_D and t_R skew is an absolute value, defined as differences seen in propagation delays between each of the drivers or receivers in the same package of the same delay, V_{CC}, temperature and load conditions.

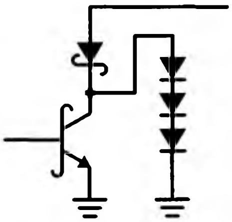

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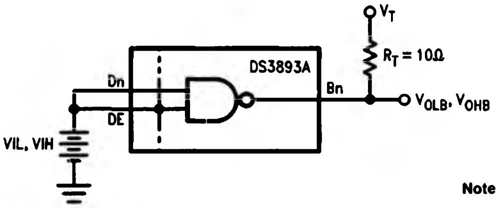
FIGURE 1. Equivalent Bus Output



Note: n = 1, 2, 3, 4

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FIGURE 2. Driver Output Voltage

AC Test Circuits

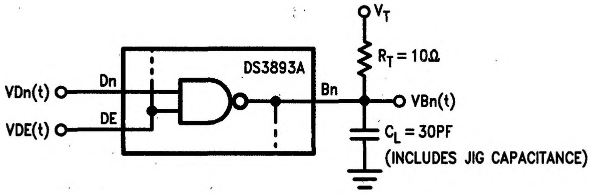

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FIGURE 3

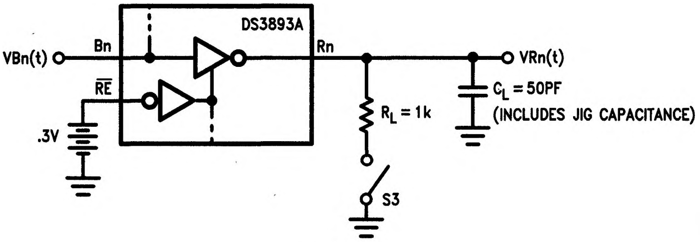

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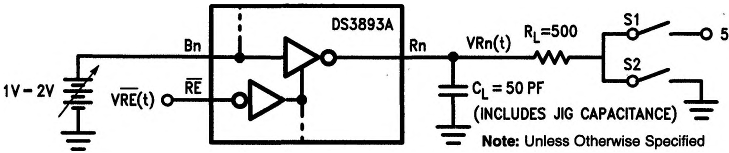
FIGURE 4



Note: Unless Otherwise Specified
The Switches are Closed

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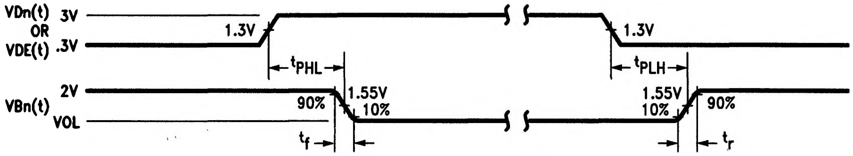
FIGURE 5

Switching Time Waveforms



$t_R = t_F \leq 4$ns FROM 10% TO 90%

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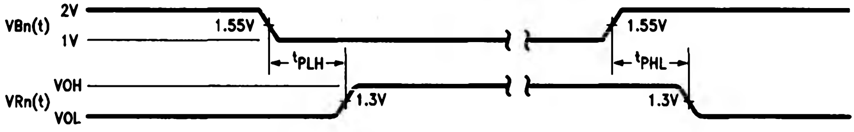
FIGURE 6. Driver Propagation Delay



$t_R = t_F \leq 4$ns FROM 10% TO 90%

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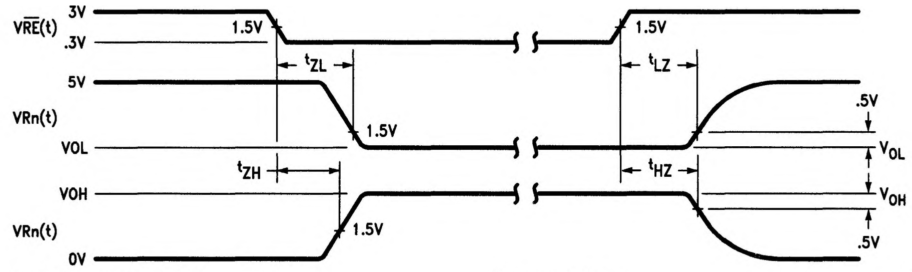
FIGURE 7. Receiver Propagation Delay

Switching Time Waveforms (Continued)



Note: $t_R = t_F \leq 4$ ns From 10% to 90%

Note: n = 1, 2, 3, 4

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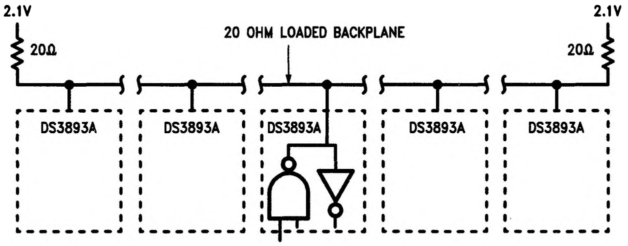
FIGURE 8. Receiver Enable and Disable Times

Typical Application



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Application Information

Due to the high current and very high speed capability of the TURBOTRANSCEIVER's driver output stage, circuit board layout and bus grounding are critical factors that affect the system performance.

Each of the TURBOTRANSCEIVER's bus ground pins should be connected to the nearest backplane ground pin with the shortest possible path. The ground pins on the connector should be distributed evenly through its length.

Although the bandgap reference receiver threshold provides sufficient DC noise margin *(Figure 9)*, ground noise and ringing on the data paths could easily exceed this margin if the series inductance of the traces and connectors are not kept to a minimum. The bandgap ground pin should be returned to the connector through a separate trace that does not carry transient switching currents. The transceivers should be mounted as close as possible to the connector. It should be noted that even one inch of trace can add a significant amount of ringing to the bus signal.

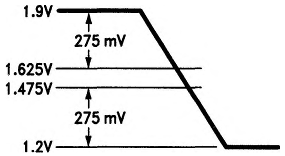

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FIGURE 9. Noise Margin

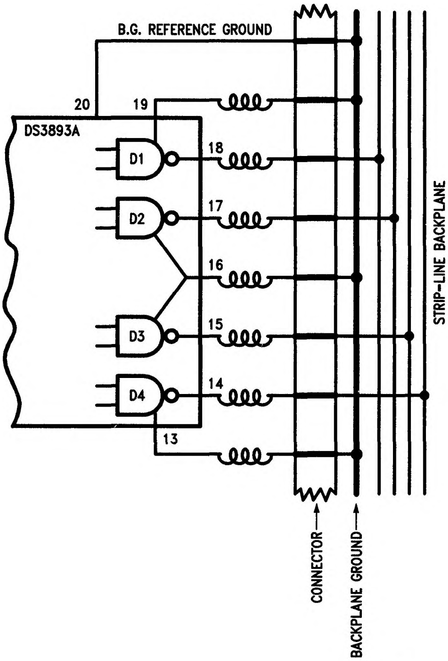

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FIGURE 10