

DS50EV401 2.5 Gbps / 5.0 Gbps or 8.0 Gbps Quad Cable and Backplane Equalizer

Check for Samples: [DS50EV401](#)

FEATURES

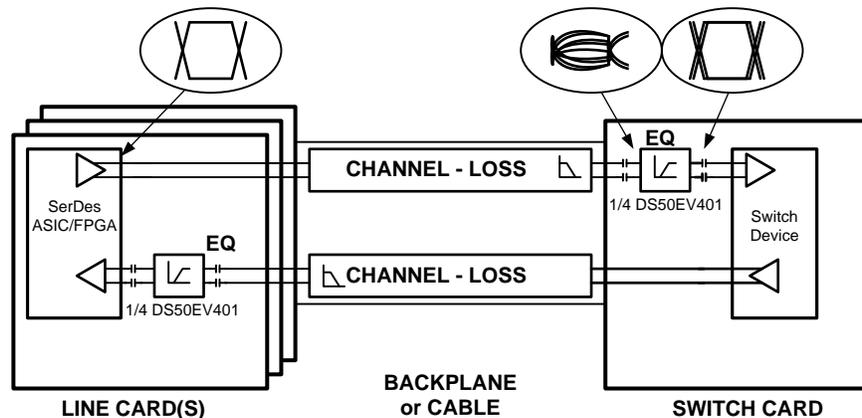
- Automatic power management on an individual lane basis
- Data rate optimized equalization
- Operates over 7 meter of 24 AWG Twin-ax Cables up to 8 Gbps
- Typical residual deterministic jitter:
 - 0.18 UI @ 8 Gbps w/ 30" of FR4
 - 0.18 UI @ 5 Gbps w/ 40" of FR4
 - 0.16 UI @ 2.5 Gbps w/ 40" of FR4
- 8 kV HBM ESD protection
- -40 to 85°C operating temperature range
- 7 mm x 7 mm 48-pin leadless WQFN package
- Single power supply of either 3.3V or 2.5V
- Low power (typically 95 mW per channel at 2.5V V_{DD})

DESCRIPTION

The DS50EV401 is a low power, programmable equalizer specifically designed to reduce inter-symbol interference (ISI) induced by a variety of interconnect media. In all modes, the equalizer can operate, error free, with an input eye that is completely closed by interconnect ISI. The MODE control, allows the user to select between equalization settings for 8.0 Gbps operation or 2.5 Gbps / 5.0 Gbps operation.

The DS50EV401 uses Current-mode logic (CML) on both input and output ports, which provide constant 50 ohm single-ended impedance to AC ground. Differential signaling is implemented through out the entire signal path to minimize supply induced jitter. The DS50EV401 is available in a 7mm x 7mm 48-pin leadless WQFN package, and is powered from a single power supply of either 3.3 or 2.5V.

Application Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
IN_0+ IN_0-	1 2	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_0+ to VDD and IN_0- to VDD.
IN_1+ IN_1-	4 5	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_1+ to VDD and IN_1- to VDD.
IN_2+ IN_2-	8 9	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_2+ to VDD and IN_2- to VDD.
IN_3+ IN_3-	11 12	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 50Ω terminating resistor connects IN_3+ to VDD and IN_3- to VDD.
OUT_0+ OUT_0-	36 35	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_0+ to V _{DD} and OUT_0- to V _{DD} .
OUT_1+ OUT_1-	33 32	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_1+ to V _{DD} and OUT_1- to V _{DD} .
OUT_2+ OUT_2-	29 28	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_2+ to V _{DD} and OUT_2- to V _{DD} .
OUT_3+ OUT_3-	26 25	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_3+ to V _{DD} and OUT_3- to V _{DD} .
EQUALIZATION CONTROL			
MODE	14	I, LVCMOS	MODE selects the equalizer frequency for EQ channels. MODE is internally pulled low. L = 6.0 - 8.0 Gbps setting H = 2.5 Gbps / 5.0 Gbps setting
DEVICE CONTROL			
EN0	44	I, LVCMOS	Channel 0 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
EN1	42	I, LVCMOS	Channel 1 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
EN2	40	I, LVCMOS	Channel 2 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
EN3	38	I, LVCMOS	Channel 3 Enable Input Pin H = normal operation (enabled) L = standby mode Pin is internally pulled High.
SD0	45	O, LVCMOS	Channel 0 Signal Detect Output Pin H = signal detected L = no signal detected
SD1	43	O, LVCMOS	Channel 1 Signal Detect Output Pin H = signal detected L = no signal detected
SD2	41	O, LVCMOS	Channel 2 Signal Detect Output Pin H = signal detected L = no signal detected.
SD3	39	O, LVCMOS	Channel 3 Signal Detect Output Pin H = signal detected L = no signal detected
POWER			
V _{DD}	3, 6, 7, 10, 13, 15, 46	Power	V _{DD} = 2.5V ± 5% or 3.3V ± 10%. V _{DD} pins should be tied to V _{DD} plane through low inductance path. A 0.1μF bypass capacitor should be connected between each V _{DD} pin to GND planes.
GND	22, 24, 27, 30, 31, 34	Ground	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
Exposed Pad	DAP	Ground	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board.

PIN DESCRIPTIONS (continued)

Pin Name	Pin Number	I/O, Type	Description
OTHER			
Reserv	16, 17, 18, 19, 20, 21, 23, 37, 47, 48		Reserved. Do not connect. Leave open.

Connection Diagram

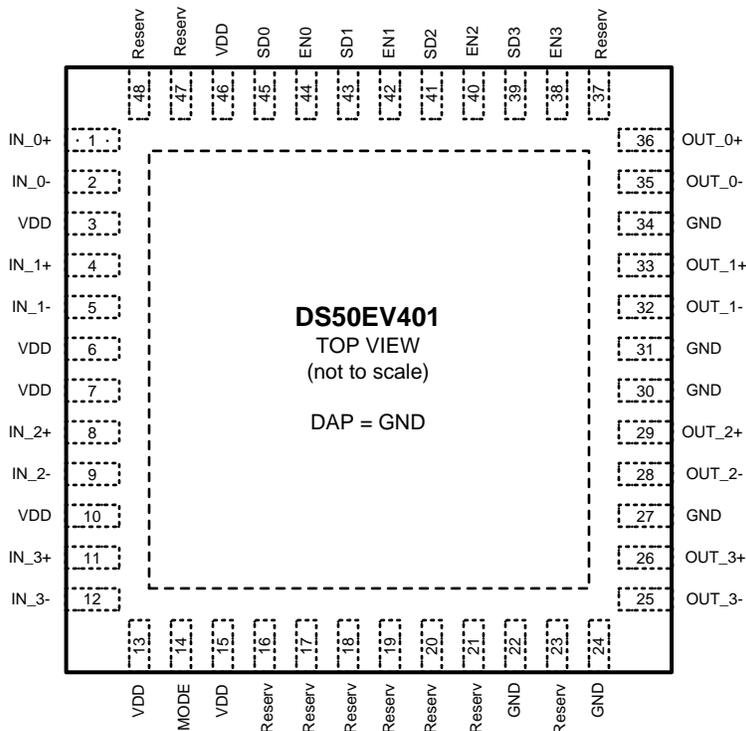


Figure 1. TOP VIEW — Not to scale



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

Supply Voltage (V_{DD})	-0.5V to +4.0V
LVC MOS Input Voltage	-0.5V + 4.0V
LVC MOS Output Voltage	-0.5V to 4.0V
CML Input/Output Voltage	-0.5V to 4.0V
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
ESD Rating	
HBM, 1.5 k Ω , 100 pF	>8 kV
Thermal Resistance θ_{JA} , No Airflow	30°C/W

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are specified for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.
- (2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DD} to GND, or	2.375	2.5	2.625	V
V_{DD} to GND	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless other specified. ^{(1) (2)}

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER						
PD	Power Dissipation 3.3V Operation	Signal active, $V_{DD} = 3.3V, 3.6V$		510	700	mW
		No signal, $V_{DD} = 3.3V, 3.6V$			100	mW
PD	Power Dissipation 2.5V Operation	Signal active, $V_{DD} = 2.5V, 2.625V$		380	490	mW
		No signal, $V_{DD} = 2.5V, 2.625V$		30		mW
N	Supply Noise Tolerance ⁽³⁾	Up to 50 MHz		100		mV _{P-P}
LVC MOS / LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	3.3V Operation	2.0		V_{DD}	V
		2.5V Operation	1.6		V_{DD}	V
V_{IL}	Low Level Input Voltage		-0.3		0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -3mA, 3.3V$ Operation	2.4			V
		$I_{OH} = -3mA, 2.5V$ Operation	2.0			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 3mA$			0.4	V
I_{IH}	Input High Current	$V_{IN} = V_{DD}$, MODE pin (pull down)			+140	μA
		$V_{IN} = V_{DD}$, EN pins (pull up)	-15		+15	μA
I_{IL}	Input Low Current	$V_{IN} = 0V$, MODE pin (pull down)	-15		+15	μA
		$V_{IN} = 0V$, EN pins (pull up)	-40			μA

- (1) Typical values represent most likely parametric norms at $V_{DD} = 3.3V$ or $2.5V$, $T_A = 25^\circ C$., and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified. ⁽¹⁾ ⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CML RECEIVER INPUTS (IN_{n+}, IN_{n-})						
V _{TX}	Input Voltage Swing (Launch Amplitude)	Measured at point A, AC or DC coupled, Figure 2	400	1000	1600	mV _{P-P}
V _{IN-S}	Input Voltage Sensitivity	AC-Coupled or DC-Coupled Required Differential Envelope measured at point B, Figure 2 , ⁽⁴⁾ , See FR4 / BACKPLANE Typical Performance Eye Diagrams ,		170		mV _{P-P}
R _{LI}	Differential Input Return Loss	100 MHz – 4.0 GHz, with fixture's effect de-embedded		10		dB
R _{IN}	Input Resistance	Single ended to V _{DD}	40	50	60	Ω
CML OUTPUTS (OUT_{n+}, OUT_{n-})						
V _O	Output Voltage Swing	Differential measurement with OUT _{n+} and OUT _{n-} terminated by 50Ω to GND AC-Coupled, Figure 3	800	1000	1200	mV _{P-P}
V _{OCM}	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω termination, ⁽⁵⁾		V _{DD} – 0.25		V
t _R , t _F	Transition Time	20% to 80% of differential output voltage, measured within 1" from output pins, Figure 3 , ⁽⁵⁾		40		ps
R _O	Output Resistance	Single-ended to V _{DD}	40	50	60	Ω
R _{LO}	Differential Output Return Loss	100 MHz – 4.0 GHz, with fixture's effect de-embedded. IN _{n+} = static high		10		dB
t _{PLHD}	Differential Low to High Propagation Delay	Propagation delay measurement at 50% V _O between input to output, 100 Mbps, Figure 4 , ⁽⁶⁾		240		ps
t _{PHLD}	Differential High to Low Propagation Delay			240		ps
t _{ID}	Idle to Valid Differential Data	V _{IN} = 800 mVp-p, 5 Gbps, EIEOS, 40" of 6 mil microstrip FR4, Figure 5 , ⁽⁷⁾		8		ns
t _{DI}	Valid Differential data to idle	V _{IN} = 800 mVp-p, 5 Gbps, EIOS, 40" of 6 mil microstrip FR4, Figure 5 , ⁽⁷⁾		8		ns
t _{CCSK}	Inter Pair Channel to Channel Skew	Difference in 50% crossing between channels		7		ps
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 8 Gbps	30" of 6 mil microstrip FR4, MODE=0, PRBS-7 (2 ⁷ -1) pattern, ⁽⁷⁾ ⁽⁸⁾		0.18		UI _{P-P}
DJ2	Residual Deterministic Jitter at 5 Gbps	40" of 6 mil microstrip FR4, MODE=1, PRBS-7 (2 ⁷ -1) pattern, ⁽⁷⁾ ⁽⁸⁾		0.18	0.21	UI _{P-P}
DJ3	Residual Deterministic Jitter at 2.5 Gbps	40" of 6 mil microstrip FR4, MODE=1, PRBS-7 (2 ⁷ -1) pattern, ⁽⁷⁾ ⁽⁸⁾		0.16	0.18	UI _{P-P}
RJ	Random Jitter	⁽⁶⁾ ⁽⁹⁾		0.5		psrms

- (4) V_{IN-S} is a measurement of the input differential envelope, see [FR4 / BACKPLANE Typical Performance Eye Diagrams](#). The device does not require an open eye.
- (5) Specification is ensured by characterization at optimal MODE setting and is not tested in production.
- (6) Measured with clock-like {11111 00000} pattern.
- (7) Specification is ensured by characterization at optimal MODE setting and is not tested in production.
- (8) Deterministic jitter is measured at the differential outputs (point C of [Figure 2](#)), minus the deterministic jitter before the test channel (point A of [Figure 2](#)). Random jitter is removed through the use of averaging or similar means.
- (9) Random jitter contributed by the equalizer is defined as sqrt(J_{OUT}² – J_{IN}²). J_{OUT} is the random jitter at equalizer outputs in ps-rms, see point C of [Figure 2](#); J_{IN} is the random jitter at the input of the equalizer in ps-rms, see point B of [Figure 2](#).

TIMING DIAGRAMS

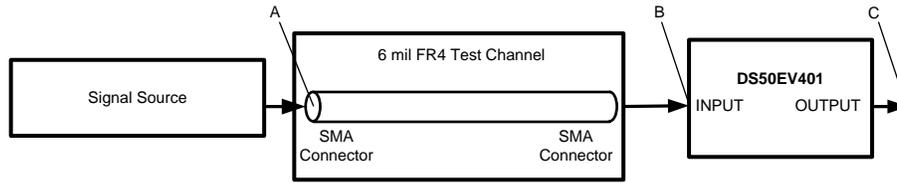


Figure 2. Test Setup Diagram

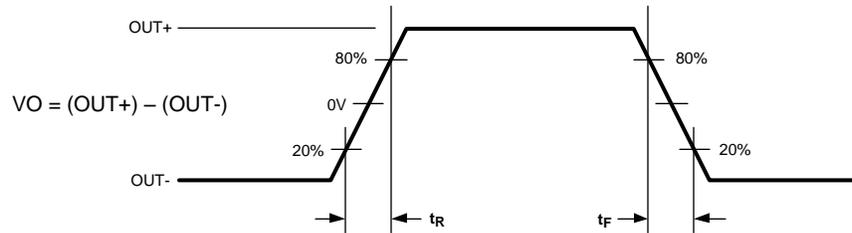


Figure 3. CML Output Transition Times

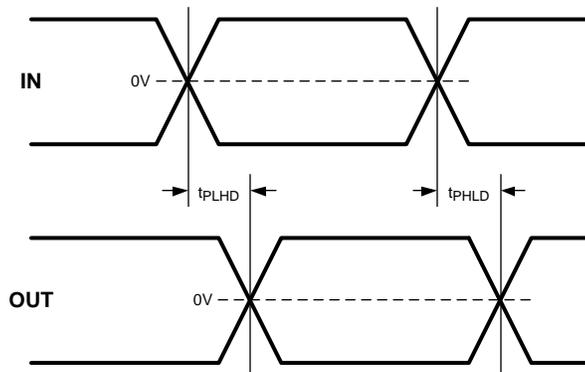


Figure 4. Propagation Delay Timing Diagram

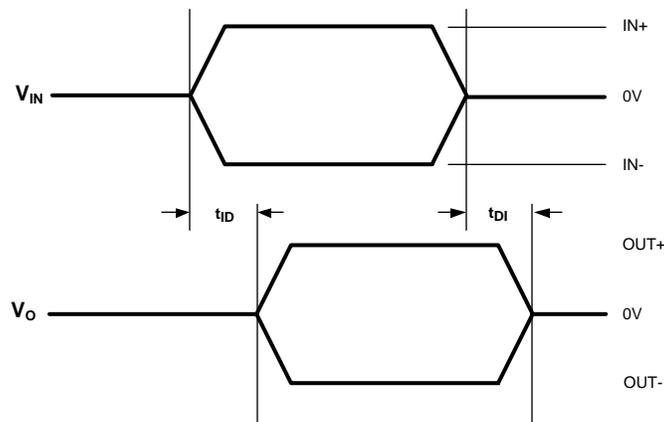


Figure 5. Idle Timing Diagram

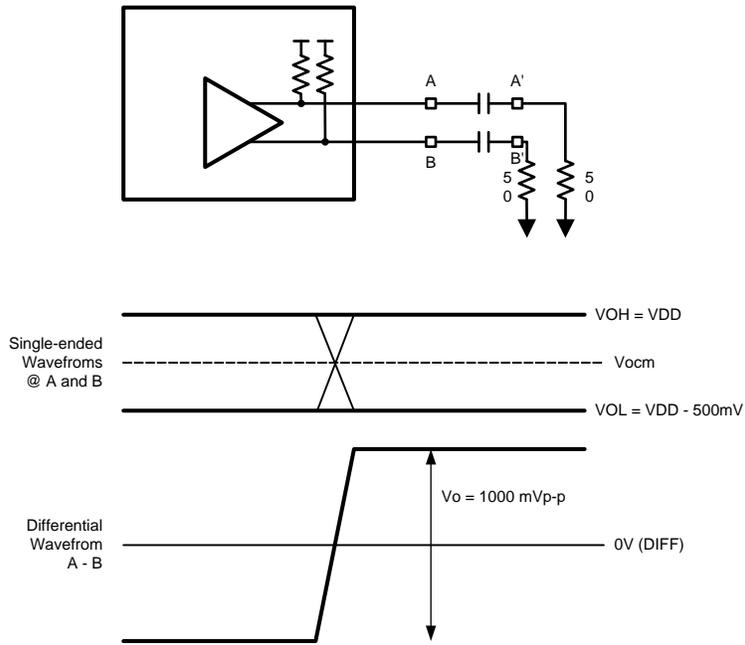


Figure 6. CML Output Swings at A/B

FUNCTIONAL DESCRIPTION

DS50EV401 APPLICATIONS INFORMATION

The DS50EV401 is a programmable quad equalizer optimized for copper backplanes and cables at transmission rates of 2.5 Gbps up to 8 Gbps. The device consists of an input receive equalizer followed by a limiting amplifier. The equalizer is designed to open an input eye that is completely closed due to inter-symbol interference (ISI) induced by the channel interconnect. The equalization is set to keep residual deterministic jitter below 0.2 unit intervals (UI) regardless of data rate. This equalization scheme allows one equalization setting to satisfy most serial links between 2.5 and 5.0 Gbps. The DS50EV401 is intended as a unidirectional receiver that should be placed in close physical proximity to the link end point. Therefore the transmitter does not include de-emphasis as TX equalization would not be needed over the short distance between the equalizer and the end point.

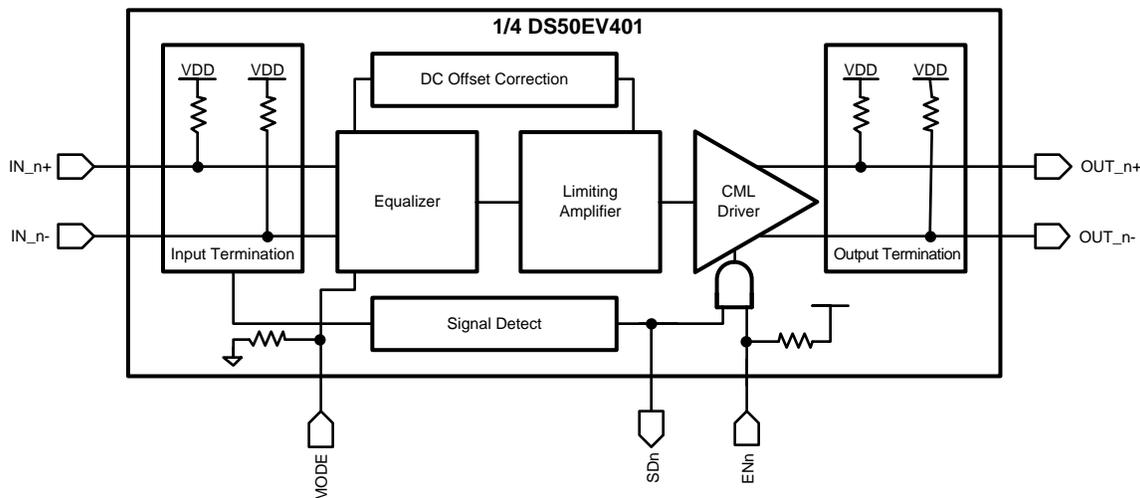


Figure 7. General Block Diagram

Data Channels

The DS50EV401 consists of four data channels. Each channel provides input termination, receiver equalization, signal limiting, offset cancellation, and a CML output driver, as shown in Figure 7. The data channels support two levels of equalization, controlled by the pin MODE. The equalization levels are set simultaneously on all 4 channels, as described in Table 1.

When an idle condition is sensed on a channel's input, the transmit driver is automatically placed into electrical idle mode. The common mode voltage is set, and the differential output is forced to zero. To save power, the output driver current is powered off when the device is in electrical idle mode. All other circuits maintain their bias currents allowing a fast recovery from idle to the active state. Electric idle is performed on a per channel basis, and several channels can be in idle while others are actively passing data.

Table 1. MODE Control Table

6 mil microstrip FR4 trace length (in)	24 AWG Twin-AX cable length (m)	Frequency	Channel Loss	MODE
0–30	0–7	8 Gbps	16 dB	0
0–40	0–10	2.5 Gbps 5.0 Gbps	14 dB 20 dB	1

APPLICATION INFORMATION

GENERAL RECOMMENDATIONS

The DS50EV401 is a high performance device capable of delivering excellent performance. As with most CML devices, it is recommended that AC coupling capacitors be used to ensure I/O compatibility with other devices. In order to extract full performance from the device in a particular application, good high-speed design practices must be followed. TI's LVDS Owner's Manual (literature number [SNLA187](#)), provides detailed information about managing signal integrity and power delivery to get the most from your design.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route CML lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the CML signals away from other signals and noise sources on the printed circuit board. See AN-1187 ([SNOA401](#)) for additional information on WQFN packages.

PACKAGE FOOTPRINT / SOLDERING

See Application Note number 1187, "Leadless Leadframe Package" for information on PCB footprint and soldering recommendations.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS50EV401 is provided with an adequate power supply. First, the supply (V_{DD}) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1μF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS50EV401. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 μF to 10 μF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS50EV401.

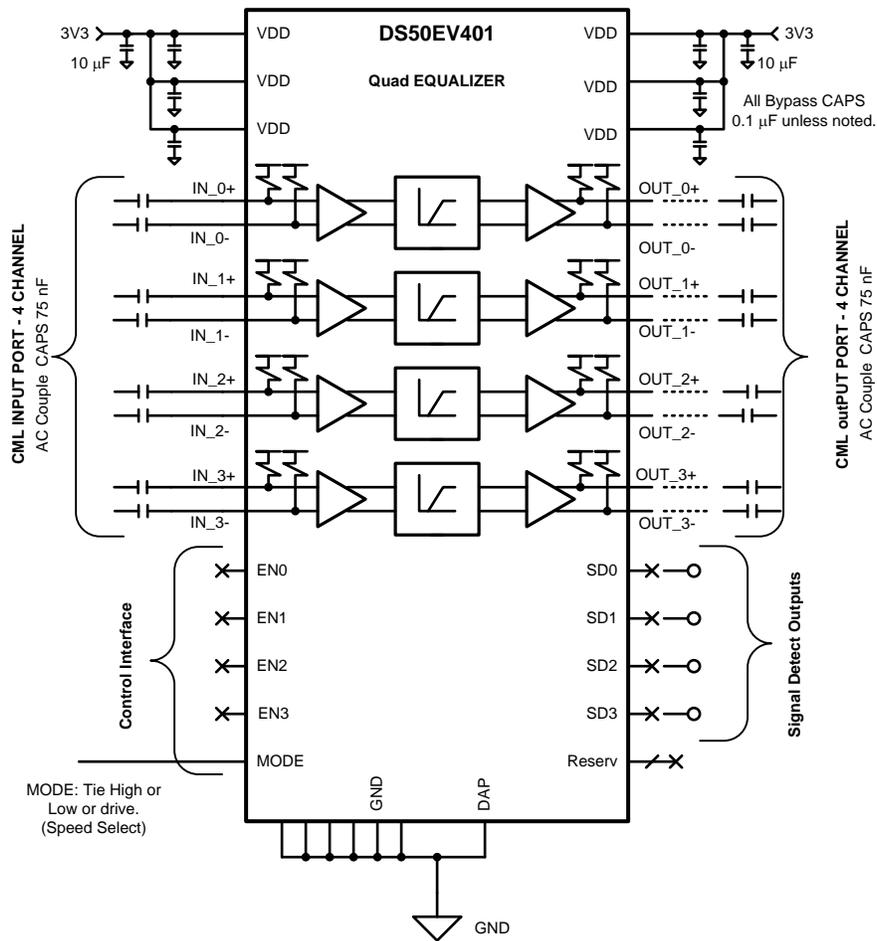


Figure 8. Typical Interface Circuit

The CML inputs are AC coupled to the device as shown in [Figure 8](#). Internal to the device are 50Ω terminations to V_{DD} .

The CML outputs drive 100 Ω transmission lines and are AC coupled and terminated at their load.

The ENABLE inputs and SIGNAL DETECT outputs are optional. Internal to the device the signal detect circuitry is connected to the enable circuit providing the automatic power management feature. When the No-signal condition is detected, the respective channel is placed in standby mode. The MODE pin is used to select between low and high data rate equalization settings. Depending upon the application it may be tied High, tied Low, or driven. There are several reserved pins on the device, these are NC pins and should be left open.

Power is supplied through six V_{DD} pins to the device. A 0.1µF capacitor is recommended per pin as close to the device as possible. A larger bulk capacitor is also recommended to be placed near by the device. Ground is supplied to the device via the ground pins and also the DAP.

TYPICAL PERFORMANCE EYE DIAGRAMS

FR4 / BACKPLANE Typical Performance Eye Diagrams

The plots show the unequalized and equalized eye patterns for various interconnects as noted. Unequalized is shown in the left column and the corresponding equalized eye pattern in shown in the right column.

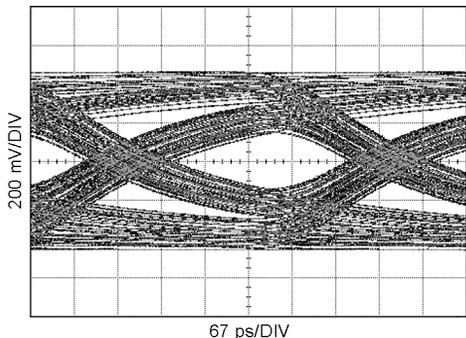


Figure 9. Unequalized Signal (40 in FR4, 2.5 Gbps, PRBS7)

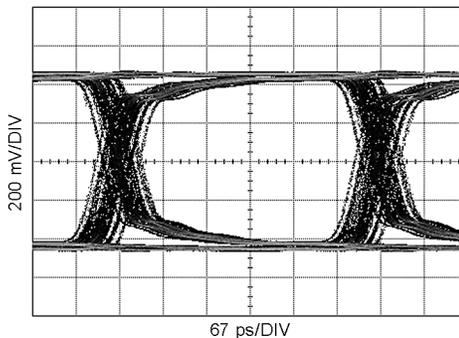


Figure 10. Equalized Signal (40 in FR4, 2.5 Gbps, PRBS7, MODE=1)

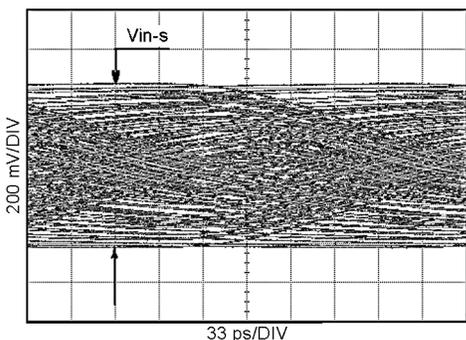


Figure 11. Unequalized Signal (40 in FR4, 5 Gbps, PRBS7)

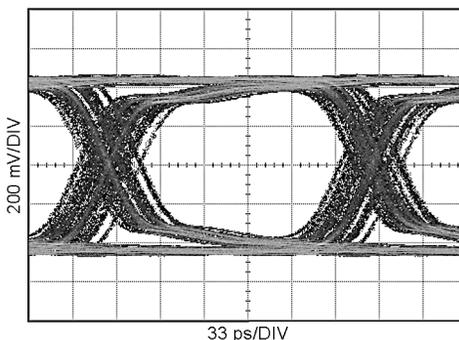


Figure 12. Equalized Signal (40 in FR4, 5 Gbps, PRBS7, MODE=1)

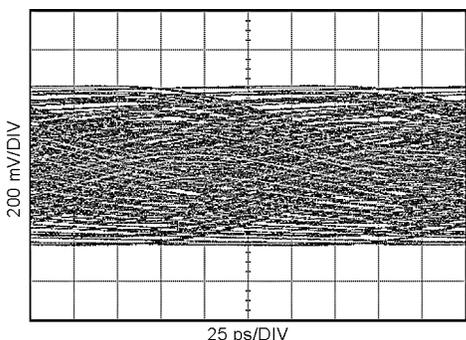


Figure 13. Unequalized Signal (30 in FR4, 8 Gbps, PRBS7)

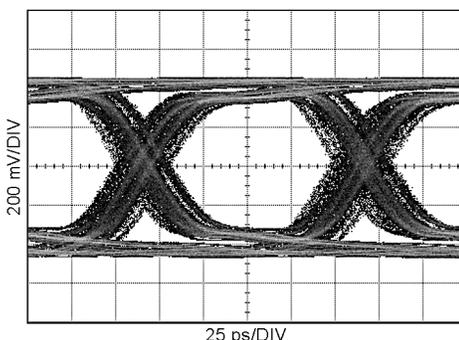


Figure 14. Equalized Signal (30 in FR4, 8 Gbps, PRBS7, MODE=0)

TYPICAL PERFORMANCE EYE DIAGRAMS (continued)

Twin-AX CABLES Typical Performance Eye Diagrams

The plots show the unequalized and equalized eye patterns for various interconnects as noted. Unequalized is shown in the left column and the corresponding equalized eye pattern is shown in the right column.

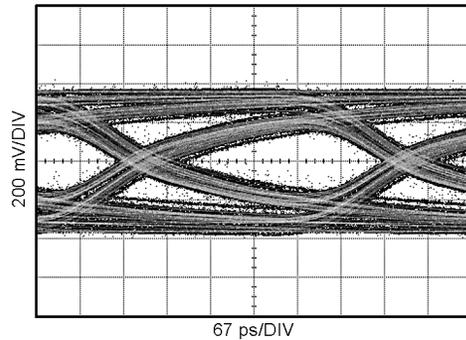


Figure 15. Unequalized Signal (10 m 24 AWG Twin-AX Cable, 2.5 Gbps, PRBS7)

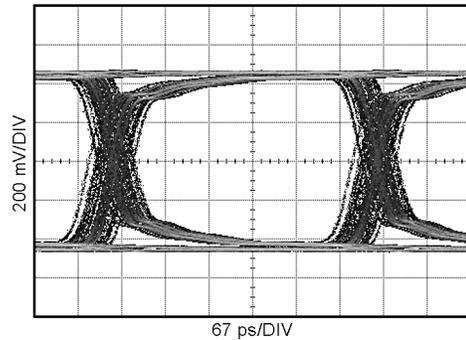


Figure 16. Equalized Signal (10 m 24 AWG Twin-AX Cable, 2.5 Gbps, PRBS7, MODE=1)

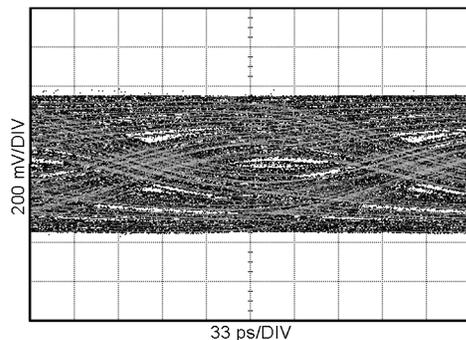


Figure 17. Unequalized Signal (10 m 24 AWG Twin-AX Cable, 5 Gbps, PRBS7)

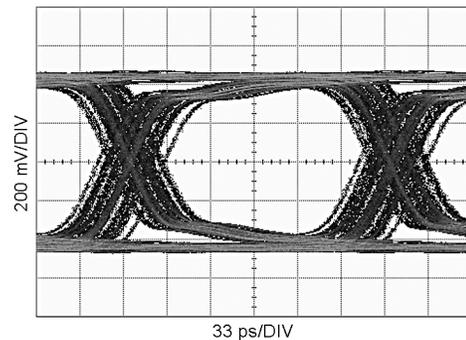


Figure 18. Equalized Signal (10 m 24 AWG Twin-AX Cable, 5 Gbps, PRBS7, MODE=1)

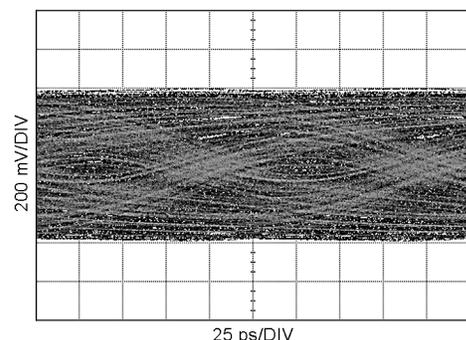


Figure 19. Unequalized Signal (7 m 24 AWG Twin-AX Cable, 8 Gbps, PRBS7)

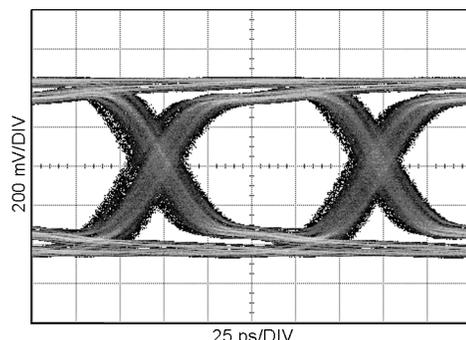
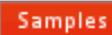
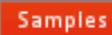


Figure 20. Equalized Signal (7 m 24 AWG Twin-AX Cable, 8 Gbps, PRBS7, MODE=0)

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS50EV401SQ/NOPB	ACTIVE	WQFN	NJU	48	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	DS50EV401	
DS50EV401SQE/NOPB	ACTIVE	WQFN	NJU	48	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	DS50EV401	
DS50EV401SQX/NOPB	ACTIVE	WQFN	NJU	48	2500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	DS50EV401	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

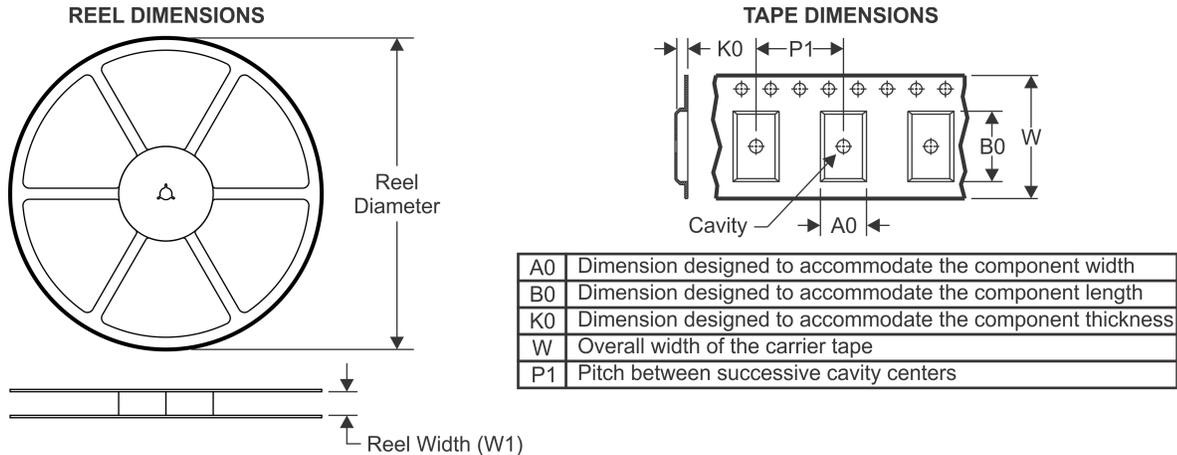
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

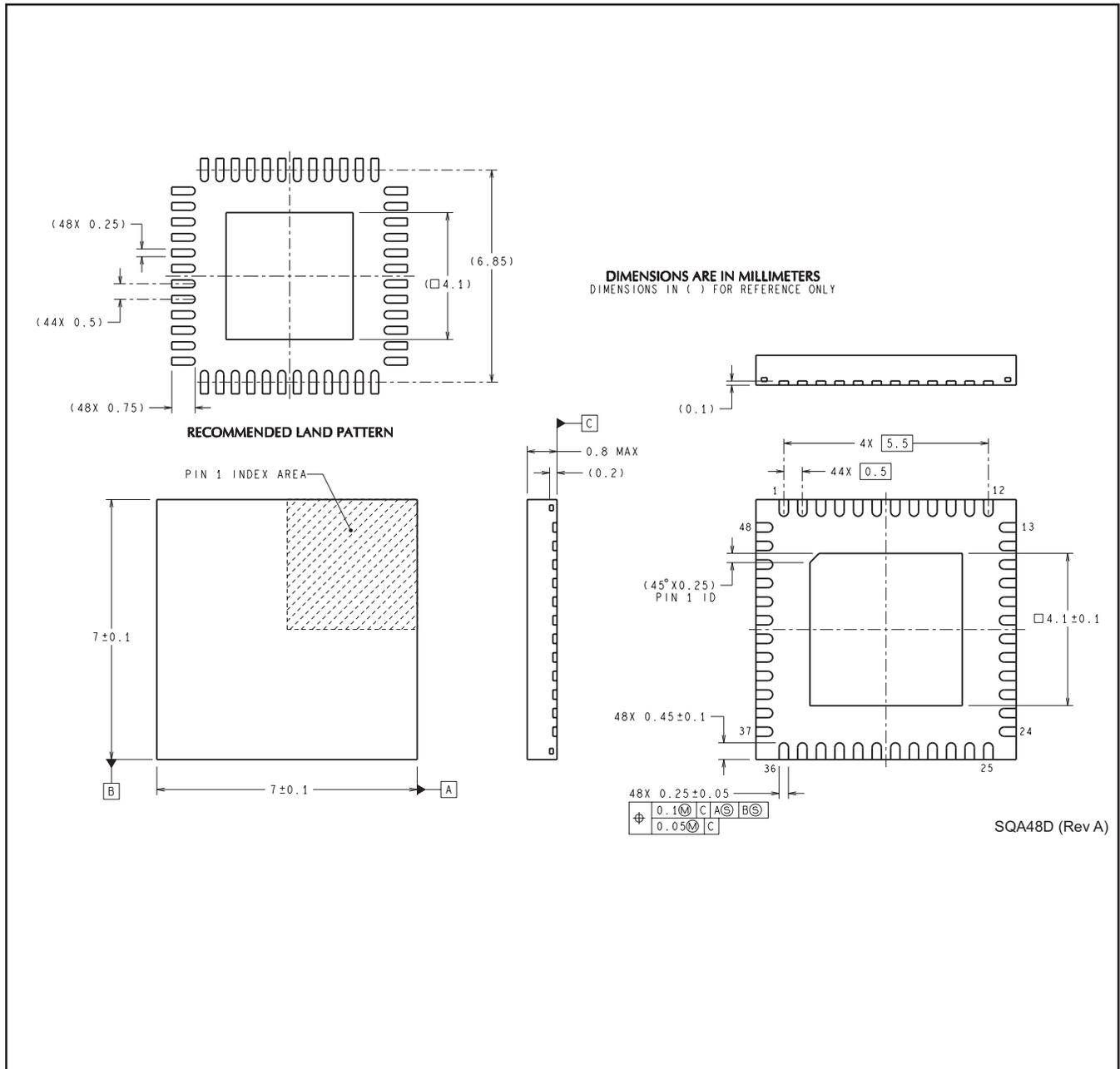
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS50EV401SQ/NOPB	WQFN	NJU	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS50EV401SQE/NOPB	WQFN	NJU	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS50EV401SQX/NOPB	WQFN	NJU	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS50EV401SQ/NOPB	WQFN	NJU	48	1000	367.0	367.0	38.0
DS50EV401SQE/NOPB	WQFN	NJU	48	250	213.0	191.0	55.0
DS50EV401SQX/NOPB	WQFN	NJU	48	2500	367.0	367.0	38.0

NJU0048D



SQA48D (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com