



DS55451/2/3/4, DS75450/1/2/3/4 Series Dual Peripheral Drivers

General Description

The DS75450 series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS75450 is a general purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. The device offers the system designer the flexibility of tailoring the circuit to the application.

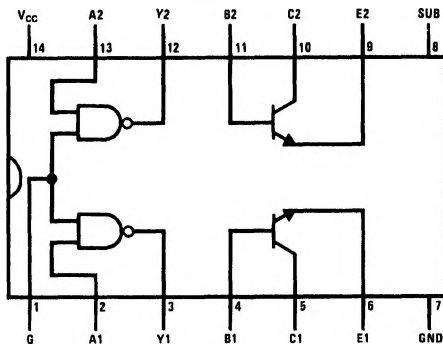
The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic)

with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

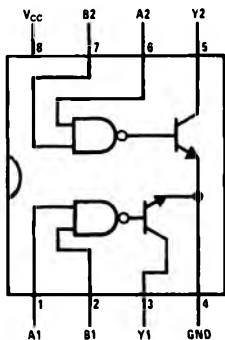
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

Connection Diagrams (Dual-In-Line and Metal Can Packages)



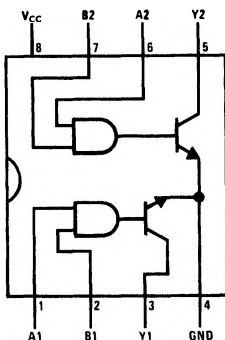
TL/F/5824-1

Top View
Order Number DS75450N
See NS Package Number N14A



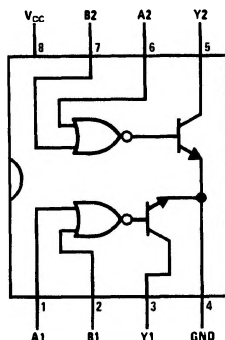
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Top View
Order Number DS55451J-8,
DS75451M or DS75451N



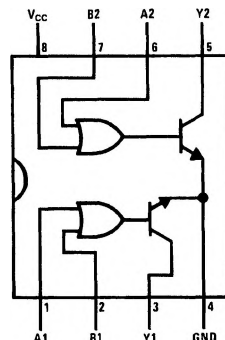
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Top View
Order Number DS55452J-8,
DS75452M or DS75452N



TL/F/5824-4

Top View
Order Number DS55453J-8,
DS75453M or DS75453N



TL/F/5824-5

Top View
Order Number DS55454J-8,
DS75454M or DS75454N

See NS Package Numbers J08A, M08A* or N08E

*See Note 6 and Appendix E regarding S.O. package power dissipation constraints.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
V_{CC} -to-Substrate Voltage DS75450	35V
Collector-to-Substrate Voltage DS75450	35V
Collector-Base Voltage DS75450	35V
Collector-Emitter Voltage (Note 4) DS75450	30V
Emitter-Base Voltage DS75450	5.0V
Output Voltage (Note 5) DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Collector Current (Note 6) DS75450	300 mA
Output Current (Note 6) DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA

DS75450 Maximum Power (Note 6)

Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

DS75451/2/3/4 Maximum Power (Note 6)

Dissipation† at 25°C	
Cavity Package	1090 mW
Molded DIP Package	957 mW
TO-5 Package	760 mW
SO Package	632 mW

Storage Temperature Range -65°C to $+150^{\circ}\text{C}$

Lead Temperature (Soldering, 4 sec.) 260°C

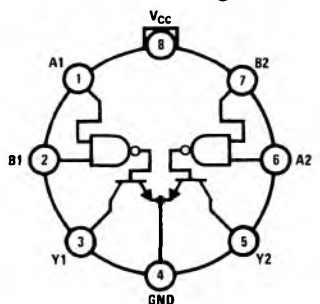
Operating Conditions (Note 7)

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	-55	$+125$	$^{\circ}\text{C}$
DS7545X	0	$+70$	$^{\circ}\text{C}$

*Derate cavity package 8.7 mW/ $^{\circ}\text{C}$ above 25°C; derate molded package 9.7 mW/ $^{\circ}\text{C}$ above 25°C.

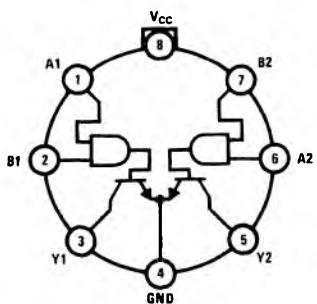
†Derate cavity package 7.3 mW/ $^{\circ}\text{C}$ above 25°C; derate molded package 7.7 mW/ $^{\circ}\text{C}$ above 25°C; derate TO-5 package 5.1 mW/ $^{\circ}\text{C}$ above 25°C; derate SO package 7.56 mW/ $^{\circ}\text{C}$ above 25°C.

Connection Diagrams (Dual-In-Line and Metal Can Packages) (Continued)



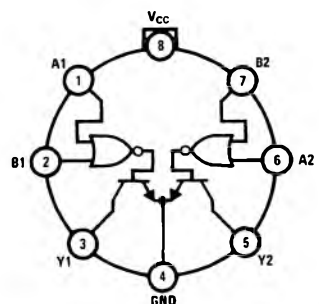
Top View

Order Number DS55451H



Top View

Order Number DS55452H



Top View

Order Number DS55453H

See NS Package Number H08C

Electrical Characteristics DS75450 (Notes 8 and 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TTL GATES						
V_{IH}	High Level Input Voltage	(Figure 1)	2			V
V_{IL}	Low Level Input Voltage	(Figure 2)			0.8	V
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -12 \text{ mA}$, (Figure 3)			-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$, (Figure 2)	2.4	3.3		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$ (Figure 1)		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	$V_{CC} = \text{Max}$, $V_I = 5.5 \text{ V}$, (Figure 4)				
		Input A			1	mA
		Input G			2	mA

Electrical Characteristics DS75450 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TTL GATES (Continued)							
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V, (Figure 4)$	Input A			40	μA
			Input G			80	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V, (Figure 3)$	Input A			-1.6	mA
			Input G			-3.2	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}, (Figure 5), (Note 10)$		-18		-55	mA
I_{CCH}	Supply Current	$V_{CC} = \text{Max}, V_I = 0V, \text{Outputs High}, (Figure 6)$			2	4	mA
I_{CCL}	Supply Current	$V_{CC} = \text{Max}, V_I = 5V, \text{Outputs Low}, (Figure 6)$			6	11	mA
OUTPUT TRANSISTORS							
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100 \mu A, I_E = 0 \mu A$		35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	$I_C = 100 \mu A, R_{BE} = 500\Omega$		30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 100 \mu A, I_C = 0 \mu A$		5			V
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 3V, (Note 11)$	$T_A = +25^{\circ}C$	$I_C = 100 \text{ mA}$	25		
				$I_C = 300 \text{ mA}$	30		
		$T_A = 0^{\circ}C$	$I_C = 100 \text{ mA}$	20			
			$I_C = 300 \text{ mA}$	25			
V_{BE}	Base-Emitter Voltage	$(Note 11)$	$I_B = 10 \text{ mA}, I_C = 100 \text{ mA}$	0.85	1		V
			$I_B = 30 \text{ mA}, I_C = 300 \text{ mA}$	1.05	1.2		V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	$(Note 11)$	$I_B = 10 \text{ mA}, I_C = 100 \text{ mA}$	0.25	0.4		V
			$I_B = 30 \text{ mA}, I_C = 300 \text{ mA}$	0.5	0.7		V

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V _{IH}	High-Level Input Voltage	(Figure 7)				2			V
V _{IL}	Low-Level Input Voltage							0.8	V
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −12 mA						−1.5	V
V _{OL}	Low-Level Output Voltage	V _{CC} = Min, (Figure 7)	V _{IL} = 0.8V	I _{OL} = 100 mA	DS55451, DS55453	0.25	0.5	V	
					DS75451, DS75453	0.25	0.4	V	
				I _{OL} = 300 mA	DS55451, DS55453	0.5	0.8	V	
					DS75451, DS75453	0.5	0.7	V	
			V _{IH} = 2V	I _{OL} = 100 mA	DS55452, DS55454	0.25	0.5	V	
					DS75452, DS75454	0.25	0.4	V	
				I _{OL} = 300 mA	DS55452, DS55454	0.5	0.8	V	
					DS75452, DS75454	0.5	0.7	V	
I _{OH}	High-Level Output Current	V _{CC} = Min, (Figure 7)	V _{OH} = 30V	V _{IH} = 2V	DS55451, DS55453		300	μA	
					DS75451, DS75453		100	μA	
				V _{IL} = 0.8V	DS55452, DS55454		300	μA	
					DS75452, DS75454		100	μA	
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max, V _I = 5.5V, (Figure 9)						1	mA

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	High-Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4\text{V}$, (Figure 9)			40	μA
I_{IL}	Low-Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}$, (Figure 8)		-1	-1.6	mA
I_{CCH}	Supply Current, Outputs High	$V_{CC} = \text{Max}$, (Figure 10)				
		$V_I = 5\text{V}$ DS55451/DS75451		7	11	mA
		$V_I = 0\text{V}$ DS55452/DS75452		11	14	mA
		$V_I = 5\text{V}$ DS55453/DS75453		8	11	mA
I_{CCL}	Supply Current, Outputs Low	$V_{CC} = \text{Max}$, (Figure 10)				
		$V_I = 0\text{V}$ DS55451/DS75451		52	65	mA
		$V_I = 5\text{V}$ DS55452/DS75452		56	71	mA
		$V_I = 0\text{V}$ DS55453/DS75453		54	68	mA
		$V_I = 5\text{V}$ DS55454/DS75454		61	79	mA

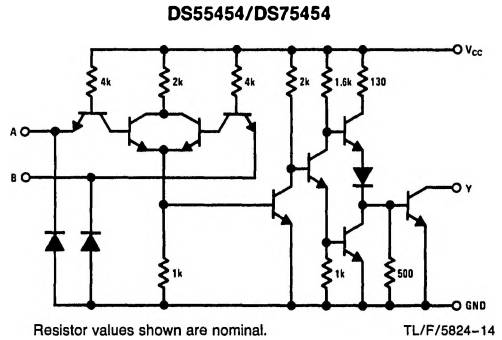
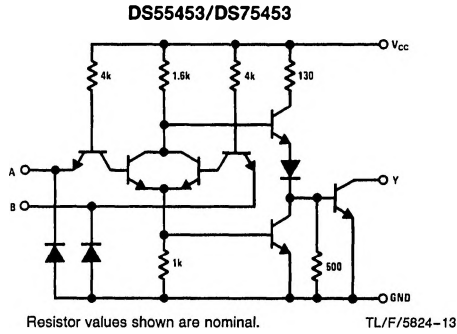
Switching Characteristics DS75450 ($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 15\text{pF}$ $R_L = 400\Omega$, TTL Gates, (Figure 12) $R_L = 50\Omega$, $I_C \approx 200\text{mA}$, Gates and Transistors Combined, (Figure 14)		12	22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L = 15\text{pF}$ $R_L = 400\Omega$, TTL Gates, (Figure 12) $R_L = 50\Omega$, $I_C \approx 200\text{mA}$, Gates and Transistors Combined, (Figure 14)		8	15	ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L = 15\text{pF}$, $R_L = 50\Omega$, $I_C \approx 200\text{mA}$, Gates and Transistors Combined, (Figure 14)		7	12	ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L = 15\text{pF}$, $R_L = 50\Omega$, $I_C \approx 200\text{mA}$, Gates and Transistors Combined, (Figure 14)		9	15	ns
V_{OH}	High-Level Output Voltage after Switching	$V_S = 20\text{V}$, $I_C \approx 300\text{mA}$, $R_{BE} = 500\Omega$, (Figure 15)	$V_S - 6.5$			mV
t_D	Delay Time	$I_C = 200\text{mA}$, $I_{B(1)} = 20\text{mA}$, $I_B = -40\text{mA}$, $V_{BE(OFF)} = -1\text{V}$, $C_L = 15\text{pF}$, $R_L = 50\Omega$, (Figure 13), (Note 12)		8	15	ns
t_R	Rise Time			12	20	ns
t_S	Storage Time			7	15	ns
t_F	Full Time			6	15	ns

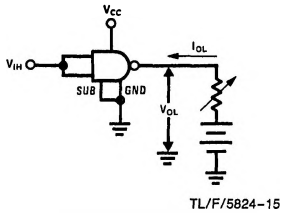
Switching Characteristics (Continued)DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 ($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L = 15\text{pF}$, $R_L = 50\Omega$, $I_O \approx 200\text{mA}$, (Figure 14)				
		DS55451/DS75451		18	25	ns
		DS55452/DS75452		26	35	ns
		DS55453/DS75453		18	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L = 15\text{pF}$, $R_L = 50\Omega$, $I_O \approx 200\text{mA}$, (Figure 14)				
		DS55451/DS75451		18	25	ns
		DS55452/DS75452		24	35	ns
		DS55453/DS75453		16	25	ns
		DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L = 15\text{pF}$, $R_L = 50\Omega$, $I_O \approx 200\text{mA}$, (Figure 14)		5	8	ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L = 15\text{pF}$, $R_L = 50\Omega$, $I_O \approx 200\text{mA}$, (Figure 14)		7	12	ns
V_{OH}	High-Level Output Voltage after Switching	$V_S = 20\text{V}$, $I_O \approx 300\text{mA}$, (Figure 15)	$V_S - 6.5$			mV

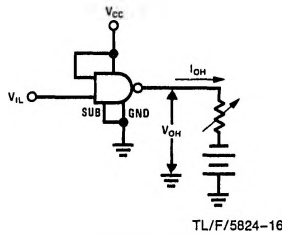
Schematic Diagrams (Continued)



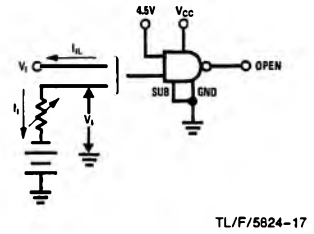
DC Test Circuits



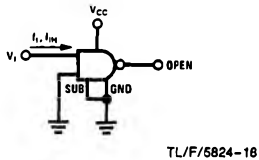
Both inputs are tested simultaneously.
FIGURE 1. V_{IH} , V_{OL}



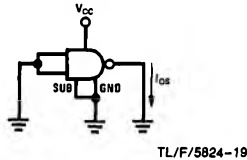
Each input is tested separately.
FIGURE 2. V_{IL} , V_{OH}



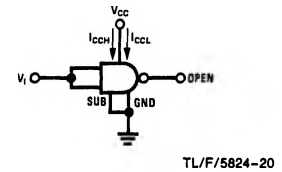
Each input is tested separately.
FIGURE 3. V_I , I_{IL}



Each input is tested separately.
FIGURE 4. I_I , I_{IH}



Each input is tested separately.
FIGURE 5. I_{OS}



Both gates are tested simultaneously.
FIGURE 6. I_{CCH} , I_{CCL}

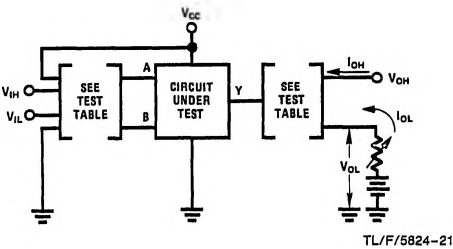
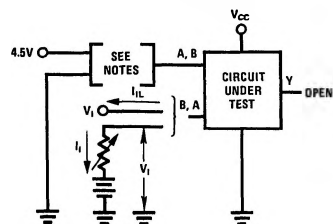


FIGURE 7. V_{IH} , V_{IL} , I_{OH} , V_{OL}

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55451	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55453	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OH}
DS55454	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

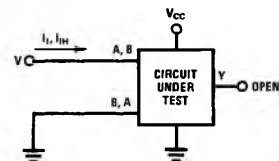
DC Test Circuits (Continued)



Note A: Each input is tested separately.
Note B: When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded.
 For all other circuits it is at 4.5V.

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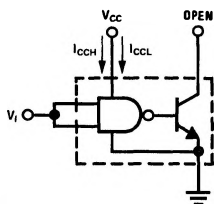
FIGURE 8. V_I , V_{IL}



Each input is tested separately.

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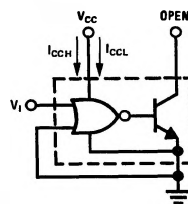
FIGURE 9. I_I , I_{IH}



Both gates are tested simultaneously.

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FIGURE 10. I_{OCH} , I_{OCL} for AND, NAND Circuits

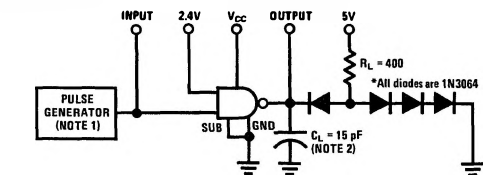


Both gates are tested simultaneously.

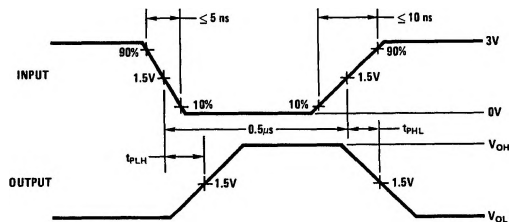
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FIGURE 11. I_{OCH} , I_{OCL} for OR, NOR Circuits

AC Test Circuits and Switching Time Waveforms



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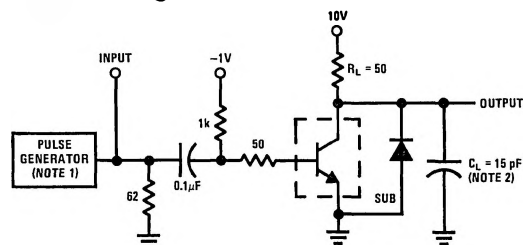
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Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

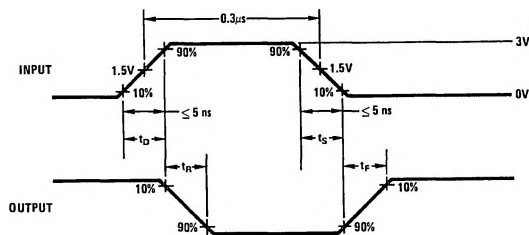
Note 2: C_L includes probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS75450 Only)

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824-28

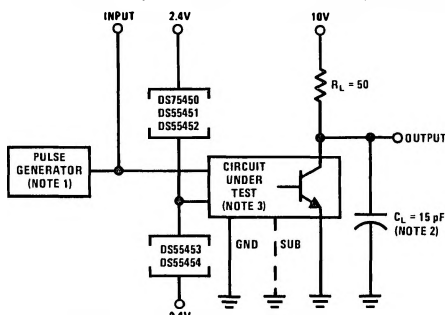


TL/F/5824-29

Note 1: The pulse generator has the following characteristics: duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor (DS75450 Only)

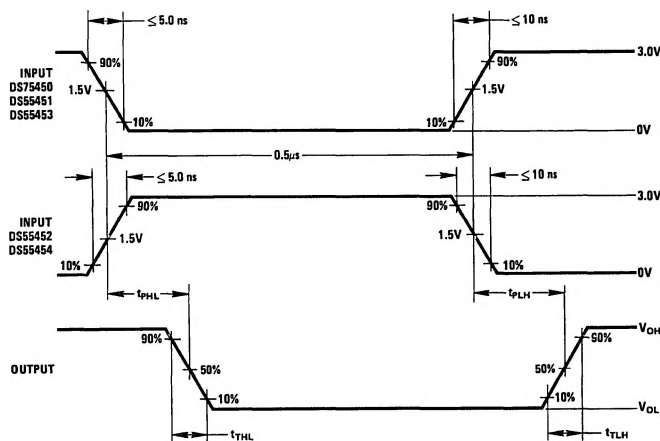


Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.

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Note 2: C_L includes probe and jig capacitance.

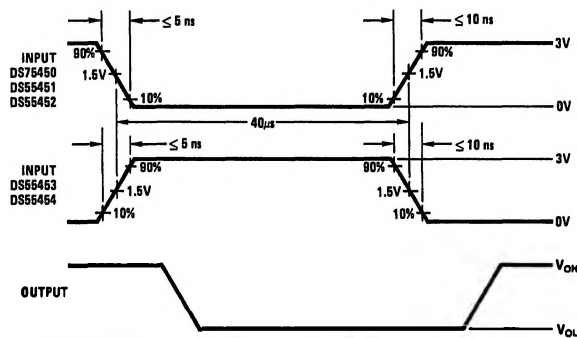
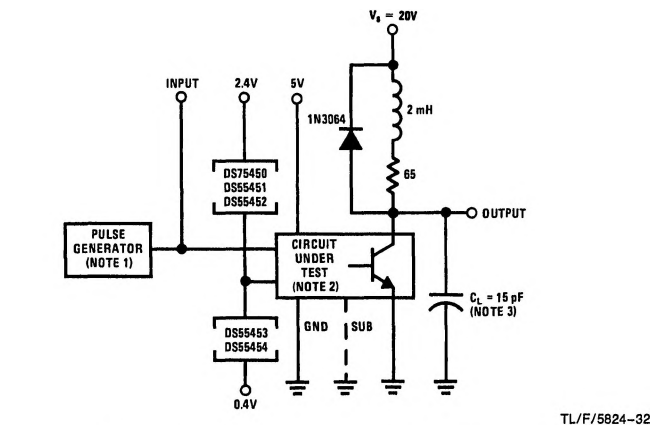
Note 3: When testing DS75450, connect output V to transistor base and ground the substrate terminal.



TL/F/5824-31

FIGURE 14. Switching Times of Complete Drivers

AC Test Circuits and Switching Time Waveforms (Continued)



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} \approx 50\Omega$.

Note 2: When testing DS75450, connect output V to transistor base with a 600 Ω resistor from there to ground and ground the substrate terminal.

Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-UP Test of Complete Drivers

Typical Performance Characteristics

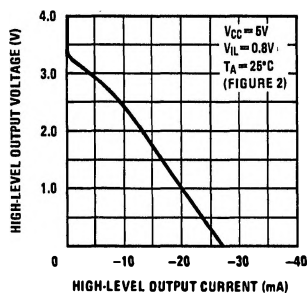


FIGURE 16. DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current

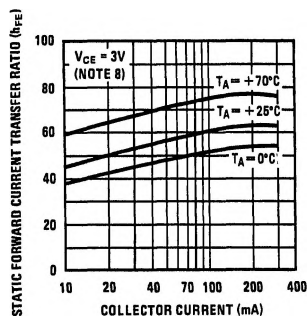


FIGURE 17. DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

Typical Performance Characteristics (Continued)

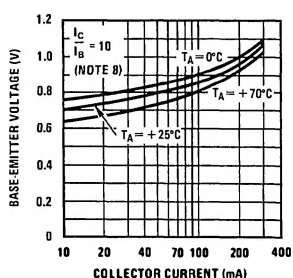


FIGURE 18. DS75450 Transistor Base-Emitter Voltage vs Collector Current

TL/F/5824-36

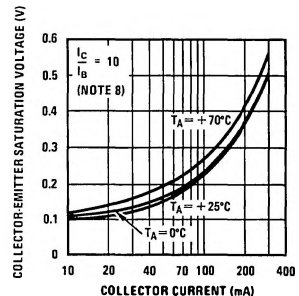
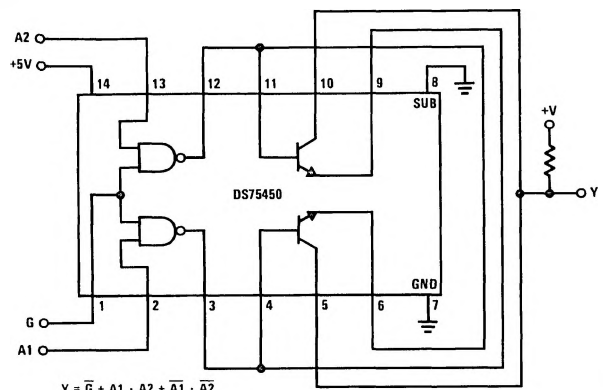


FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

TL/F/5824-37

Typical Applications



$$Y = \overline{G} + A1 \cdot A2 + \overline{A1} \cdot \overline{A2}$$

FIGURE 20. Gated Comparator

TL/F/5824-38

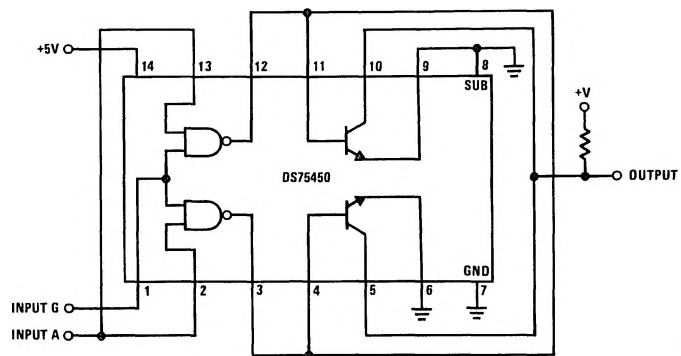
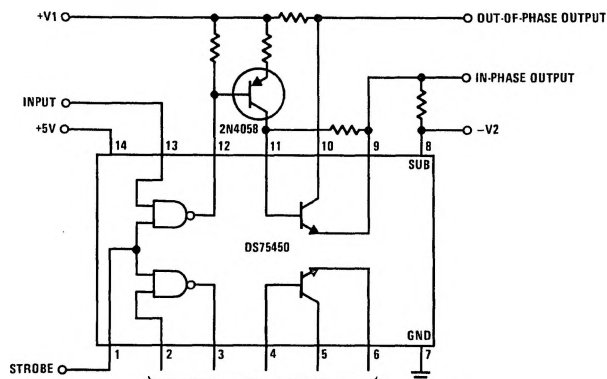


FIGURE 21. 500 mA Sink

TL/F/5824-39

Typical Applications (Continued)



This side can perform the same or another function.

FIGURE 22. Floating Switch

TL/F/5824-40

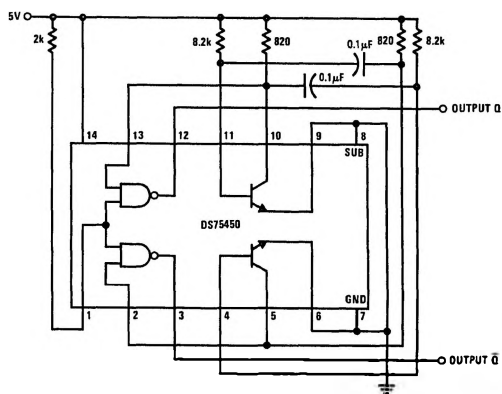
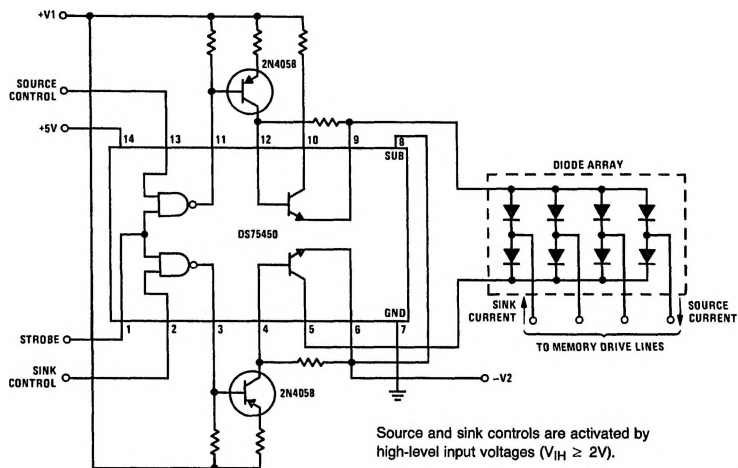


FIGURE 23. Square-Wave Generator

TL/F/5824-41



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

FIGURE 24. Core Memory Driver

TL/F/5824-42

Typical Applications (Continued)

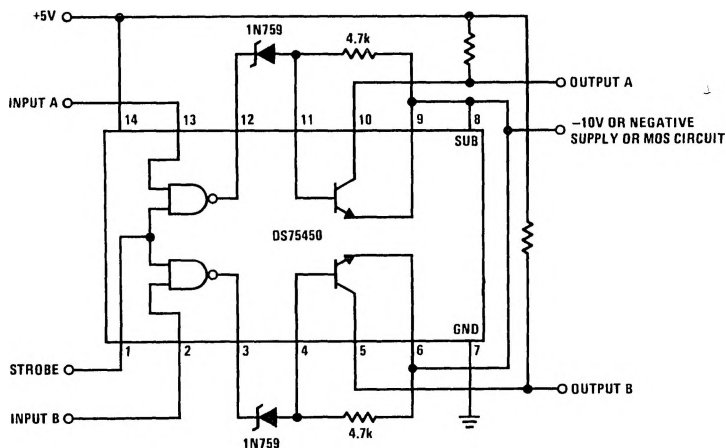


FIGURE 25. Dual TTL-to-MOS Driver

TL/F/5824-43

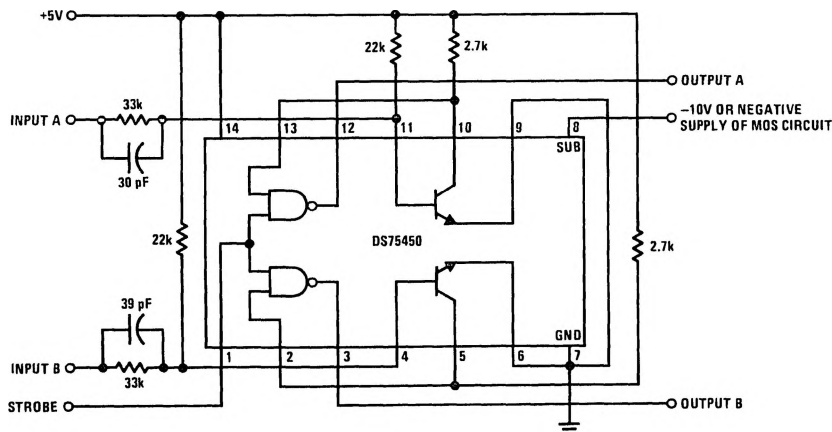
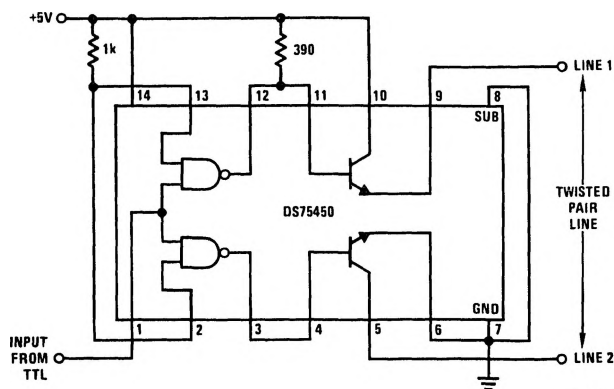


FIGURE 26. Dual MOS-to-TTL Driver

TL/F/5824-44



Termination is made at the receiving end as follows:
Line 1 is terminated to ground through Z_0/Z ;
Line 2 is terminated to +5V through Z_0/Z ;
where Z_0 is the line impedance.

FIGURE 27. Balanced Line Driver

TL/F/5824-45

Typical Applications (Continued)

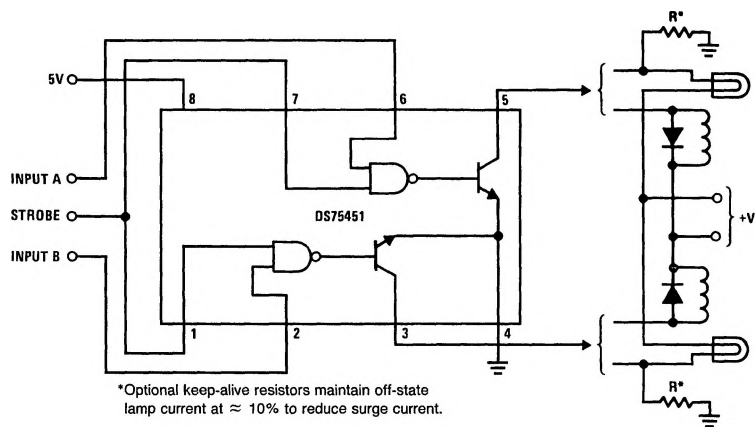


FIGURE 28. Dual Lamp or Relay Driver

TL/F/5824-46

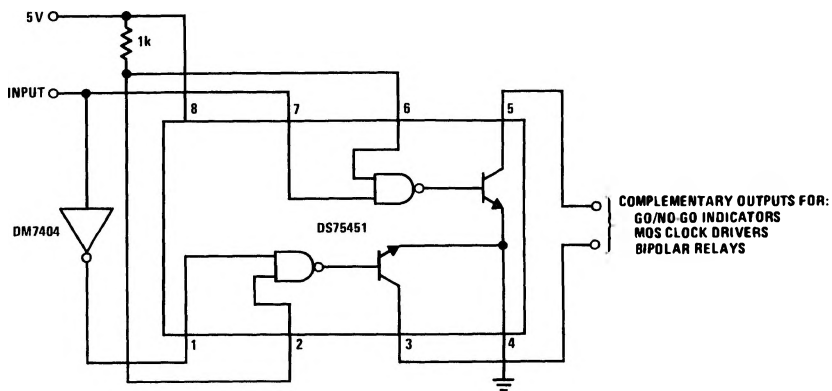


FIGURE 29. Complementary Driver

TL/F/5824-47

Typical Applications (Continued)

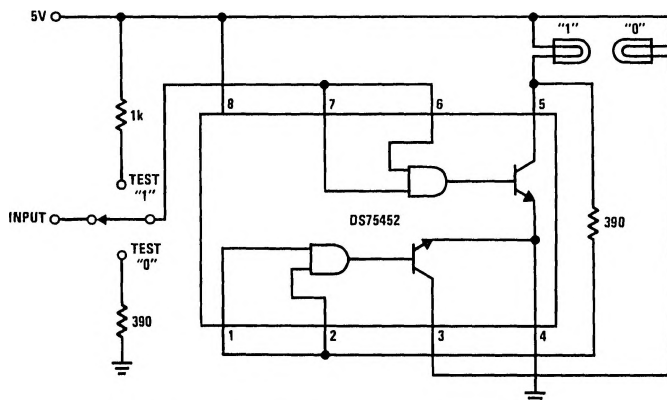
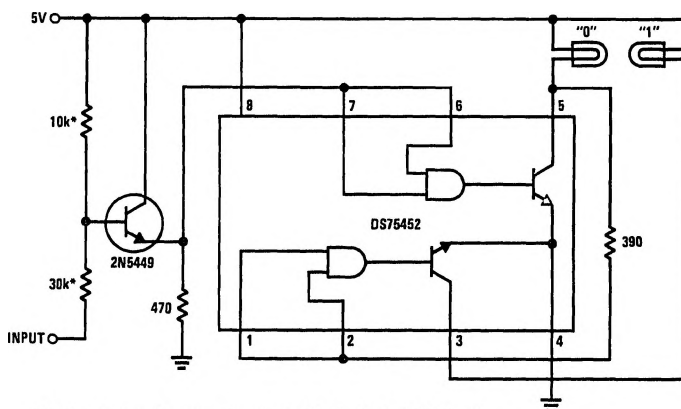


FIGURE 30. TTL or DTL Positive Logic-Level Detector

TL/F/5824-48



*The two input resistors must be adjusted for the level of MOS input.

FIGURE 31. MOS Negative Logic-Level Detector

TL/F/5824-49

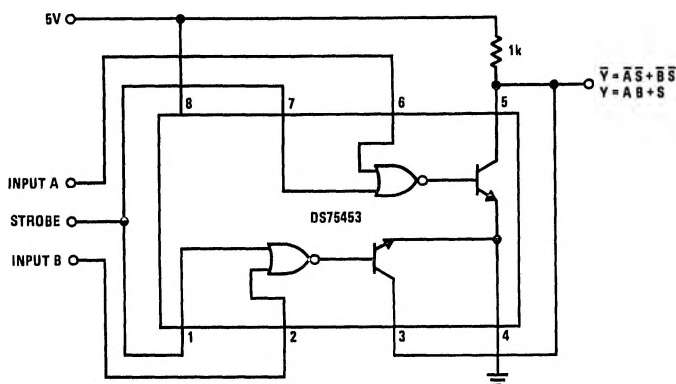
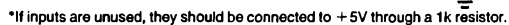


FIGURE 32. Logic Signal Comparator

TL/F/5824-50



TL/F/5824-51

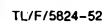


FIGURE 33. In-Phase Detector



TL/F/5824-53

Typical Applications (Continued)

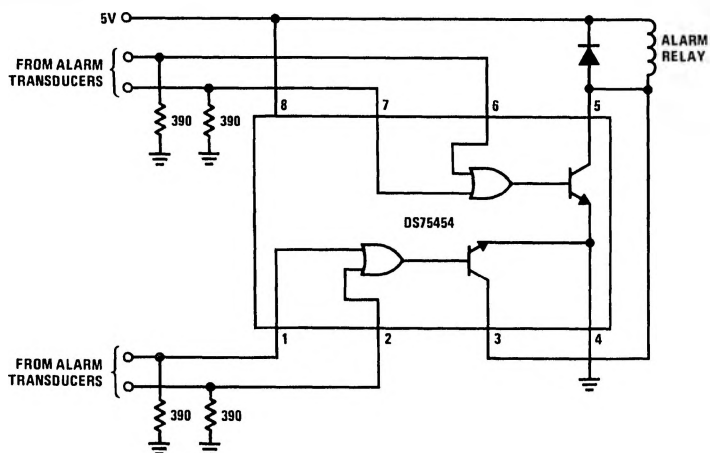


FIGURE 35. Alarm Detector

TL/F/5824-54