



DS7830/DS8830 Dual Differential Line Driver

General Description

The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

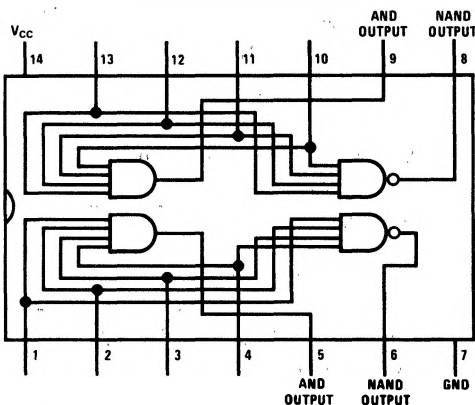
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω . The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

- Single 5V power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Connection Diagram

Dual-In-Line and Flat Package



TL/F/5799-2

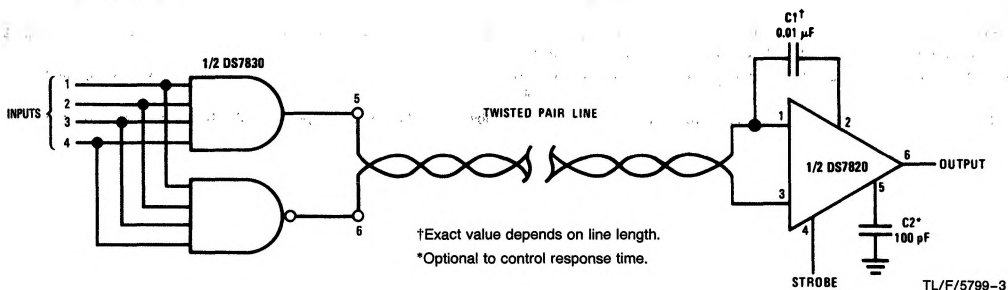
Top View

Order Number DS8830N
See NS Package Number N14A

For Complete Military 883 Specifications, See RETS Data Sheet.
Order Number DS7830J/883 or DS7830W/883
See NS Package Number J14A

Typical Application

Digital Data Transmission



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Output Short Circuit Duration (125°C)	1 second
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7830	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	-55	+125	°C
DS8830	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$				
		$I_{OUT} = -0.8\text{ mA}$	2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 2.0V$				
		$I_{OUT} = 40\text{ mA}$	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 2.0V$				
		$I_{OUT} = 32\text{ mA}$		0.2	0.4	V
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$			120	μA
		$V_{IN} = 5.5V$			2	mA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$			-4.8	mA
I_{SC}	Output Short Circuit Current	$V_{CC} = 5.0V$, $T_A = 125^\circ\text{C}$, (Note 4)	-40	-100	-120	mA
I_{CC}	Supply Current	$V_{IN} = 5.0V$, (Each Driver)		11	18	mA
V_I	Input Clamp	$V_{CC} = \text{Min}$, $I_{IN} = -12\text{ mA}$		-1.0	-1.5	V

Switching Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay AND Gate	$R_L = 400\Omega$, $C_L = 15\text{ pF}$ (Figure 1)		8	12	ns
t_{pd0}				11	18	ns
t_{pd1}	Propagation Delay NAND Gate	$R_L = 400\Omega$, $C_L = 15\text{ pF}$ (Figure 1)		8	12	ns
t_{pd0}				5	8	ns
t_1	Differential Delay	Load, 100 Ω and 5000 pF, (Figure 2)		12	16	ns
t_2	Differential Delay	Load, 100 Ω and 5000 pF, (Figure 2)		12	16	ns

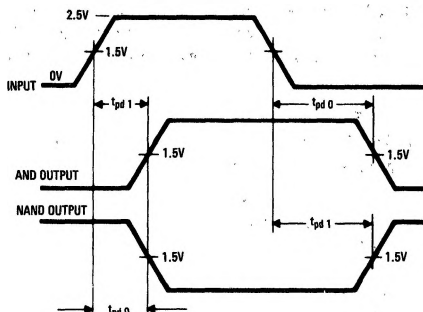
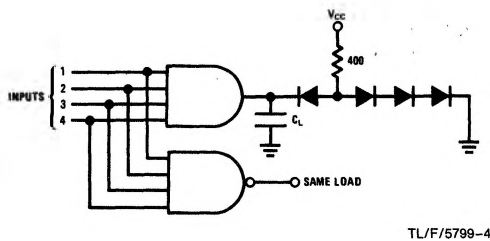
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the -55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



$f = 1 \text{ MHz}$
 $t_r = t_f \leq 10 \text{ ns}$ (10% to 90%)
 Duty cycle = 50%

FIGURE 1

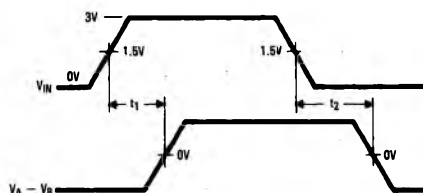
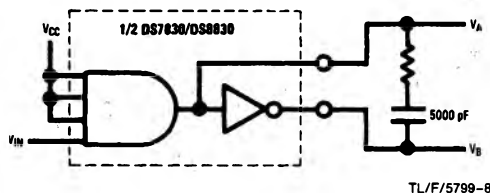
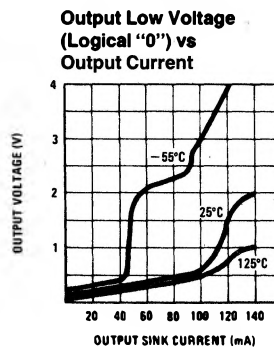
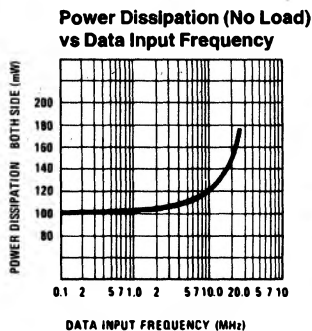
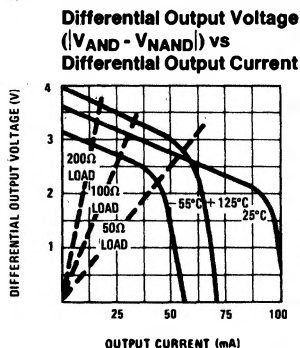
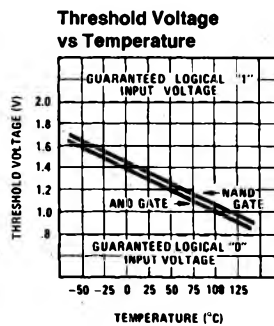
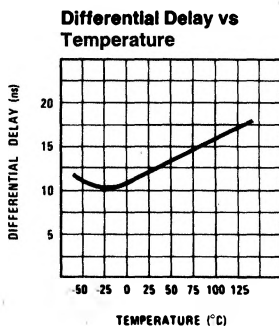
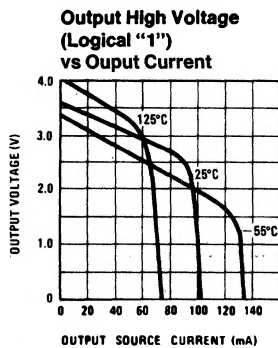


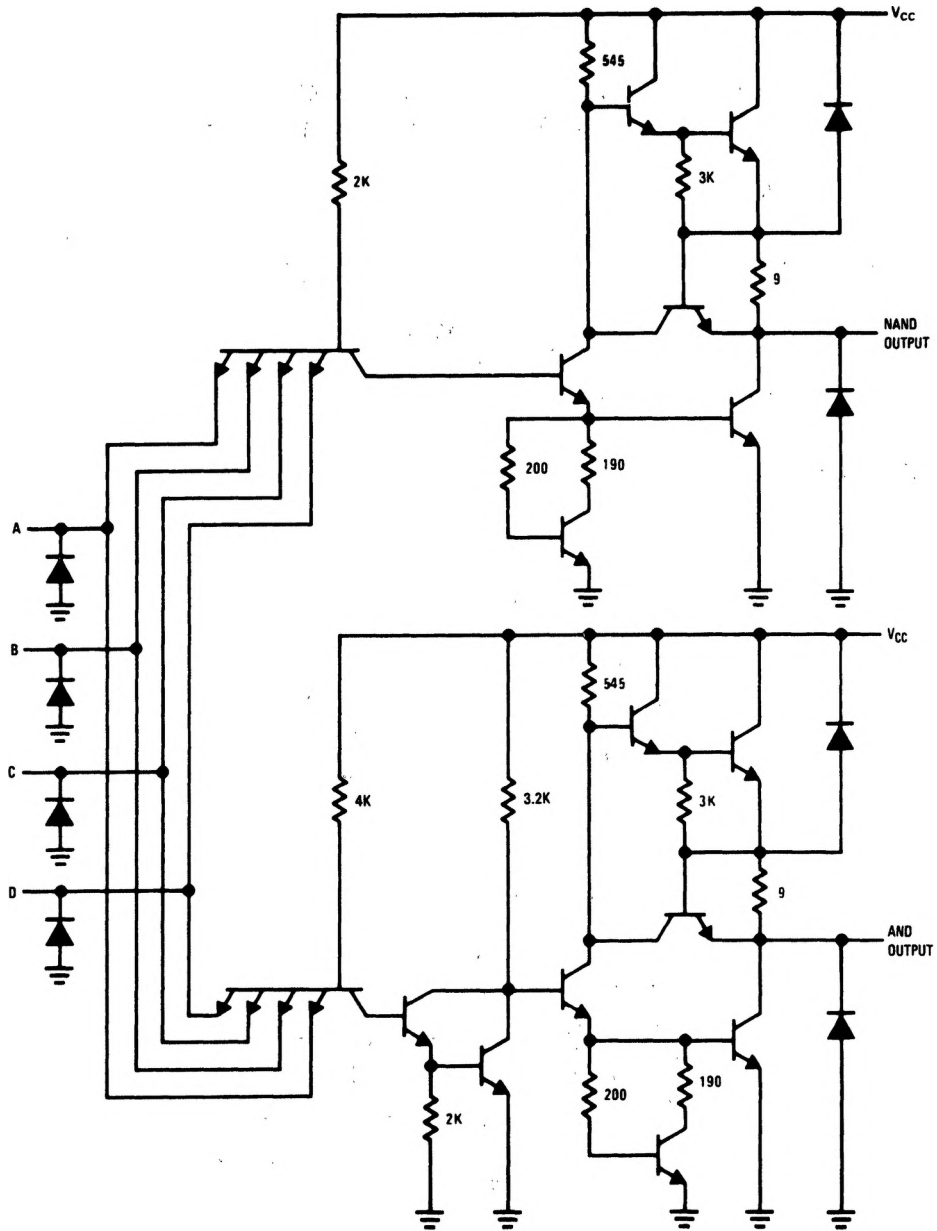
FIGURE 2

Typical Performance Characteristics



TL/F/5799-7

Schematic Diagram



*2 Per Package

TL/F/5799-1