DS80PCI102 2.5 Gbps / 5.0 Gbps / 8.0 Gbps 1 Lane PCI Express Repeater with Equalization and De-Emphasis

Check for Samples: DS80PCI102

FEATURES

- **Comprehensive family, proven system interoperability**
  - **DS80PCI102: x1 PCIe Gen-1/2/3**
  - **DS80PCI402: x4 PCIe Gen-1/2/3**
  - **DS80PCI800: x8/x16 PCIe Gen-1/2/3**
- **Automatic rate detect and adaption to Gen-1/2/3 speeds**
- **Seamless support for Gen-3 transmit FIR handshake**
- **Rate adaptive receive EQ (up to 36 dB), transmit de-emphasis (up to 12 dB) only Gen-1/2**
- **Adjustable Transmit VOD: 0.7 to 1.3Vp-p (pin mode)**
- **0.2 UI of residual deterministic jitter at 8Gbps after 40" of FR4 or 10m 30awg PCIe cable**
- **Low power dissipation with ability to turnoff unused channels: 65mW/channel**
- **Automatic receiver detect (hot-plug)**
- **Multiple configuration modes: Pins/SMBus/Direct EEPROM load**
- **Single supply voltage: 2.5V or 3.3V (selectable)**
- **Flow-thru pinout in 4mmx4mm 24-pin leadless WQFN package**
- **>5 kV HBM ESD rating**
- **-40 to 85°C operating temperature range**

DESCRIPTION

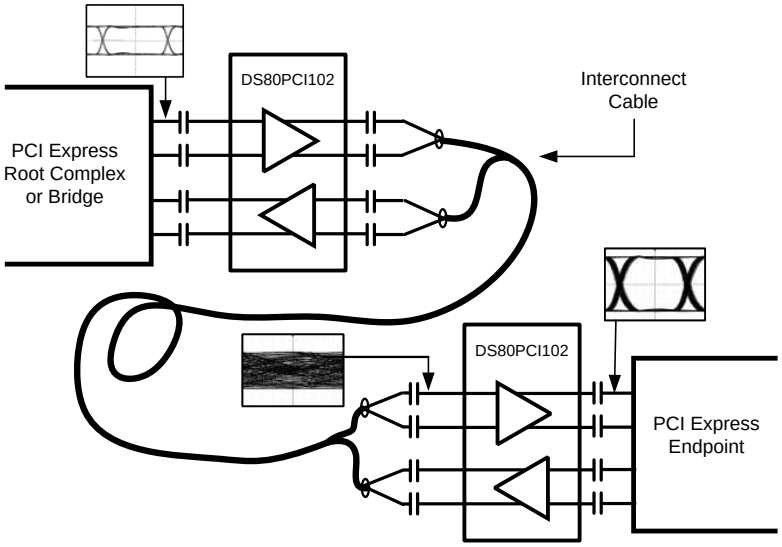
The DS80PCI102 is a low power, 1 lane repeater with 4-stage input equalization, and output de-emphasis driver to enhance the reach of PCI express serial links in board-to-board or cable interconnects. Ideal for x1 PCI express configuration, the DS80PCI102 automatically detects and adapts to Gen-1, Gen-2 and Gen-3 data rates for easy system upgrade.

Each channel supports seamless detection and management of the new Gen-3 transmit equalizer coefficients (FIR tap) handshake protocol and PCIe control signals such as transmit idle, beacon etc. without external system intervention. An automatic receive detection circuitry controls the input termination impedance based upon endpoint insertion (hot-plug events). These features ensure PCIe interoperability at both the electrical and system level, while reducing design complexity.

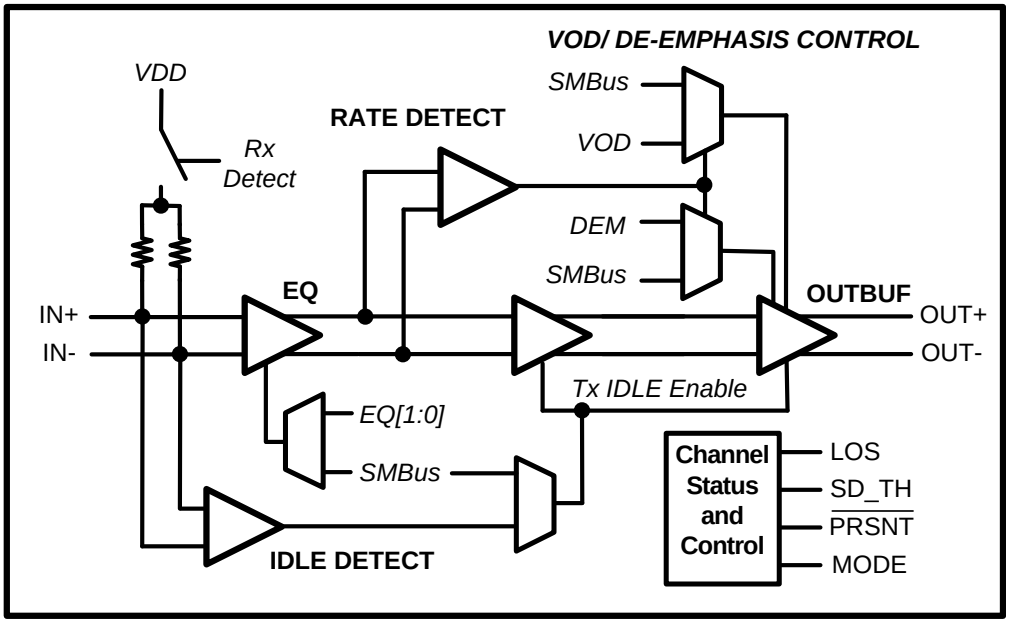
The DS80PCI102 offers programmable transmit de-emphasis (up to 12 dB), transmit VoD (up to 1300 mVp-p) and receive equalization (up to 36 dB) to enable longer distance transmission in lossy copper cables (10m+), or backplanes (40"+) with multiple connectors. The receiver is capable of opening an input eye that is completely closed due to inter-symbol interference (ISI) introduced by the interconnect medium.

The programmable settings can be applied easily via pins, software (SMBus/I2C) or loaded via an external EEPROM. In EEPROM mode the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver. The DS80PCI102 is part of PowerWise family of energy efficient devices.

Typical Application



Block Diagram - Detail View Of Channel (1 of 2)



Pin Diagram

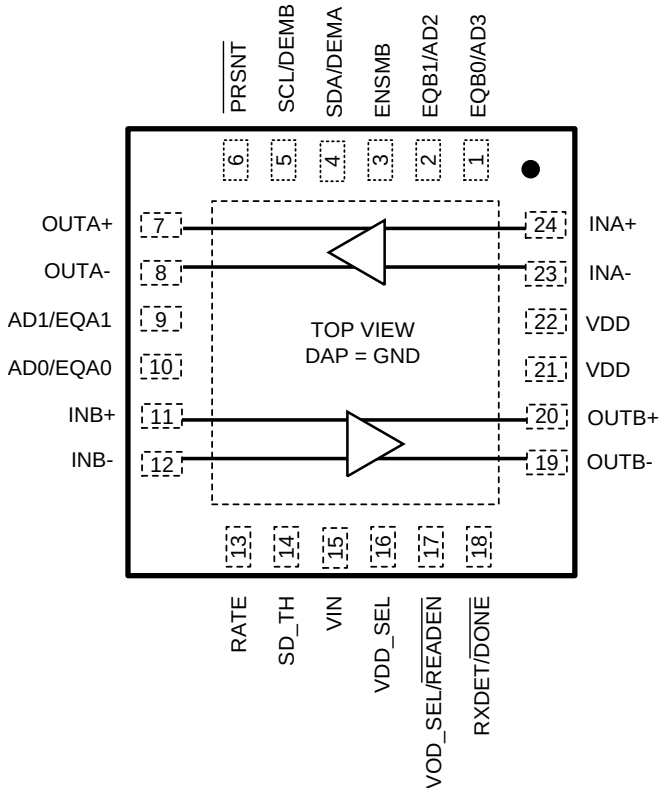


Figure 1. DS80PCI102 Pin Diagram 24 lead

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Pin Description
Differential High Speed I/O's			
INA+, INA- , INB+, INB-	24, 23 11, 12	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. A gated on-chip 50Ω termination resistor connects INn+ to VDD and INn- to VDD when enabled.
OUTA+, OUTA-, OUTB+, OUTB-	7, 8 20, 19	O, CML	Inverting and non-inverting 50Ω driver outputs with de-emphasis. Compatible with AC coupled CML inputs.
Control Pins			
ENSMB	3	I, LVCMOS Float	System Management Bus (SMBus) enable pin High = Register Access, SMBus Slave mode Float = SMBus Master mode, read from External EEPROM Low = External Pin Control Mode
ENSMB = 1 (SMBUS MODE)			
SCL	5	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode SMBUS clock input pin is enabled (slave mode). Clock output when loading EEPROM configuration (master mode).
SDA	4	I, LVCMOS, O, OPEN Drain	ENSMB Master or Slave mode The SMBus bi-directional SDA pin is enabled. Data input or open drain (pulldown only) output.
AD0-AD3	10, 9, 2, 1	I, LVCMOS (Internal Pull-down)	ENSMB Master or Slave mode SMBus Slave Address Inputs. In SMBus mode, these pins are the user set SMBus slave address inputs. There are 16 addresses supported by these pins. Pins must be tied LOW or HIGH when used to define the device SMBus address.

Pin Descriptions (continued)

Pin Name	Pin Number	I/O, Type	Pin Description
$\overline{\text{READEN}}$	17	I, LVCMOS	When using an External EEPROM, a transition from high to low starts the load from the external EEPROM. In SMBus slave mode, set $\overline{\text{READEN}}$ = 0.
$\overline{\text{DONE}}$	18	O, LVCMOS	EEPROM Download Status HIGH indicates Error / Still Loading LOW indicates download complete. No Error.
ENSMB = 0 (PIN MODE)			
EQA0, EQA1 EQB0, EQB1	10, 9 1, 2	I, 4-LEVEL, LVCMOS	EQA[1:0] control the level of equalization of the A channel and EQB[1:0] control the level of B channel. The EQA/B pins are active only when ENSMB is de-asserted (LOW). When ENSMB goes high the SMBus registers provide independent control of each lane, and the EQA/B[1:0] pins are converted to SMBUS AD[3:0] inputs. See Table 1
DEMA, DEMB	4, 5	I, 4-LEVEL, LVCMOS	DEMA/B controls the level of de-emphasis. The DEMA/B pins are only active when ENSMB is de-asserted (LOW). DEMA controls the A channel and DEMB controls the B channel. When ENSMB goes high the SMBus registers provide independent control of each channel and the DEM pins are converted to SMBUS SDA and SCL pins. See Table 2
$\overline{\text{PRSNT}}$	6	I, LVCMOS	HIGH = Low Power LOW = Normal Operation Note: See Electrical Table for detailed specifications.
VOD_SEL	17	I, 4-LEVEL, LVCMOS	VOD Select pin. See Table 2
VDD_SEL	16	I, FLOAT	Enables the 3.3V to 2.5V internal regulator Float = 2.5 V Mode Operation Tie GND = 3.3 V Mode Operation
RXDET	18	I, 4-LEVEL, LVCMOS	The RXDET pin controls the receiver detect function. Depending on the input level, a 50Ω or >50kΩ termination to the power rail is enabled. See Table 3
RATE	13	I, 4-LEVEL, LVCMOS	RATE control pin selects GEN 1,2 and GEN 3 operating modes. 0 = GEN 1,2 Float = AUTO Rate Select (with DEM control) R = Tie 20kΩ to GND = GEN 3 (no DEM control) 1 = GEN 3 (with DEM control)
SD_TH	14	I, 4-LEVEL, LVCMOS	Controls the internal Signal Detect Threshold. See Table 4
Power			
VDD	21, 22	Power	Power supply pins 2.5V MODE, connect to 2.5V supply 3.3V MODE, do not connect to any supply voltage. Should be used to attach external decoupling to device, 100 - 200 nF recommended.
VIN	15	Power	VIN = 3.3V +/-10% (input to internal LDO regulator) NOTE: Must float VIN for 2.5V MODE operation.
GND	DAP	Power	Ground pad (DAP - die attach pad).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (VDD - 2.5V)	-0.5V to +2.75V
Supply Voltage (VIN - 3.3V)	-0.5V to +4.0V
LVCMOS Input/Output Voltage	-0.5V to +4.0V
CML Input Voltage	-0.5V to (VDD+0.5)
CML Input Current	-30 to +30 mA
Junction Temperature	125°C
Storage Temperature	-40°C to +125°C
Lead Temperature Range Soldering (4 sec.)	+260°C
ESD Rating	
HBM, STD - JESD22-A114F	> 5 kV
MM, STD - JESD22-A115-A	100 V
CDM, STD - JESD22-C101-D	1250 V
Package Thermal Resistance	
θJC	3.2°C/W
θJA, No Airflow, 4 layer JEDEC	33.0°C/W
For soldering specifications see Application Note SNOA549C: http://www.ti.com/lit/an/snoa549c/snoa549c.pdf	

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units
Supply Voltage (2.5V mode)	2.375	2.5	2.625	V
Supply Voltgae (3.3V mode)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C
SMBus (SDA, SCL)			3.6	V

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power						
IDD	Supply Current	VIN = 3.3V supply, EQ = Enabled, RXDET = 1, VOD = 1.0 Vp-p, $\overline{\text{PRSNT}}$ = LOW		50	63	mA
		VIN = 3.3V supply, $\overline{\text{PRSNT}}$ = HIGH		9	12	mA
		VDD = 2.5V, $\overline{\text{PRSNT}}$ = HIGH		6	9	mA
LVCMOS / LVTTL DC Specifications						
V_{ih}	High Level Input Voltage		2.0		3.6	V
V_{ih}	High Level Input Voltage	$\overline{\text{PRSNT}}$ pin in 3.3V Mode	0.9 * VIN			V
		$\overline{\text{PRSNT}}$ pin in 2.5V Mode	0.9 * VDD			
V_{il}	Low Level Input Voltage		0		0.7	V
V_{oh}	High Level Output Voltage (DONE pin)	I_{oh} = −4mA	2.0			V
V_{ol}	Low Level Output Voltage (DONE pin)	I_{ol} = 4mA			0.4	V
I_{ih}	Input High Current (PRSNT pin)	VIN Supply = 3.6 V, Input = 3.6 V	-15		+15	uA
	Input High Current with internal resistors (4–level input pin)		+20		+80	uA
I_{il}	Input Low Current (PRSNT pin)	VIN = 3.6 V, Input = 0 V	-15		+15	uA
	Input Low Current with internal resistors (4–level input pin)		-160		-40	uA
CML Receiver Inputs (IN_n+, IN_n-)						
$RL_{rx\text{-}diff}$	RX Differential return loss	0.05 - 1.25 GHz		-16		dB
		1.25 - 2.5 GHz		-16		dB
		2.5 - 4.0 GHz		-14		dB
RLrx-cm	RX Common mode return loss	0.05 - 2.5 GHz		-12		dB
		2.5 - 4.0 GHz		-8		dB
Zrx-dc	RX DC common mode impedance	VDD = 2.5 V	40	50	60	Ω
Zrx-diff-dc	RX DC differntial mode impedance	VDD = 2.5 V	80	100	120	Ω
Vrx-diff-dc	VID - Differential RX peak to peak input voltage		0.6		1.2	V
Zrx-high-imp-dc-pos	DC Input common mode impedance for V>0	VID = 0 to 200mV, ENSMB = 0, RXDET = 0, VDD = 2.5 V		50		KΩ
Vrx-signal-det-diff-pp	Signal detect assert level for active data signal	SD_TH = Float, 0101 pattern at 8 Gbps		180		mVp-p
Vrx-idle-det-diff-pp	Signal detect de-assert level for electrical idle	SD_TH = Float, 0101 pattern at 8 Gbps		110		mVp-p
High Speed Outputs						
$V_{tx\text{-}diff\text{-}pp}$	Output Voltage Differential Swing	Differential measurement with OUT_n+ and OUT_n-, terminated by 50Ω to GND, AC-Coupled, VID = 1.0 Vp-p, DEMA/B = 0, VOD_SEL = Float, (1)	0.8	1.0	1.1	Vp-p
$V_{tx\text{-}de\text{-}ratio\_3.5}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEMA/B = Float, VOD_SEL = Float, (GEN 1, 2)		-3.5		dB

(1) In GEN3 mode, the output VOD level is not fixed. It will be adjusted automatically based on the VID input amplitude level. The output VOD level set by DEMA/B[1:0] in GEN3 mode is dependent on the VID level and the frequency content. The DS80PCI102 repeater in GEN3 mode is designed to be transparent, so the TX-FIR (de-emphasis) is passed to the RX to support the PCIe GEN3 handshake negotiation link training.

ELECTRICAL CHARACTERISTICS (continued)

$V_{tx\text{-}de\text{-}ratio\_6}$	TX de-emphasis ratio	VOD = 1.0 Vp-p, DEMA/B = 20kΩ to GND, VOD_SEL = Float, (GEN 1, 2)		-6		dB
$T_{TX\text{-}RJ}$	Random Ritter	VID = 800 mV, 0101 pattern, 8.0 Gbps, VOD = 1.0V, EQ = 00, DE = 0 dB		0.3		ps (rms)
$T_{TX\text{-}DJ}$	Deterministic Jitter	VID = 800 mV, PRBS15, 8.0 Gbps VOD = 1.0V, EQ = 00, DE = 0 dB		0.1		UI
$T_{TX\text{-}RISE\text{-}FALL}$	TX rise/fall time	20% to 80% of differential output voltage	34	45		ps
$T_{RF\text{-}MISMATCH}$	TX rise/fall mismatch	20% to 80% of differential output voltage		0.01		UI
$RL_{TX\text{-}DIFF}$	TX Differential return loss	0.05 - 1.25 GHz		-16		dB
		1.25 - 2.5 GHz		-12		dB
		2.5 - 4 GHz		-11		dB
$RL_{TX\text{-}CM}$	TX Common mode return loss	0.05 - 2.5 GHz		-12		dB
		2.5 - 4 GHz		-8		dB
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance			100		Ω
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	TX AC common mode voltage	VOD = 1.0 Vp-p, DEMA/B = 0, VOD_SEL = Float			100	mVpp
$I_{TX\text{-}SHORT}$	TX short circuit current limit	Total current the transmitter can supply when shorted to VDD or GND		20		mA
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle				100	mV
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common mode voltgae between TX+ and TX-				25	mV
$T_{TX\text{-}IDLE\text{-}DATA}$	Max time to transition to differential DATA signal after IDLE	VID = 1.0 Vp-p, 8 Gbps		3.5		ns
$T_{TX\text{-}DATA\text{-}IDLE}$	Max time to transition to IDLE after differential DATA signal	VID = 1.0 Vp-p, 8 Gbps		6.5		ns
$T_{PLHD/PHLD}$	High to Low and Low to High Differential Propagation Delay	DE = 0, EQ = 00, (2)		200		ps
T_{LSK}	Lane to lane skew	T = 25C, VDD = 2.5V		25		ps
T_{PPSK}	Part to part propagation delay skew	T = 25C, VDD = 2.5V		40		ps
Equalization						
DJE1	Residual deterministic jitter at 8 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 1F'h,** DEM = 0 dB		0.14		UI
DJE2	Residual deterministic jitter at 5 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 1F'h,** DEM = 0 dB		0.1		UI
DJE3	Residual deterministic jitter at 2.5 Gbps	35” 4mils FR4, VID = 0.8 Vp-p, PRBS15, **EQ = 1F'h,** DEM = 0 dB		0.05		UI
DJE4	Residual deterministic jitter at 8 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.16		UI
DJE5	Residual deterministic jitter at 5 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.1		UI

(2) Propagation Delay measurements will change slightly based on the level of EQ selected. EQ = 00 will result in the shortest propagation delays.

ELECTRICAL CHARACTERISTICS (continued)

DJE6	Residual deterministic jitter at 2.5 Gbps	10 meters 30 awg cable, VID = 0.8 Vp-p, PRBS15, **EQ = 2F'h,** DEM = 0 dB		0.05		UI
De-emphasis (Gen 1&2 mode only)						
DJD1	Residual deterministic jitter at 2.5 Gbps AND 5.0 Gbps	10” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1.0 Vp-p, **DEM = −3.5 dB**		0.1		UI
DJD2	Residual deterministic jitter at 2.5 Gbps AND 5.0 Gbps	20” 4mils FR4, VID = 0.8 Vp-p, PRBS15, EQ = 00, VOD = 1.0 Vp-p, **DEM = −9 dB**		0.1		UI

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	(1)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SCL	(1) (2)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	Pullup V_{DD} = 3.3V, (1) (2) (3)		2000		Ω
		Pullup V_{DD} = 2.5V, (1) (2) (3)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS						
FSMB	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
TBUF	Bus Free Time Between Stop and Start Condition		1.3			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	0.6			µs
TSU:STA	Repeated Start Condition Setup Time		0.6			µs
TSU:STO	Stop Condition Setup Time		0.6			µs
THD:DAT	Data Hold Time		0			ns
TSU:DAT	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period	(4)	0.6		50	µs
t_F	Clock/Data Fall Time	(4)			300	ns
t_R	Clock/Data Rise Time	(4)			300	ns
t_{POR}	Time in which a device must be operational after power-on reset	(4) (5)			500	ms

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
(5) Guaranteed by Design. Parameter not tested in production.

TEST CIRCUIT DIAGRAMS

Timing Diagrams

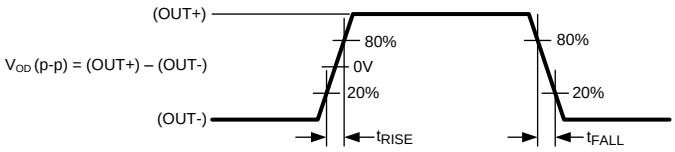


Figure 2. CML Output and Rise and Fall Times

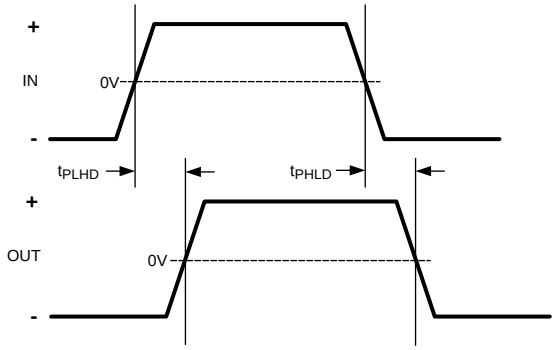


Figure 3. Propagation Delay Timing Diagram

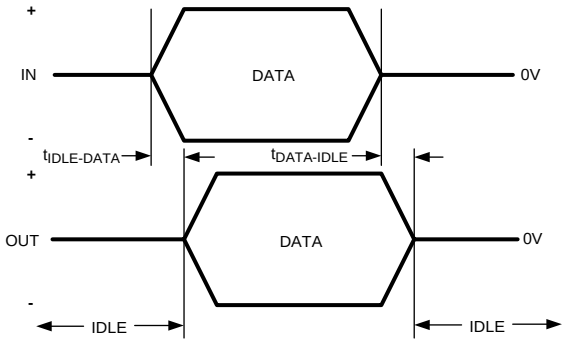


Figure 4. Transmit IDLE-DATA and DATA-IDLE Response Time

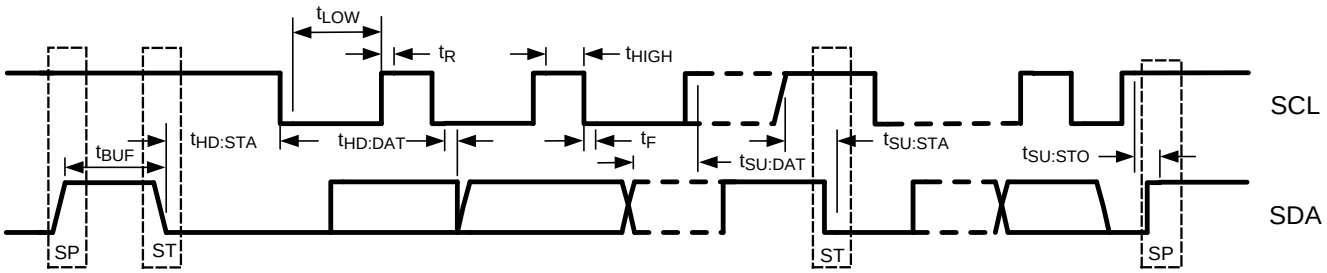


Figure 5. SMBus Timing Parameters

Functional Descriptions

The DS80PCI102 is a low power media compensation 1 lane repeater optimized for PCI Express Gen 1/2 and 3. The DS80PCI102 compensates for lossy FR-4 printed circuit board backplanes and balanced cables. The DS80PCI102 operates in 3 modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = float) to load register informations from external EEPROM; please refer to SMBUS Master Mode for additional information.

Pin Control Mode:

When in pin mode (ENSMB = 0) , the repeater is configurable with external pins. Equalization and de-emphasis can be selected via pin for each side independently. When de-emphasis is asserted VOD is automatically adjusted per the De- Emphasis table below. The receiver detect pins RXDET provides automatic and manual control for input termination (50Ω or >50KΩ). Rate setting is also pin controllable with pin selections (Gen 1/2, auto detect and Gen 3). The receiver electrical idle detect threshold is also adjustable via the SD_TH pin.

SMBUS Mode:

When in SMBus mode, the VOD (output amplitude), equalization, de-emphasis, and termination disable features are all programmable on a individual lane basis, instead of grouped by A or B as in the pin mode case. Upon assertion of ENSMB the RATE, EQx and DEMx functions revert to register control immediately. The EQx and DEMx pins are converted to AD0-AD3 SMBus address inputs. The other external control pins remain active unless their respective registers are written to and the appropriate override bit is set, in which case they are ignored until ENSMB is driven low (pin mode). On power-up and when ENSMB is driven low all registers are reset to their default state. If PRSNT is asserted while ENSMB is high, the registers retain their current state.

Equalization settings accessible via the pin controls were chosen to meet the needs of most PCIe applications. If additional fine tuning or adjustment is needed, additional equalization settings can be accessed via the SMBus registers. Each input has a total of 256 possible equalization settings. The tables show the 16 setting when the device is in pin mode. When using SMBus mode, the equalization, VOD and de-Emphasis levels are set by registers.

The DS80PCI102 has an optional internal voltage regulator to provide the 2.5V supply to the device. In 3.3V mode, the VIN pin = 3.3V is used to supply power to the device and the VDD pins should be left open. The internal regulator will provide the 2.5V to the VDD pins of the device and a 0.1 uF cap is needed at each of 2 VDD pins for power supply de-coupling (total capacitance should be ≤0.25 uF). The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5V mode, the VIN pin should be left open and 2.5V supply must be applied to the VDD pins. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

The input control pins have been enhanced to have 4 different levels and provide a wider range of control settings when ENSMB=0.

Table 1. Equalizer Settings

Level	EQA1 EQB1	EQA0 EQB0	EQ – 8 bits [7:0]	dB at 1.25 GHz	dB at 2.5 GHz	dB at 4 GHz	Suggested Use
1	0	0	0000 0000 = 0x00	2.1	3.7	4.9	FR4 < 5 inch trace
2	0	R	0000 0001 = 0x01	3.4	5.8	7.9	FR4 5 inch 5–mil trace
3	0	Float	0000 0010 = 0x02	4.8	7.7	9.9	FR4 5 inch 4–mil trace
4	0	1	0000 0011 = 0x03	5.9	8.9	11.0	FR4 10 inch 5–mil trace
5	R	0	0000 0111 = 0x07	7.2	11.2	14.3	FR4 10 inch 4–mil trace
6	R	R	0001 0101 = 0x15	6.1	11.4	14.6	FR4 15 inch 4–mil trace
7	R	Float	0000 1011 = 0x0B	8.8	13.5	17.0	FR4 20 inch 4–mil trace
8	R	1	0000 1111 = 0x0F	10.2	15.0	18.5	FR4 25 to 30 inch 4–mil trace
9	Float	0	0101 0101 = 0x55	7.5	12.8	18.0	FR4 30 inch 4–mil trace
10	Float	R	0001 1111 = 0x1F	11.4	17.4	22.0	FR4 35 inch 4–mil trace
11	Float	Float	0010 1111 = 0x2F	13.0	19.7	24.4	10m, 30awg cable

Table 1. Equalizer Settings (continued)

Level	EQA1 EQB1	EQA0 EQB0	EQ – 8 bits [7:0]	dB at 1.25 GHz	dB at 2.5 GHz	dB at 4 GHz	Suggested Use
12	Float	1	0011 1111 = 0x3F	14.2	21.1	25.8	10m – 12m cable
13	1	0	1010 1010 = 0xAA	13.8	21.7	27.4	
14	1	R	0111 1111 = 0x7F	15.6	23.5	29.0	
15	1	Float	1011 1111 = 0xBF	17.2	25.8	31.4	
16	1	1	1111 1111 = 0xFF	18.4	27.3	32.7	

Table 2. De-emphasis and Output Voltage Settings (RATE = GEN 1, 2 and 3)

Level	VOD_SEL	DEMA/DEMB	VOD (Vp-p)	DEM (dB) (see note below	Suggested Use
1	0	0	0.7	0	FR4 <5 inch 4–mil trace
2	0	R	0.7	- 6	FR4 12 inch 4–mil trace
3	0	Float	0.7	- 3.5	FR4 10 inch 4–mil trace
4	0	1	0.7	- 9	FR4 15 inch 4–mil trace
5	R	0	1.2	0	FR4 <5 inch 4–mil trace
6	R	R	1.2	- 6	FR4 12 inch 4–mil trace
7	R	Float	1.2	- 3.5	FR4 10 inch 4–mil trace
8	R	1	1.2	- 9	FR4 15 inch 4–mil trace
9	Float	0	1.0	0	FR4 <5 inch 4–mil trace
10	Float	R	1.0	- 6	FR4 15 inch 4–mil trace
11	Float	Float	1.0	- 3.5	FR4 10 inch 4–mil trace
12	Float	1	1.0	- 9	FR4 20 inch 4–mil trace
13	1	0	1.1	0	FR4 <5 inch 4–mil trace
14	1	R	1.1	- 1.5	FR4 5 inch 4–mil trace
15	1	Float	1.3	- 1.5	FR4 5 inch 4–mil trace
16	1	1	1.3	- 3.5	FR4 10 inch 4–mil trace

Note: The VOD output amplitude and DEM de-emphasis levels are set with the VOD_DEL and DEMA/B pins. The de-emphasis levels are available in GEN1, GEN2 & GEN 3 modes when RATE = AUTO (FLOAT).

Table 3. RX-Detect Settings

PRSNT#	RXDET	Input Termination	Termination sensed on output pins	Comments
0	0	Hi-Z	X	Manual RX-Detect, input is high impedance mode
0	Tie 20kΩ to GND	Pre Detect: Hi-Z Post Detect: 50 Ω	High Z until receiver is detected	Auto RX-Detect, outputs test every 12 msec for 600 msec then stops; termination is high-z until detection; once detected input termination is 50 Ω Reset function by pulsing PRSNT# high for 5 usec then low again
0	Float (Default)	Pre Detect: Hi-Z Post Detect: 50 Ω	High Z until recevier is detected	Auto RX-Detect, outputs test every 12 msec until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω
0	1	50 Ω	X	Manual RX-Detect, input is 50 Ω
1	X	High Impedance	X	Power down mode, input is high impedance, output drivers are disabled. Used to reset RX-Detect State Machine when held high for 5 usec

Table 4. Signal Detect Threshold Level

SD_TH	SMBus REG bit [3:2] and [1:0]	Assert Level (typ)	De-assert Level (typ)
0	10	210 mVp-p	150 mVp-p
R	01	160 mVp-p	100 mVp-p
F (default)	00	180 mVp-p	110 mVp-p

Table 4. Signal Detect Threshold Level (continued)

1	11	190 mVp-p	130 mVp-p
Note: VDD = 2.5V, 25°C and 0101 pattern at 8 Gbps			

APPLICATION INFORMATION

4-Level Input Configuration Guidelines

The 4-level input pins utilize a resistor divider to help set the 4 valid levels. There is an internal 30K pull-up and a 60K pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull-down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

Table 5. 4-Level Input Voltage

Level	Setting	3.3V Mode	2.5V Mode
0	1K to GND	0.1 V	0.08 V
R	20K to GND	0.33 * V_{IN}	0.33 * V_{DD}
F	FLOAT	0.67 * V_{IN}	0.67 * V_{DD}
1	1K to V_{DD}/V_{IN}	V_{IN} - 0.05V	V_{DD} - 0.04V

- Typical 4-Level Input Thresholds
  - Level 1 - 2 = 0.2 V_{IN} or V_{DD}
  - Level 2 - 3 = 0.5 V_{IN} or V_{DD}
  - Level 3 - 4 = 0.8 V_{IN} or V_{DD}

In order to minimize the startup current associated with the integrated 2.5V regulator the 1K pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1K resistors into a single lower value resistor. As an example; combining two inputs with a single 500Ω resistor is a good way to save board space. For the 20KΩ to GND, this should also scale to 10KΩ.

PCB Layout Guidelines

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on WQFN packages.

Different transmission line topologies can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at vias can be minimized or eliminated by increasing the swell around each hole and providing for a low inductance return current path. When the via structure is associated with thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high frequency effects of stubs on the signal path.

Power Supply Configuration Guidelines

The DS80PCI102 can be configured for 2.5V operation or 3.3V operation. The lists below outline required connections for each supply selection.

3.3V Mode of Operation

1. Tie VDD_SEL = 0 with 1K resistor to GND.
2. Feed 3.3V supply into VIN pin. Local 1.0 uF decoupling at VIN is recommended.
3. See information on VDD bypass below.
4. SDA and SCL pins should connect pull-up resistor to VIN
5. Any 4-Level input which requires a connection to "Logic 1" should use a 1K resistor to VIN

2.5V Mode of Operation

6. VDD_SEL = Float
7. VIN = Float
8. Feed 2.5V supply into VDD pins.
9. See information on VDD bypass below.

10. SDA and SCL pins connect pull-up resistor to VDD for 2.5V uC SMBus IO
11. SDA and SCL pins connect pull-up resistor to VDD for 3.3V uC SMBus IO
12. Any 4-Level input which requires a connection to "Logic 1" should use a 1K resistor to VIN

Note: The DAP (bottom solder pad) is the GND connection.

Power Supply Bypass

Two approaches are recommended to ensure that the DS80PCI102 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the device. Smaller body size capacitors can help facilitate proper component placement.

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. ENSMB must be pulled high to enable SMBus mode and allow access to the configuration registers.

The DS80PCI102 has AD[3:0] inputs in SMBus mode. These pins are the user set SMBus slave address inputs. When pulled low the AD[3:0] = 0000'b, the device default address byte is B0'h. Based on the SMBus 2.0 specification, this configuration results in a 7-bit slave address of 1011000'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1011 0000'b or B0'h. The device address byte can be set with the use of the AD[3:0] inputs.

Shown in the form of an expression:

Slave Address [7:4] = The DS80PCI102 hardware address (1011'b) + Address pin AD[3]

Slave Address [3:1] = Address pins AD[2:0]

Slave Address [0] = 0'b for a WRITE or 1'b for a READ

Slave Address Examples:

- AD[3:0] = 0001'b, the device slave address byte is B2'h
  - Slave Address [7:4] = 1011'b + 0'b = 1011'b or B'h
  - Slave Address [3:1] = 001'b
  - Slave Address [0] = 0'b for a WRITE
- AD[3:0] = 0010'b, the device slave address byte is B4'h
  - Slave Address [7:4] = 1011'b + 0'b = 1011'b or B'h
  - Slave Address [3:1] = 010'b
  - Slave Address [0] = 0'b for a WRITE
- AD[3:0] = 0100'b, the device slave address byte is B8'h
  - Slave Address [7:4] = 1011'b + 0'b = 1011'b or B'h
  - Slave Address [3:1] = 100'b
  - Slave Address [0] = 0'b for a WRITE
- AD[3:0] = 1000'b, the device slave address byte is C0'h
  - Slave Address [7:4] = 1011'b + 1'b = 1100'b or C'h
  - Slave Address [3:1] = 000'b
  - Slave Address [0] = 0'b for a WRITE

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see SMBus Register Map Table for more information.

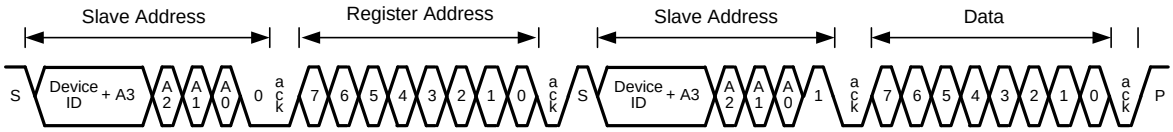


Figure 6. Typical SMBus Write Operation

EEPROM Modes in DS80PCI102 Devices

The DS80PCI102 supports reading directly from an external EEPROM device by implementing SMBus Master mode. When using the SMBus master mode, the DS80 will read directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user needs to follow these specific guidelines.

- Set the DS80PCI102 into SMBus Master Mode
  - Float ENSMB (PIN 3)
- The external EEPROM device must support 400 KHz operation

- The external EEPROM device address byte must be 0xA0'h
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is B0'h.
- Based on the SMBus 2.0 specification, a device can have a 7-bit slave address of 1010 000'b. The LSB is set to 0'b (for a WRITE). The bit mapping for SMBus is listed below:
  - [7:5] = Reserved Bits from the SMBus specification
  - [4:1] = Usable SMBus Address Bits
  - [0] = Write Bit
- The DS80PCI102 devices have AD[3:0] inputs in SMBus mode (pins 1, 2, 9, 10). These pins set SMBus slave address. When the AD[3:0] = 0001'b, the device address byte is B2'h.
  - [7:5] = Default to 3b'101
  - [4:1] = Address of 4'b0001
  - [0] = Write Bit, 1'b0
- The device address can be set with the use of the AD[3:0] input up to 16 different addresses. Use the example below to set each of the SMBus addresses.
  - AD[3:0] = 0001'b, the device address byte is B2'h
  - AD[3:0] = 0010'b, the device address byte is B4'h
  - AD[3:0] = 0011'b, the device address byte is B6'h
  - AD[3:0] = 0100'b, the device address byte is B8'h
- The master implementation in the DS80PCI102 supports multiple devices reading from 1 EEPROM. When tying multiple devices to the SDA and SCL pins, use these guidelines:
  - Use adjacent SMBus addresses for the 4 devices
  - Use a pull-up resistor on SDA; value = 4.7KΩ
  - Use a pull-up resistor on SCL: value = 4.7KΩ
  - Daisy-chain READEN# (pin 17) and DONE# (pin18) from one device to the next device in the sequence
    1. Tie READEN# of the 1st device in the chain (U1) to GND
    2. Tie DONE# of U1 to READEN# of U2
    3. Tie DONE# of U2 to READEN# of U3
    4. Tie DONE# of U3 to READEN# of U4
    5. Optional: Tie DONE# of U4 to a LED to show each of the devices have been loaded successfully

Master EEPROM Mode in the DS80PCI102

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS80PCI102 device. The first 3 bytes of the EEPROM always contain a header common and necessary to control initialization of all devices connected to the I2C bus. CRC enable flag to enable/disable CRC checking. There is a MAP bit to flag the presence of an address map that specifies the configuration data start in the EEPROM. If the MAP bit is not present the configuration data start address is derived from the DS80PCI102 address and the configuration data size. A bit to indicate an EEPROM size > 256 bytes is necessary to properly address the EEPROM. There are 37 bytes of data size for each DS80PCI102 device.

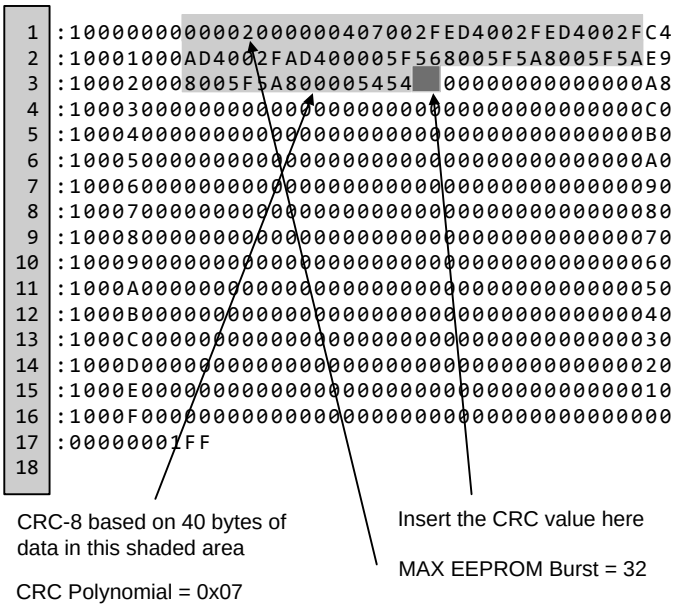


Figure 7. Typical EEPROM Data Set

The CRC-8 calculation is performed on the first 3 bytes of header information plus the 37 bytes of data for the DS80PCI102 or 40 bytes in total. The result of this calculation is placed immediately after the DS80PCI102 data in the EEPROM which ends with "5454". The CRC-8 in the DS80PCI102 uses a polynomial = $x^8 + x^2 + x + 1$

In SMBus master mode the DS80PCI102 reads its initial configuration from an external EEPROM upon power-up. Some of the pins of the DS80PCI102 perform the same functions in SMBus master and SMBus slave mode. Once the DS80PCI102 has finished reading its initial configuration from the external EEPROM in SMBus master mode it reverts to SMBus slave mode and can be further configured by an external controller over the SMBus. The connection to an external SMBus master is optional and can be omitted for applications were additional security is desirable. There are two pins that provide unique functions in SMBus master mode.

- DONE#
- READEN#

When the DS80PCI102 is powered up in SMBus master mode, it reads its configuration from the external EEPROM when the READEN# pin goes low. When the DS80PCI102 is finished reading its configuration from the external EEPROM, it drives the DONE# pin low. In applications where there is more than one DS80PCI102 on the same SMBus, bus contention can result if more than one DS80PCI102 tries to take control of the SMBus at the same time. The READEN# and DONE# pins prevent this bus contention. The system should be designed so that the READEN# pin from one DS80PCI102 in the system is driven low on power-up. This DS80PCI102 will take command of the SMBus on power-up and will read its initial configuration from the external EEPROM. When it is finished reading its configuration, it will drive the DONE# pin low. This pin should be connected to the READEN# pin of another DS80PCI102. When this DS80PCI102 senses its READEN# pin driven low, it will take command of the SMBus and read its initial configuration from the external EEPROM, after which it will set its DONE# pin low. By connecting the DONE# pin of each DS80PCI102 to the READEN# pin of the next DS80PCI102, each DS80PCI102 can read its initial configuration from the EEPROM without causing bus contention.

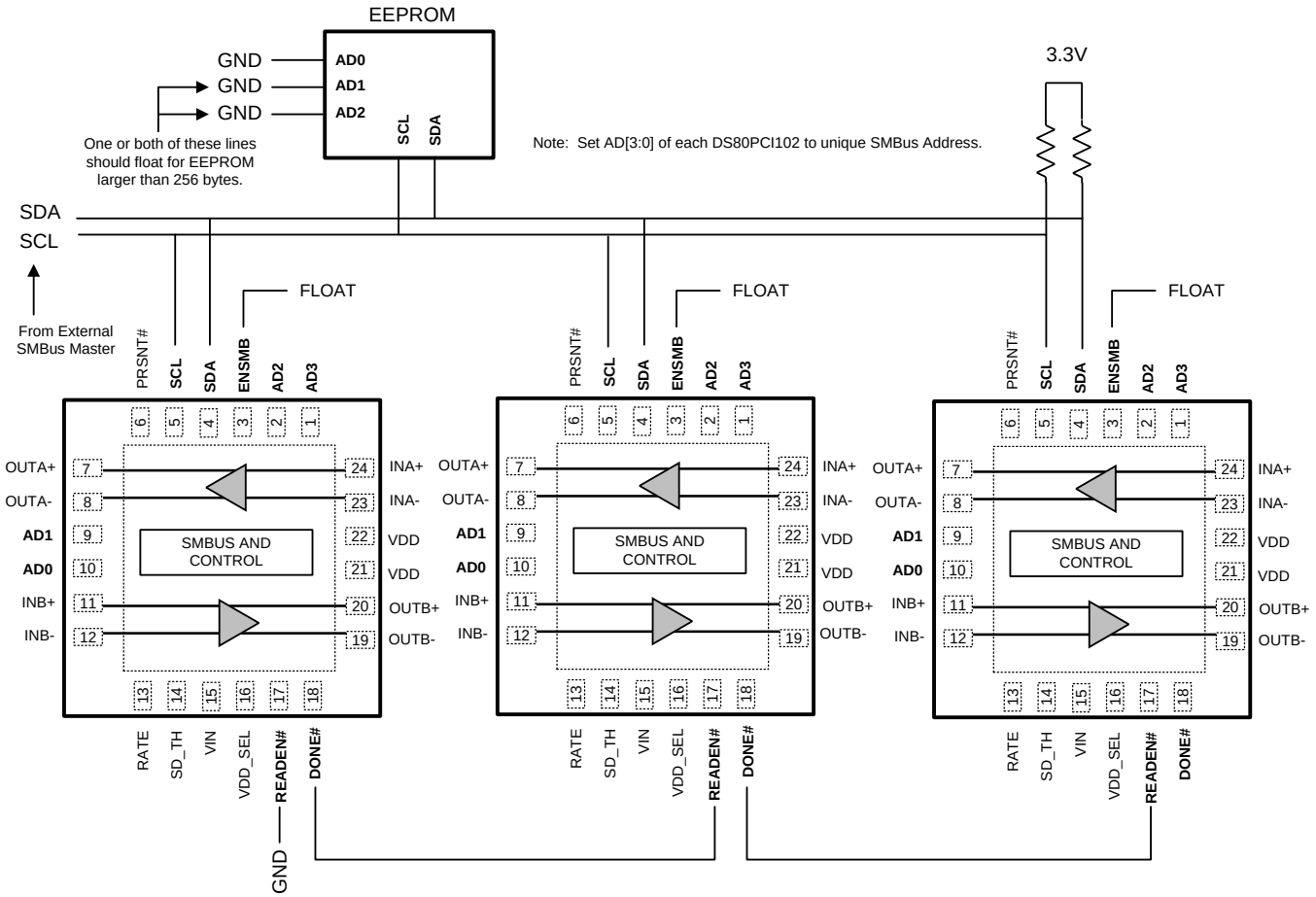


Figure 8. Typical multi-device EEPROM connection diagram

Table 6. Multi-Device EEPROM Register Map Overview

	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIt 0
Header	0	CRC EN	Address Map	EEPROM > 256 Bytes	Reserved	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
	1	RES	RES	RES	RES	RES	RES	RES	RES
	2	EE Burst[7]	EE Burst[6]	EE Burst[5]	EE Burst[4]	EE Burst[3]	EE Burst[2]	EE Burst[1]	EE Burst[0]
Device 0 Info	3	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	4	EE AD0 [7]	EE AD0 [6]	EE AD0 [5]	EE AD0 [4]	EE AD0 [3]	EE AD0 [2]	EE AD0 [1]	EE AD0 [0]
Device 1 Info	5	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	6	EE AD1 [7]	EE AD1 [6]	EE AD1 [5]	EE AD1 [4]	EE AD1 [3]	EE AD1 [2]	EE AD1 [1]	EE AD1 [0]
Device 2 Info	7	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	8	EE AD2 [7]	EE AD2 [6]	EE AD2 [5]	EE AD2 [4]	EE AD2 [3]	EE AD2 [2]	EE AD2 [1]	EE AD2 [0]
Device 3 Info	9	CRC[7]	CRC[6]	CRC[5]	CRC[4]	CRC[3]	CRC[2]	CRC[1]	CRC[0]
	10	EE AD3 [7]	EE AD3 [6]	EE AD3 [5]	EE AD3 [4]	EE AD3 [3]	EE AD3 [2]	EE AD3 [1]	EE AD3 [0]
Device 0 Addr 3	11	RES	RES	RES	RES	RES	RES	PWDN CH B	PWDN CH A
Device 0 Addr 4	12	RES	RES	PDWN Inp	PDWN OSC	Ovrd PRST	RES	RES	RES
Device 0 Addr 38	47	DEMA[2] OVRD	DEMA[1] OVRD	DEMA[0] OVRD	VODA[2] OVRD	VODA[1] OVRD	VODA[0] OVRD	RES	RES

Table 6. Multi-Device EEPROM Register Map Overview (continued)

Device 0 Addr 39	48	DEMB[2] OVRD	DEMB[1] OVRD	DEMB[0] OVRD	VODB[2] OVRD	VODB[1] OVRD	VODB[0] OVRD	RES	RES
Device 1 Addr 3	49	RES	RES	RES	RES	RES	RES	PWDN CH B	PWDN CH A
Device 1 Addr 4	50	RES	RES	PDWN Inp	PDWN OSC	Ovrd PRST	RES	RES	RES
Device 1 Addr 38	85	DEMA[2] OVRD	DEMA[1] OVRD	DEMA[0] OVRD	VODA[2] OVRD	VODA[1] OVRD	VODA[0] OVRD	RES	RES
Device 1 Addr 39	86	DEMB[2] OVRD	DEMB[1] OVRD	DEMB[0] OVRD	VODB[2] OVRD	VODB[1] OVRD	VODB[0] OVRD	RES	RES
Device 2 Addr 3	87	RES	RES	RES	RES	RES	RES	PWDN CH B	PWDN CH A
Device 2 Addr 4	88	RES	RES	PDWN Inp	PDWN OSC	Ovrd PRST	RES	RES	RES
Device 2 Addr 38	124	DEMA[2] OVRD	DEMA[1] OVRD	DEMA[0] OVRD	VODA[2] OVRD	VODA[1] OVRD	VODA[0] OVRD	RES	RES
Device 2 Addr 39	125	DEMB[2] OVRD	DEMB[1] OVRD	DEMB[0] OVRD	VODB[2] OVRD	VODB[1] OVRD	VODB[0] OVRD	RES	RES
Device 3 Addr 3	126	RES	RES	RES	RES	RES	RES	PWDN CH B	PWDN CH A
Device 3 Addr 4	127	RES	RES	PDWN Inp	PDWN OSC	Ovrd PRST	RES	RES	RES
Device 3 Addr 38	163	DEMA[2] OVRD	DEMA[1] OVRD	DEMA[0] OVRD	VODA[2] OVRD	VODA[1] OVRD	VODA[0] OVRD	RES	RES
Device 3 Addr 39	164	DEMB[2] OVRD	DEMB[1] OVRD	DEMB[0] OVRD	VODB[2] OVRD	VODB[1] OVRD	VODB[0] OVRD	RES	RES

- CRC EN = 1
- Address Map = 1
- EEPROM > 256 Bytes = 0

Table 7. Single EEPROM Header + Register Map with Default Value

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	BIt 0
Description	0	CRC EN	Address Map Present	EEPROM > 256 Bytes	Reserved	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]
Value		0	0	0	0	0	0	0	0
Description	1	RES	RES	RES	RES	RES	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	2	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Value		0	0	0	0	0	0	0	0
Description	3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PWDN CH B	PWDN CH A
Register								0x01 [1]	0x01 [0]
Value		0	0	0	0	0	0	0	0
Description	4	Reserved	Reserved	PDWN Inp	PWDN Osc	Ovrd PRST	Reserved	Reserved	Reserved
Register				0x02 [3]	0x02 [2]	0x02 [0]			
Value		0	0	0	0	0	0	0	0
Description	5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Overide IDLE_th	Ovrd VID
Register					0x04 [1]	0x04 [0]		0x08 [6]	0x08 [5]
Value		0	0	0	0	0	1	0	0

Table 7. Single EEPROM Header + Register Map with Default Value (continued)

Description	6	Ovrd_IDLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x08 [4]							
Value		0	0	0	0	0	1	1	1
Description	7	Reserved	Reserved	Reserved	Reserved	Idle auto A	Idle sel A	Reserved	Reserved
Register						0x0E [5]	0x0E [4]		
Value		0	0	0	0	0	0	0	0
Description	8	CHA EQ[7]	CHA EQ[6]	CHA EQ[5]	CHA EQ[4]	CHA EQ[3]	CHA EQ[2]	CHA EQ[1]	CHA EQ[0]
Register		0x0F [7]	0x0F [6]	0x0F [5]	0x0F [4]	0x0F [3]	0x0F [2]	0x0F [1]	0x0F [0]
Value		0	0	1	0	1	1	1	1
Description	9	A Sel scp	A Sel lim	CHA VID[2]	CHA VID[1]	CHA VID[0]	Reserved	Reserved	Reserved
Register		0x10 [7]	0x10 [6]	0x10 [5]	0x10 [4]	0x10 [3]			
Value		1	0	1	0	1	1	0	1
Description	10	DEMA[2]	DEMA[1]	DEMA[0]	CHA Slow	IDLE tha[1]	IDLE tha[0]	IDLE thd[1]	IDLE thd[0]
Register		0x11 [2]	0x11 [1]	0x11 [0]	0x12 [7]	0x12 [3]	0x12 [2]	0x12 [1]	0x12 [0]
Value		0	1	0	0	0	0	0	0
Description	11	Idle auto B	Idle sel B	Reserved	Reserved	CHB EQ[7]	CHB EQ[6]	CHB EQ[5]	CHB EQ[4]
Register		0x15 [5]	0x15 [4]			0x16 [7]	0x16 [6]	0x16 [5]	0x16 [4]
Value		0	0	0	0	0	0	1	0
Description	12	CHB EQ[3]	CHB EQ[2]	CHB EQ[1]	CHB EQ[0]	B Sel scp	B Sel lim	CHB VID[2]	CHB VID[1]
Register		0x16 [3]	0x16 [2]	0x16 [1]	0x16 [0]	0x17 [7]	0x17 [6]	0x17 [5]	0x17 [4]
Value		1	1	1	1	1	0	1	0
Description	13	CHB VID[0]	Reserved	Reserved	Reserved	CHB DEM[2]	CHB DEM[1]	CHB DEM[0]	CHB Slow
Register		0x17 [3]				0x18 [2]	0x18 [1]	0x18 [0]	0x19 [7]
Value		1	1	0	1	0	1	0	0
Description	14	IDLE tha[1]	IDLE tha[0]	IDLE thd[1]	IDLE thd[0]	Reserved	Reserved	Reserved	Reserved
Register		0x19 [3]	0x19 [2]	0x19 [1]	0x19 [0]				
Value		0	0	0	0	0	0	0	0
Description	15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	1	0	1	1	1	1
Description	16	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	1	0	1	1	0	1
Description	17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	0	0	0	0	0
Description	18	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register			0x23 [4]	0x23 [3]	0x23 [2]				
Value		0	0	0	0	0	0	1	0
Description	19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PCI102 CHA VOD[2]
Register									0x25 [4]
Value		1	1	1	1	1	0	1	0
Description	20	PCI102 CHA VOD[1]	PCI102 CHA VOD[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x25 [3]	0x25 [2]						
Value		1	1	0	1	0	1	0	0

Table 7. Single EEPROM Header + Register Map with Default Value (continued)

Description	21	Reserved	Reserved	Reserved	Reserved	ovrd fst idle	en hi idle th A	en hi idle th B	en fst idle A
Register						0x28 [6]	0x28 [5]	0x28 [4]	0x28 [3]
Value		0	0	0	0	0	0	0	1
Description	22	en fst idle B	sd mgain A	sd mgain B	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x28 [2]	0x28 [1]	0x28 [0]					
Value		1	0	0	0	0	0	0	0
Description	23	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	1	1	1	1
Description	24	Reserved	Reserved	Reserved	Reserved	CHB VOD[2]	CHB VOD[1]	CHB VOD[0]	Reserved
Register						0x2D [4]	0x2D [3]	0x2D [2]	
Value		0	1	0	1	0	1	1	0
Description	25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	0	0	0	0	0	0
Description	26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	1	0	1
Description	27	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	1	1	1	0	1	0	1
Description	28	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	1	0	1	0	0	0
Description	29	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	0	0	0
Description	30	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	1	1	1	1
Description	31	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	1	0	1	1	0	1	0
Description	32	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	0	0	0	0	0	0
Description	33	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	1	0	1
Description	34	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	1	1	1	0	1	0	1
Description	35	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		1	0	1	0	1	0	0	0
Description	36	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register									
Value		0	0	0	0	0	0	0	0

Table 7. Single EEPROM Header + Register Map with Default Value (continued)

Description	37	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DEM VOD OVRD
Register									0x59 [0]
Value		0	0	0	0	0	0	0	0
Description	38	DEMA[2] OVRD	DEMA[1] OVRD	DEMA[0] OVRD	VODA[2] OVRD	VODA[1] OVRD	VODA[0] OVRD	Reserved	Reserved
Register		0x5A [7]	0x5A [6]	0x5A [5]	0x5A [4]	0x5A [3]	0x5A [2]		
Value		0	1	0	1	0	1	0	0
Description	39	DEMB[2] OVRD	DEMB[1] OVRD	DEMB[0] OVRD	VODB[2] OVRD	VODB[1] OVRD	VODB[0] OVRD	Reserved	Reserved
Register		0x5B [7]	0x5B [6]	0x5B [5]	0x5B [4]	0x5B [3]	0x5B [2]		
Value		0	1	0	1	0	1	0	0

Below is an example of a 2 kbits (256 x 8-bit) EEPROM Register Dump in hex format for a multi-device DS80PCI102 application.

Table 8. Multi DS80PCI102 EEPROM Data

EEPROM Address	Address (Hex)	EEPROM Data	Comments
0	00	0x43	CRC_EN = 0, Address Map = 1, Device Count = 3 (Devices 0, 1, 2, and 3)
1	01	0x00	
2	02	0x08	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x30	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x0B	Device 3 Address Location
11	0B	0x00	Begin Device 0 and Device 3 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x2F	Default EQ CHA
17	11	0xED	
18	12	0x40	
19	13	0x02	Default EQ CHB
20	14	0xFE	Default EQ CHB
21	15	0xD4	
22	16	0x00	
23	17	0x2F	
24	18	0xAD	
25	19	0x40	
26	1A	0x32	PCI102 CHA VOD = 1000 mV
27	1B	0xFA	
28	1C	0xD4	
29	1D	0x01	
30	1E	0x80	

Table 8. Multi DS80PCI102 EEPROM Data (continued)

EEPROM Address	Address (Hex)	EEPROM Data	Comments
31	1F	0x5F	
32	20	0x56	PCI102 CHB VOD = 1000 mV
33	21	0x80	
34	22	0x05	
35	23	0xF5	
36	24	0xA8	
37	25	0x00	
38	26	0x5F	
39	27	0x5A	
40	28	0x80	
41	29	0x05	
42	2A	0xF5	
43	2B	0xA8	
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	
47	2F	0x54	End Device 0 and Device 3 - Address Offset 39
48	30	0x00	Begin Device 1 and Device 2 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x2F	Default EQ CHA
54	36	0xED	
55	37	0x40	
56	38	0x02	Default EQ CHB
57	39	0xFE	Default EQ CHB
58	3A	0xD4	
59	3B	0x00	
60	3C	0x2F	
61	3D	0xAD	
62	3E	0x40	
63	3F	0x32	PCI102 CHA VOD = 1000 mV
64	40	0xFA	
65	41	0xD4	
66	42	0x01	
67	43	0x80	
68	44	0x5F	
69	45	0x56	PCI102 CHB VOD = 1000 mV
70	46	0x80	
71	47	0x05	
72	48	0xF5	
73	49	0xA8	
74	4A	0x00	
75	4B	0x5F	
76	4C	0x5A	
77	4D	0x80	

Table 8. Multi DS80PCI102 EEPROM Data (continued)

EEPROM Address	Address (Hex)	EEPROM Data	Comments
78	4E	0x05	
79	4F	0xF5	
80	50	0xA8	
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 1 and Device 2 - Address Offset 39

Table 9. SMBus Register Map

Address	Register Name	Bits	Field	Type	Default	EEPROM Reg Bit	Description
0x00	Device ID	7	Reserved	R/W	0x00		set bit to 0
		6:3	I2C Address [3:0]	R			[6:3] SMBus strap observation
		2	EEPROM reading done	R			1: EEPROM Loading 0: EEPROM Done Loading
		1	Reserved	RWSC			set bit to 0
		0	Reserved	RWSC			set bit to 0
0x01	Control 1	7:2	Reserved	R/W	0x00		Set bits to 0
		1:0	PWDN A/B			Yes	[1]: Powerdown Channel B (1); Normal Operation (0) [0]: Powerdown Channel A (1); Normal Operation (0)
0x02	Control 2	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3	PWDN Inputs			Yes	Set bit to 0
		2	PWDN Oscillator			Yes	Set bit to 0
		1	Reserved				Set bit to 0
		0	Override PRSNT			Yes	1: Enables Reg 0x01[1:0] 0: Normal Operation
0x04	Reserved	7:0	Reserved	R/W	0x00	Yes	Set bits to 0
0x05	CRC bits	7:0	CRC[7:0]	R/W	0x00		Slave Mode CRC Bits
0x06	CRC Control	7:5	Reserved	R/W	0x10		Set bits to 0
		4	Reserved			Yes	Set bit to 1
		3	Register Mode Enable				[1]: CRC Disable (No CRC Check) [0]: CRC Check ENABLE Note: With CRC check DISABLED register updates take immediate effect on high speed data path. With CRC check ENABLED register updates will NOT take effect until correct CRC value is loaded
		2:0	Reserved				Set bits to 0
0x07	Digital Reset and Control	7	Reserved	R/W	0x01		Set bits to 0
		6	Reset Regs				Self clearing reset for registers. Writing a [1] will return register settings to default values.
		5	Reset SMBus Master				Self clearing reset to SMBus master state machine
		4:0	Reserved				Set bits to '0001b

Table 9. SMBus Register Map (continued)

0x08	Pin Override	7	Reserved	R/W	0x00		Set bit to 0
		6	Override Idle Threshold			Yes	[1]: Override by Channel - see Reg 0x12 and 0x19 [0]: SD_TH pin control
		5:4	Reserved			Yes	Set bits to 0
		3	Override RXDET			Yes	[1]: Force RXDET by Channel - see Reg 0x0E and 0x15 [0]: Normal Operation
		2	Override RATE			Yes	[1]: Override by Channel - see Reg 0x10 and 0x17 [0]: Normal Operation
		1:0	Reserved			Yes	Set bits to 0
0x0C	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0.
0x0D	CH A Reserved	7:0	Reserved	R/W	0x00		Set bits to 0.
0x0E	CH A RXDET Control	7:5	Reserved	R/W	0x00		Set bits to 0.
		4	Reserved			Yes	Set bit to 0.
		3:2	RXDET			Yes	00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved				Set bits to 0.
0x0F	CH A EQ Control	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Control - total of 256 levels 8 bits [7:0] = HEX = dB at 4 GHz 0000 0000 = 0x00 = 4.9dB 0000 0001 = 0x01 = 7.9dB 0000 0010 = 0x02 = 9.9dB 0000 0011 = 0x03 = 11.0dB 0000 0111 = 0x07 = 14.3dB 0001 0101 = 0x15 = 14.6dB 0000 1011 = 0x0B = 17.0dB 0000 1111 = 0x0F = 18.5dB 0101 0101 = 0x55 = 18.0dB 0001 1111 = 0x1F = 22.0dB 0010 1111 = 0x2F = 24.4dB (default) 0011 1111 = 0x3F = 25.8dB 1010 1010 = 0xAA = 27.4dB 0111 1111 = 0x7F = 29.0dB 1011 1111 = 0xBF = 31.4dB 1111 1111 = 0xFF = 32.7dB
0x10	CH A RATE Control	7	Sel_scp	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Sel_RATE			Yes	1 = Select GEN1/2 Mode 0 = Select GEN3 Mode
		5:3	Reserved			Yes	Set bits to 0
		2:0	Reserved			Yes	Set bits to '101b

Table 9. SMBus Register Map (continued)

0x11	CH A DEM Control	7	Reserved	R	0x82		
		6:5	Rate Information				Signal Rate Detected 00 = GEN1 - 2.5G 01 = GEN2 - 5.0G 11 = GEN3 - 8.0G
		4:3	Reserved	R/W			Set bits to 0
		2:0	DEM [2:0]			Yes	DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x12	CH A Idle Threshold	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	idle_thA[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00 = 180 mV (Default) 01 = 160 mV 10 = 210 mV 11= 190 mV
		1:0	idle_thD[1:0]			Yes	De-assert Thresholds Use only if register 0x08 [6] = 1 00 = 110 mV (Default) 01 = 100 mV 10 = 150 mV 11= 130 mV
0x13	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0.
0x14	CH B Reserved	7:0	Reserved	R/W	0x00		Set bits to 0.
0x15	CH B RXDET Control	7:5	Reserved	R/W	0x00		Set bits to 0.
		4	Reserved			Yes	Set bit to 0.
		3:2	RXDET			Yes	00: Input is high-z impedance 01: Auto RX-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is high-z until detection; once detected input termination is 50 Ω 10: Auto RX-Detect, outputs test every 12 ms until detection occurs; termination is high-z until detection; once detected input termination is 50 Ω 11: Input is 50 Ω Note: override RXDET pin.
		1:0	Reserved				Set bits to 0.
0x16	CH B EQ Control	7:0	BOOST [7:0]	R/W	0x2F	Yes	EQ Control - total of 256 levels 8 bits [7:0] = HEX = dB at 4 GHz 0000 0000 = 0x00 = 4.9dB 0000 0001 = 0x01 = 7.9dB 0000 0010 = 0x02 = 9.9dB 0000 0011 = 0x03 = 11.0dB 0000 0111 = 0x07 = 14.3dB 0001 0101 = 0x15 = 14.6dB 0000 1011 = 0x0B = 17.0dB 0000 1111 = 0x0F = 18.5dB 0101 0101 = 0x55 = 18.0dB 0001 1111 = 0x1F = 22.0dB 0010 1111 = 0x2F = 24.4dB (default) 0011 1111 = 0x3F = 25.8dB 1010 1010 = 0xAA = 27.4dB 0111 1111 = 0x7F = 29.0dB 1011 1111 = 0xBF = 31.4dB 1111 1111 = 0xFF = 32.7dB

Table 9. SMBus Register Map (continued)

0x17	CH B RATE Control	7	Sel_scp	R/W	0xED	Yes	1 = Short Circuit Protection ON 0 = Short Circuit Protection OFF
		6	Sel_RATE			Yes	1 = Select GEN1/2 Mode 0 = Select GEN3 Mode
		5:3	Reserved			Yes	Set bits to 0
		2:0	Reserved				Set bits to '101b
0x18	CH B DEM Control	7	Reserved	R	0x02		
		6:5	Rate Information				Signal Rate Detected 00 = GEN1 - 2.5G 01 = GEN2 - 5.0G 11 = GEN3 - 8.0G
		4:3	Reserved	R/W			Set bits to 0
		2:0	DEM [2:0]			Yes	DEM Control 000: 0 dB 001: –1.5 dB 010: –3.5 dB (default) 011: –5 dB 100: –6 dB 101: –8 dB 110: –9 dB 111: –12 dB
0x19	CH B Idle Threshold	7	Reserved	R/W	0x00	Yes	Set bits to 0.
		6:4	Reserved				
		3:2	idle_thA[1:0]			Yes	Assert Thresholds Use only if register 0x08 [6] = 1 00 = 180 mV (Default) 01 = 160 mV 10 = 210 mV 11= 190 mV
		1:0	idle_thD[1:0]			Yes	De-assert Thresholds Use only if register 0x08 [6] = 1 00 = 110 mV (Default) 01 = 100 mV 10 = 150 mV 11= 130 mV
0x25	CH A VOD	7:5	Reserved	R/W	0xAD		Set bits to 0.
		4:2	VOD CHA Control			Yes	VOD Control CHA 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V (default) 100: 1.1 V 101: 1.2 V 110: 1.3 V 111: 1.4 V
		1:0	Reserved				Set bits to 01'b
0x2D	CH B VOD	7:5	Reserved	R/W	0xAD		Set bits to 0
		4:2	VOD CHB Control			Yes	VOD Control CHB 000: 0.7 V 001: 0.8 V 010: 0.9 V 011: 1.0 V (default) 100: 1.1 V 101: 1.2 V 110: 1.3 V 111: 1.4 V
		1:0	Reserved				Set bits to 01'b
0x51	Device Information	7:5	Version[2:0]	R	0x77		Read bits = 011'b
		4:0	Device ID[4:0]				PCI102 = 1 0111'b

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DS80PCI102SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	
DS80PCI102SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	

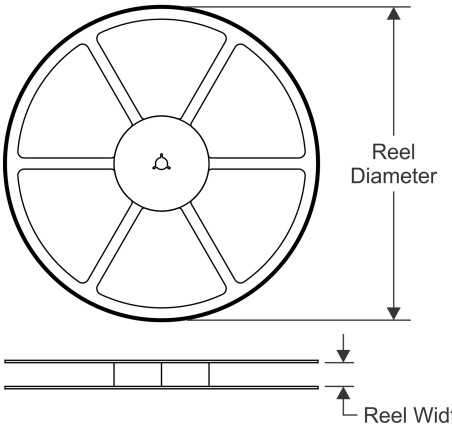
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

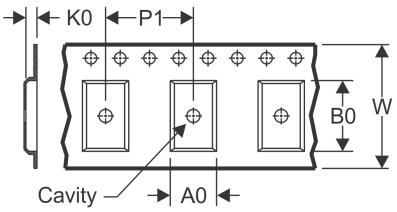
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

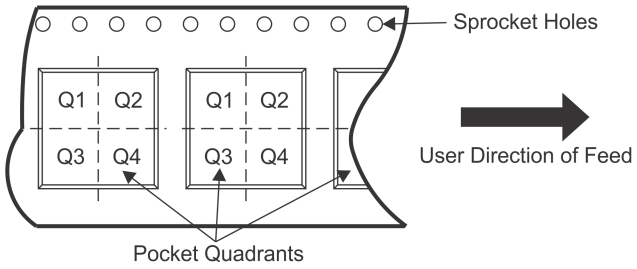


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

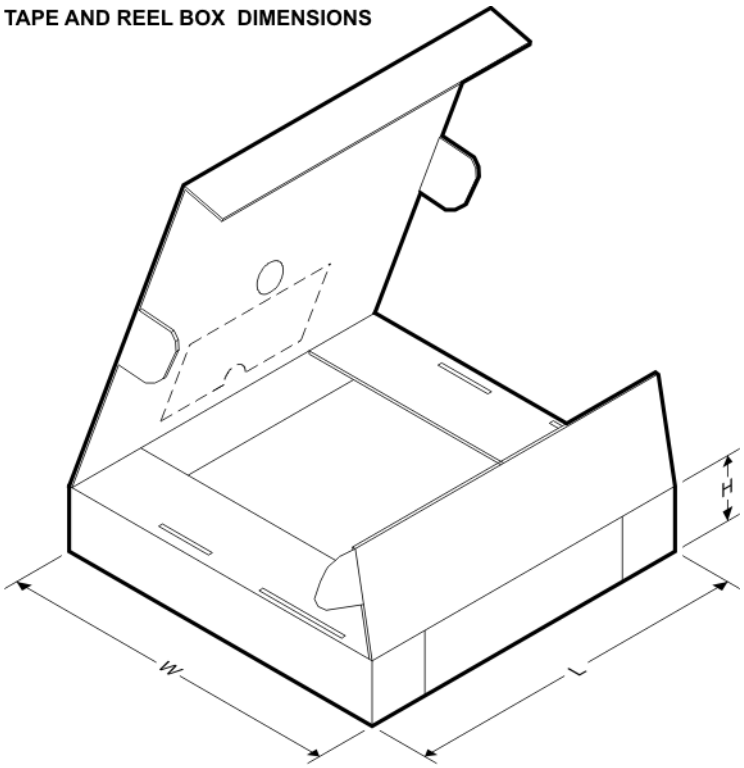
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS80PCI102SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS80PCI102SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

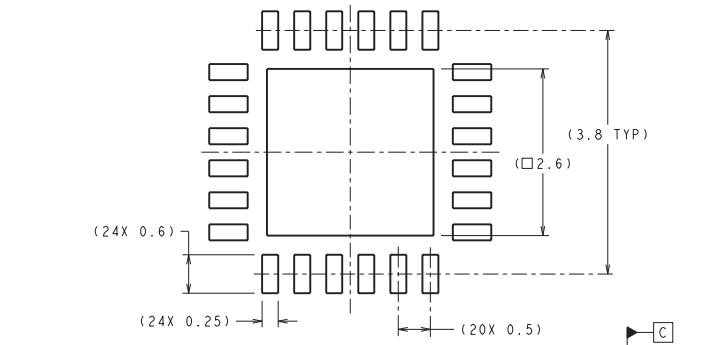
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

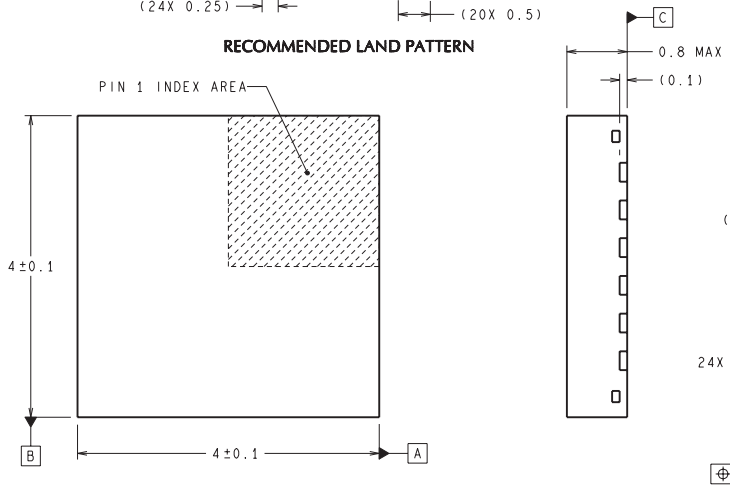
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS80PCI102SQ/NOPB	WQFN	RTW	24	1000	213.0	191.0	55.0
DS80PCI102SQE/NOPB	WQFN	RTW	24	250	213.0	191.0	55.0

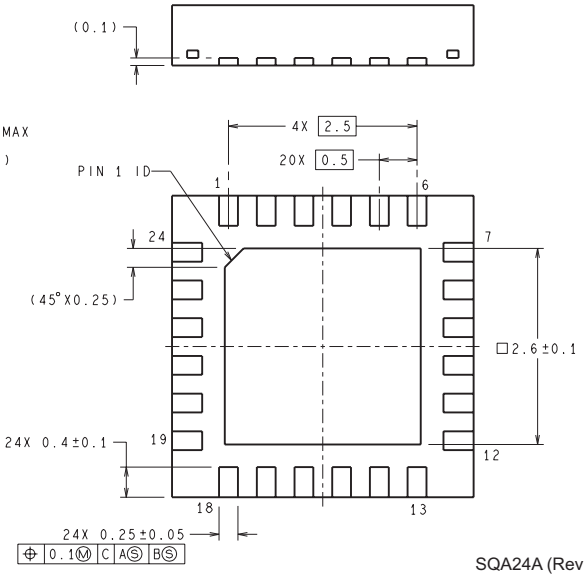
RTW0024A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SQA24A (Rev B)

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