## DS92LV040A 4 Channel Bus LVDS Transceiver

### Check for Samples: DS92LV040A

## FEATURES

- **Bus LVDS Signaling**
- **Propagation Delay: Driver 2.3ns max, Receiver 3.2ns max**
- **Low power CMOS Design**
- **100% Transition Time 1ns Driver Typical, 1.3ns Receiver Typical**
- **High Signaling Rate Capability (above 155 Mbps)**
- **0.1V to 2.3V Common Mode Range for $V_{ID}$ = 200mV**
- **70 mV Receiver Sensitivity**
- **Supports Open and Terminated Failsafe on Port Pins**
- **3.3V Operation**
- **Glitch Free Power up/down (Driver & Receiver Disabled)**
- **Light Bus Loading (5 pF typical) per Bus LVDS Load**
- **Designed for Double Termination Applications**
- **Balanced Output Impedance**

- **Product Offered in 44 Pin WQFN Package**
- **High Impedance Bus Pins on Power Off ($V_{CC}$ = 0V)**

## DESCRIPTION

The DS92LV040A is one in a series of Bus LVDS transceivers designed specifically for high speed, low power backplane or cable interfaces. The device operates from a single 3.3V power supply and includes four differential line drivers and four receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver translates 3V LVTTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation while consuming minimal power and reducing EMI. In addition, the differential signaling provides common mode noise rejection greater than ±1V.

The receiver threshold is less than +0/−70 mV. The receiver translates the differential Bus LVDS to standard (LVTTL/LVCMOS) levels. (See the Applications Information Section for more details.)

## Simplified Functional Diagram
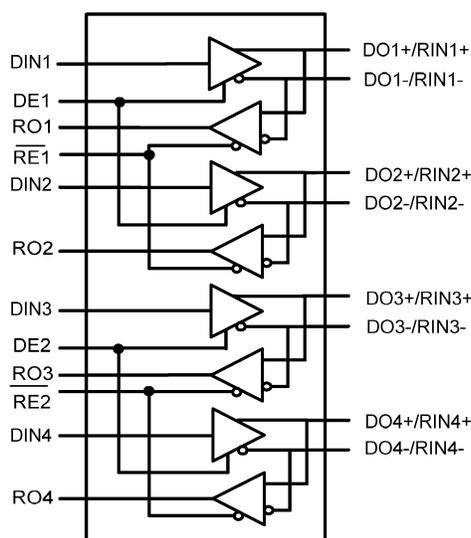
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1][2][3]

| | | |
|---|---|---|
| Supply Voltage ($V_{CC}$) | | 4.0V |
| Enable Input Voltage | (DE, $\overline{RE}$) | −0.3V to ($V_{CC}$ +0.3V) |
| Driver Input Voltage ($D_{IN}$) | | −0.3V to ($V_{CC}$ +0.3V) |
| Receiver Output Voltage | ($R_{OUT}$) | −0.3V to ($V_{CC}$ +0.3V) |
| Bus Pin Voltage (DO/RI±) | | −0.3V to +3.9V |
| ESD[4][5] | | |
| (HBM 1.5 kΩ, 100 pF) | | >4kV |
| Machine Model | | >250V |
| Maximum Package Power Dissipation at 25°C | WQFN[6] | 4.8 W |
| | Derate WQFN Package | 38.8mW/°C |
| | $\theta_{ja}$ [6] | 25.8°C/W |
| | $\theta_{jc}$ | 25.5°C/W |
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | | 260°C |

(1)  If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2)  All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except $V_{OD}$, $\Delta V_{OD}$ and $V_{ID}$.
(3)  "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(4)  All typicals are given for $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise stated.
(5)  ESD Rating: HBM (1.5 kΩ, 100 pF) > 4 kV EIAJ (0Ω, 200 pF) > 250.
(6)  Package must be mounted to pc board in accordance with AN-1187 to achieve thermals.

## Recommended Operating Conditions

| | | Min | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | 3.0 | 3.6 | V |
| Receiver Input Voltage | | 0.0 | 2.4 | V |
| Operating Free Air Temperature | | −40 | +85 | °C |
| Slowest Input Edge Rate | (20% to 80%)[1] | | | Δt/ΔV |
| | Data | | 1.0 | ns/V |
| | Control | | 3.0 | ns/V |

(1)  Generator waveforms for all tests unless otherwise specified: f = 25 MHz, $Z_O$ = 50Ω, $t_r$, $t_f$ = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.

Product Folder Links: *DS92LV040A*

## DC Electrical Characteristics[1]

Over recommended operating supply voltage and temperature ranges unless otherwise specified. [2][3]

| Symbol | Parameter | Conditions | | Pin | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Output Differential Voltage | $R_L = 27\Omega$, Figure 1 | | DO+/RI+, DO−/RI− | 200 | 300 | 460 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | | 5 | 27 | mV |
| $V_{OS}$ | Offset Voltage | | | | 1.1 | 1.3 | 1.5 | V |
| $\Delta V_{OS}$ | Offset Magnitude Change | | | | | 5 | 10 | mV |
| $V_{OHD}$ | Driver Output High Voltage | $R_L = 27\Omega$ | | | | 1.4 | 1.65 | V |
| $V_{OLD}$ | Driver Output Low Voltage | $R_L = 27\Omega$ | | | 0.95 | 1.1 | | V |
| $I_{OSD}$ | Driver Output Short Circuit Current[4] | $V_{OD} = 0V$, DE = $V_{CC}$, Driver outputs shorted together | | | | \|30\| | \|45\| | mA |
| $V_{OHR}$ | Receiver Voltage Output High[5] | $V_{ID} = +300$ mV | $I_{OH} = -4$ mA | $R_{OUT}$ | $V_{CC}-0.2$ | | | V |
| | | Inputs Open | | | $V_{CC}-0.2$ | | | V |
| | | Inputs Terminated, $R_L = 27\Omega$ | | | $V_{CC}-0.2$ | | | V |
| $V_{OLR}$ | Receiver Voltage Output Low | $I_{OL} = 4.0$ mA, $V_{ID} = -300$ mV | | | | 0.05 | 0.100 | V |
| $I_{OD}$ | Receiver Output Dynamic Current[4] | $V_{ID} = 300mV$, $V_{OUT} = V_{CC}-1.0V$ | | | −50 | \|33\| | | mA |
| | | $V_{ID} = -300mV$, $V_{OUT} = 1.0V$ | | | | \|36\| | 60 | mA |
| $V_{TH}$ | Input Threshold High[6] | DE = 0V, Over common mode range | | DO+/RI+, DO−/RI− | | −40 | 0 | mV |
| $V_{TL}$ | Input Threshold Low[6] | | | | −70 | −40 | | mV |
| $V_{CMR}$ | Receiver Common Mode Range | | | | $\|V_{ID}\|/2$ | | $2.4 - \|V_{ID}\|/2$ | V |
| $I_{IN}$ | Input Current | DE = 0V, $\overline{RE} = 2.4V$, $V_{IN} = +2.4V$ or 0V | | | −20 | ±1 | +20 | µA |
| | | $V_{CC} = 0V$, $V_{IN} = +2.4V$ or 0V | | | −20 | ±1 | +20 | µA |
| $V_{IH}$ | Minimum Input High Voltage | | | $D_{IN}$, DE, $\overline{RE}$ | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Maximum Input Low Voltage | | | | GND | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{IN} = V_{CC}$ or 2.4V | | | −20 | ±2.5 | +20 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN} = GND$ or 0.4V | | | −20 | ±2.5 | +20 | µA |
| $V_{CL}$ | Input Diode Clamp Voltage | $I_{CLAMP} = -18$ mA | | | −1.5 | −0.8 | | V |
| $I_{CCD}$ | Power Supply Current Drivers Enabled, Receivers Disabled | No Load, DE = $\overline{RE}$ = $V_{CC}$, DIN = $V_{CC}$ or GND | | $V_{CC}$ | | 20 | 40 | mA |
| $I_{CCR}$ | Power Supply Current Drivers Disabled, Receivers Enabled | DE = $\overline{RE}$ = 0V, $V_{ID}$ = ±300mV | | | | 27 | 40 | mA |
| $I_{CCZ}$ | Power Supply Current, Drivers and Receivers TRI-STATE | DE = 0V; $\overline{RE}$ = $V_{CC}$, DIN = $V_{CC}$ or GND | | | | 28 | 40 | mA |
| $I_{CC}$ | Power Supply Current, Drivers and Receivers Enabled | DE = $V_{CC}$; $\overline{RE}$ = 0V, DIN = $V_{CC}$ or GND, $R_L = 27\Omega$ | | | | 70 | 100 | mA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{CC} = 0V$ or OPEN, $D_{IN}$, DE, $\overline{RE}$ = 0V or OPEN, $V_{APPLIED} = 3.6V$ (Port Pins) | | DO+/RI+, DO−/RI− | −20 | | +20 | µA |
| $C_{OUTPUT}$ | Capacitance @ Bus Pins | | | DO+/RI+, DO−/RI− | | 5 | | pF |
| $c_{OUTPUT}$ | Capacitance @ $R_{OUT}$ | | | $R_{OUT}$ | | 5 | | pF |

(1) The DS92LV040A functions within datasheet specification when a resistive load is applied to the driver outputs.
(2) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except $V_{OD}$, $\Delta V_{OD}$ and $V_{ID}$.
(3) All typicals are given for $V_{CC}$ = +3.3V and $T_A$ = +25°C, unless otherwise stated.
(4) Only one output at a time should be shorted, do not exceed maximum package power dissipation capacity.
(5) $V_{OH}$ fail-safe terminated test performed with 27Ω connected between RI+ and RI− inputs. No external voltage is applied.
(6) Propagation delays, transition times, and receiver threshold are guaranteed by design and characterization.

## AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified. [1]

| Symbol | Parameter | Conditions[2] | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DIFFERENTIAL DRIVER TIMING REQUIREMENTS** | | | | | | |
| $t_{PHLD}$ | Differential Prop. Delay High to Low[3] | $R_L = 27\Omega$, Figure 2, Figure 3, $C_L = 10$ pF | 1.0 | 1.5 | 2.3 | ns |
| $t_{PLHD}$ | Differential Prop. Delay Low to High[3] | | 1.0 | 1.5 | 2.3 | ns |
| $t_{SKD1}$ | Differential Skew $\|t_{PHLD} - t_{PLHD}\|$ (duty cycle)[4] [3] | | | 80 | 160 | ps |
| $t_{CCSK}$ | Channel to Channel Skew (all 4 channels)[3][5] | | | 220 | 400 | ps |
| $t_{TLH}$ | Transition Time Low to High (20% to 80%) | | 0.4 | 0.75 | 1.3 | ns |
| $t_{THL}$ | Transition Time High to Low (80% to 20%) | | 0.4 | 0.75 | 1.3 | ns |
| $t_{PHZ}$ | Disable Time High to Z | $R_L = 27\Omega$, Figure 4, Figure 5, $C_L = 10$ pF | | 5.0 | 10 | ns |
| $t_{PLZ}$ | Disable Time Low to Z | | | 5.0 | 10 | ns |
| $t_{PZH}$ | Enable Time Z to High | | | 5.0 | 10 | ns |
| $t_{PZL}$ | Enable Time Z to Low | | | 5.0 | 10 | ns |
| $f_{MAXD}$ | Guaranteed operation per data sheet up to the Min. Duty Cycle 45/55%, Transition time ≤ 25% of period[3] | | 85 | 125 | | MHz |
| **DIFFERENTIAL RECEIVER TIMING REQUIREMENTS** | | | | | | |
| $t_{PHLDR}$ | Differential Prop. Delay High to Low[3] | Figure 6, Figure 7, $C_L = 15$ pF | 1.6 | 2.4 | 3.2 | ns |
| $t_{PLHDR}$ | Differential Prop Delay Low to High[3] | | 1.6 | 2.4 | 3.2 | ns |
| $t_{SDK1R}$ | Differential Skew $\|t_{PHLD} - t_{PLHD}\|$ (duty cycle)[4][3] | | | 85 | 160 | ps |
| $t_{CCSKR}$ | Channel to Channel Skew (all 4 channels)[3][5] | | | 140 | 300 | ps |
| $t_{TLHR}$ | Transition Time Low to High (10% to 90%)[3] | | 0.850 | 1.250 | 2.0 | ns |
| $t_{THLR}$ | Transition Time High to Low (90% to 10%)[3] | | 0.850 | 1.030 | 2.0 | ns |
| $t_{PHZ}$ | Disable Time High to Z | $R_L = 500\Omega$, Figure 8, Figure 9, $C_L = 15$ pF | | 3.0 | 10 | ns |
| $t_{PLZ}$ | Disable Time Low to Z | | | 3.0 | 10 | ns |
| $t_{PZH}$ | Enable Time Z to High | | | 3.0 | 10 | ns |
| $t_{PZL}$ | Enable Time Z to Low | | | 3.0 | 10 | ns |
| $f_{MAXR}$ | Guaranteed operation per data sheet up to the Min. Duty Cycle 45/55%, Transition time ≤ 25% of period[3] | | 85 | 125 | | MHz |

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, $Z_O = 50\Omega$, $t_r$, $t_f$ = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.
(2) $C_L$ includes probe and fixture capacitance.
(3) Propagation delays, transition times, and receiver threshold are guaranteed by design and characterization.
(4) $t_{SKD1}$ $\|t_{PHLD} - t_{PLHD}\|$ is the worst case pulse skew (measure of duty cycle) over recommended operation conditions.
(5) Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.

## APPLICATIONS INFORMATION

General application guidelines and hints may be found in the following application notes: AN-808, AN-977, AN-971, and AN-903.

BLVDS drivers and receivers are intended to be used in a differential backplane configuration. Transceivers or receivers are connected to the driver through a balanced media such as differential PCB traces. Typically, the characteristic differential impedance of the media (Zo) is in the range of 50Ω to 100Ω. Two termination resistors of ZoΩ each are placed at the ends of the transmission line backplane. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. The effects of mid-stream connector(s), cable stub(s), and other impedance discontinuity as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS92LV040A differential line driver is a balanced current mode design. A current mode driver, generally speaking has a high output impedance (100 ohms) and supplies a reasonably constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). The current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 12 mA. The current changes as a function of load resistor. The current mode requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop. Unterminated configurations are not allowed. The 12 mA loop current will develop a differential voltage of about 300mV across a 27Ω (double terminated 54Ω differential transmission backplane) effective resistance, which the receiver detects with a 230 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (300 mV – 70 mV = 230 mV)). The signal is centered around +1.2V (Driver Offset, $V_{OS}$ ) with respect to ground. Note that the steady-state voltage ($V_{SS}$ ) peak-to-peak swing is twice the differential voltage ($V_{OD}$ ) and is typically 600 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static ICC requirements of the ECL/PECL designs. LVDS requires 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers. The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

There are a few common practices which should be implied when designing PCB for Bus LVDS signaling. Recommended practices are:
- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes. Surface mount capacitors placed close to power and ground pins work best. Three or more high frequency, multi-layer ceramic (MLC) surface mount (0.1 µF, 0.01 µF, 0.001 µF) in parallel should be used between each $V_{CC}$ and ground.
  - Multiple vias should be used to connect $V_{CC}$ and Ground planes to the pads of the by-pass capacitors.
  - In addition, it may be necessary to randomly distribute by-pass capacitors of different values (200pF to 1000pF) to achieve different resonant frequencies.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating). Limit traces on unused inputs to <0.5 inches.
- Isolate TTL signals from Bus LVDS signals

MEDIA (CONNECTOR or BACKPLANE) SELECTION:
- The backplane and connectors should have a matched differential impedance. Use controlled impedance traces which match the differential impedance of your transmission medium (ie. backplane or cable) and termination resistor(s). Run the differential pair trace lines as close together as possible as soon as they leave the IC . This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver. Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between

signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuity on the line. Avoid 90° turns (these cause impedance discontinuity). Use arcs or 45° bevels. Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuity in differential impedance. Minor violations at connection points are allowable.

• Stub Length: Stub lengths should be kept to a minimum. The typical transition time of the DS92LV040A BLVDS output is 0.75ns (20% to 80%). The extrapolated 100 percent time is 0.75/0.6 or 1.25ns. For a general approximation, if the electrical length of a trace is greater than 1/5 of the transition edge, then the trace is considered a transmission line. For example, 1.25ns/5 is 250 picoseconds. Let velocity equal 160ps per inch for a typical loaded backplane. Then maximum stub length is 250ps/160ps/in or 1.56 inches. To determine the maximum stub for your backplane, you need to know the propagation velocity for the actual conditions (refer to application notes AN 905 and AN 808).

PACKAGE and SOLDERING INFORMATION:

• Refer to packaging application note AN-1187. This application note details the package attachment methods to achieve the correct solderability and thermal results.

**Table 1. Functional Table**

| MODE SELECTED | DE | $\overline{RE}$ |
|---|---|---|
| DRIVER MODE | H | H |
| RECEIVER MODE | L | L |
| TRI-STATE™ MODE | L | H |
| LOOP BACK MODE | H | L |

**Table 2. Transmitter Mode**

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| DE | D$_{IN}$ | DO+ | DO− |
| H | L | L | H |
| H | H | H | L |
| H | 0.8V< D$_{IN}$ <2.0V | X | X |
| L | X | Z | Z |

**Table 3. Receiver Mode**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{RE}$ | (RI+) − (RI−) | |
| L | L (< −70 mV) | L |
| L | H (> 0 mV) | H |
| L | −70 mV < V$_{ID}$ < 0 mV | X |
| H | X | Z |

## Test Circuits and Timing Waveforms
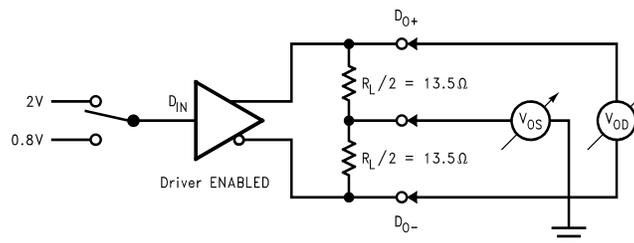


**Figure 1. Differential Driver DC Test Circuit**

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Product Folder Links: *DS92LV040A*
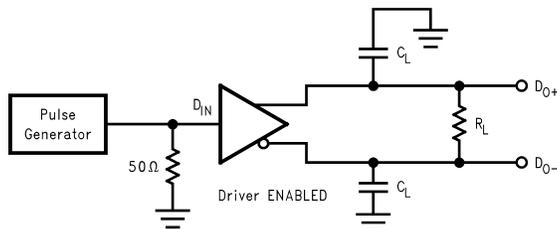
**Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit**
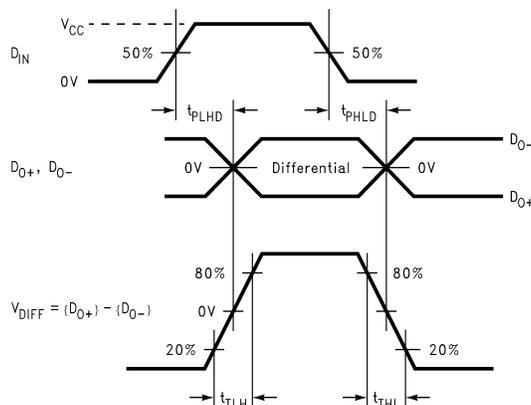


**Figure 3. Differential Driver Propagation Delay and Transition Time Waveforms**
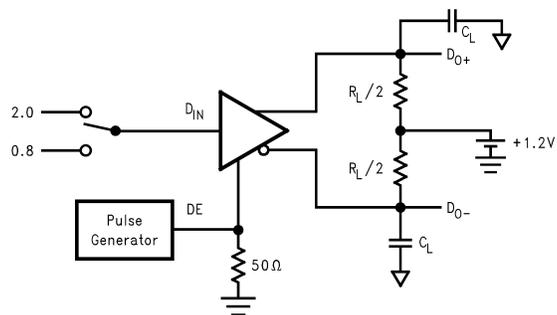


**Figure 4. Driver TRI-STATE™ Delay Test Circuit**
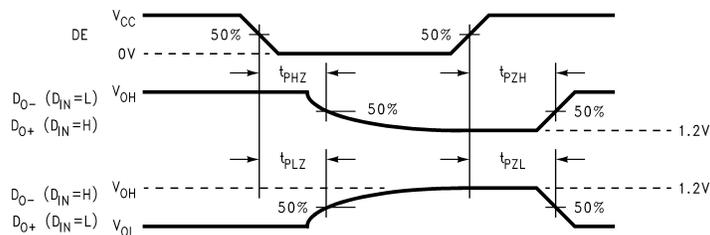


**Figure 5. Driver TRI-STATE™ Delay Waveforms**

Product Folder Links: *DS92LV040A*
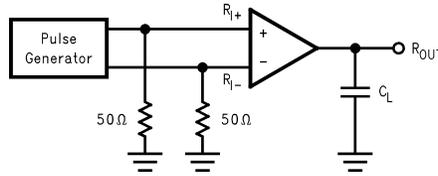
**Figure 6. Receiver Propagation Delay and Transition Time Test Circuit**
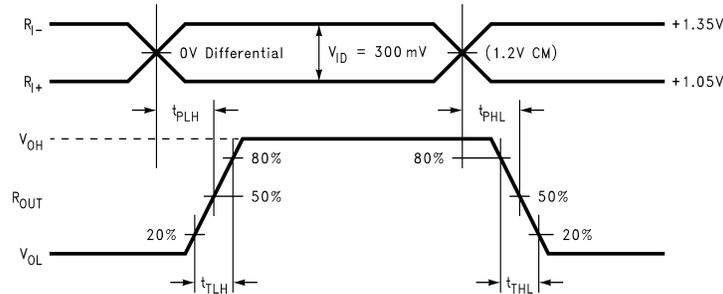


**Figure 7. Receiver Propagation Delay and Transition Time Waveforms**
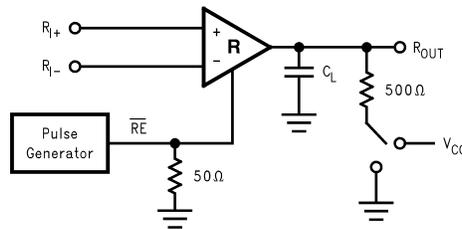


**Figure 8. Receiver TRI-STATE™ Delay Test Circuit**
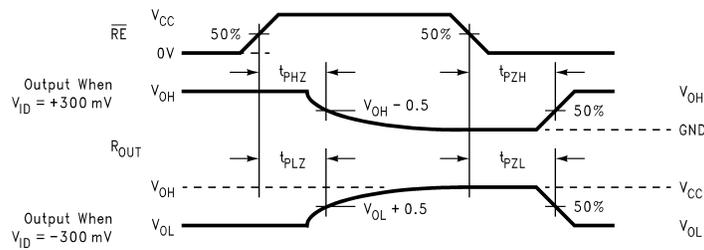


**Figure 9. Receiver TRI-STATE™ Delay Waveforms**

## Typical Bus Application Configurations
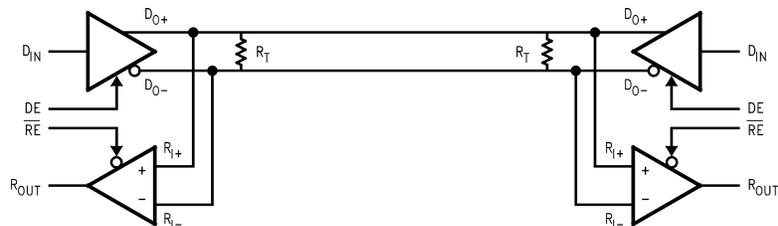


**Figure 10. Bidirectional Half-Duplex Point-to-Point Applications**

Product Folder Links: *DS92LV040A*
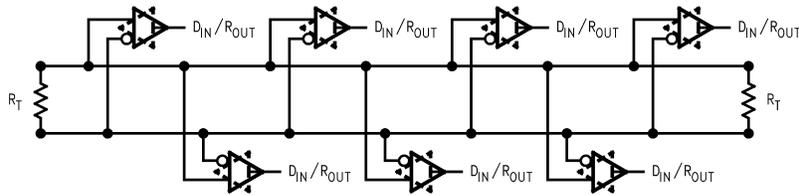
**Figure 11. Multi-Point Bus Applications**

## Connection Diagram
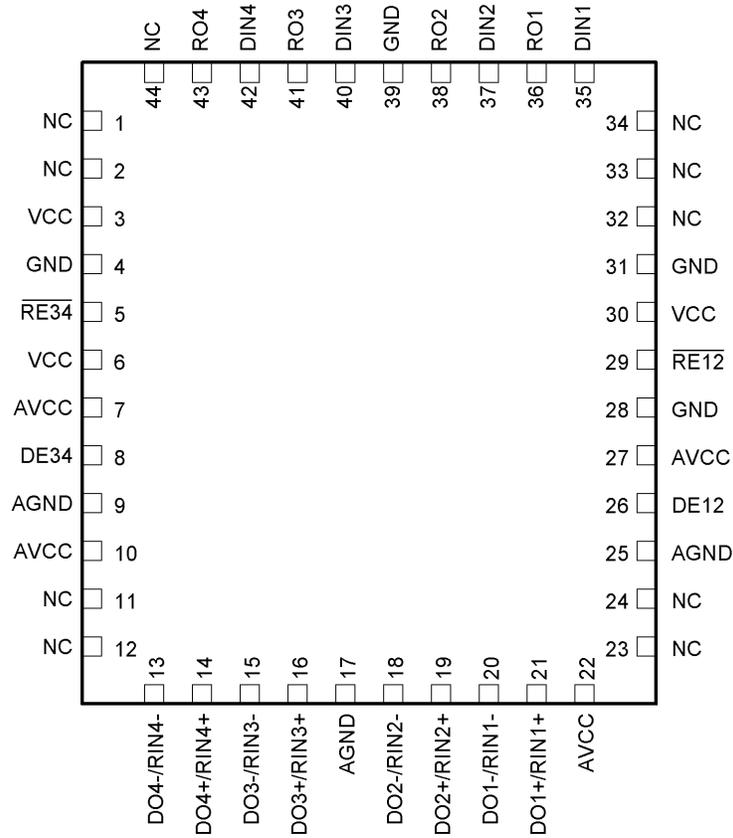


**Figure 12. Top View**
**See Package Number NJN0044A**

## Pinout Description

| Pin Name | Pin # | Input/Output | Descriptions |
|---|---|---|---|
| DO+/RI+ | 14, 16, 19, 21 | I/O | True Bus LVDS Driver Outputs and Receiver Inputs. |
| DO−/RI− | 13, 15, 18, 20 | I/O | Complimentary Bus LVDS Driver Outputs and Receiver Inputs. |
| $D_{IN}$ | 35, 37, 40, 42 | I | LVTTL Driver Input. No pull up or pull down is attached to this pin |
| RO | 36, 38, 41, 43 | O | LVTTL Receiver Output. |
| $\overline{RE12}$ | 29 | I | Receiver Enable LVTTL Input (Active Low). This pin, when low, configures receiver outputs, RO1 and RO2 active. When this pin is high, RO1 and RO2 are TRI-STATE. If this pin is floating, a weak current source to $V_{CC}$ causes RO1 and RO2 to be TRI-STATE |
| $\overline{RE34}$ | 5 | I | Receiver Enable LVTTL Input (Active Low). This pin, when low, configures receiver outputs, RO3 and RO4 active. When this pin is high, RO3 and RO4 are TRI-STATE. If this pin is floating, a weak current source to $V_{CC}$ causes RO3 and RO4 to be TRI-STATE |
| DE12 | 26 | I | Driver Enable LVTTL Input (Active High). This pin, when high, configures driver outputs, DO1+/RIN1+, DO1−/RIN1− and DO2+/RIN2+, DO2−/RIN2− active. When this pin is low, driver outputs 1 and 2 are TRI-STATE. If this pin is floating, a weak current source to $V_{CC}$ causes driver outputs 1 and 2 to be active |
| DE34 | 8 | I | Driver Enable LVTTL Input (Active High). This pin, when high, configures driver outputs, DO3+/RIN3+, DO3−/RIN3− and DO4+/RIN4+, DO4−/RIN4− active. When this pin is low, driver outputs 3 and 4 are TRI-STATE. If this pin is floating, a weak current source to $V_{CC}$ causes driver outputs 3 and 4 to be active |
| GND | 4, 28, 31, 39 | Ground | Ground for digital circuitry (must connect to GND on PC board). These pins connected internally. |
| $V_{CC}$ | 3, 6, 30 | Power | $V_{CC}$ for digital circuitry (must connect to $V_{CC}$ on PC board). These pins connected internally. |
| AGND | 9, 17, 25 | Ground | Ground for analog circuitry (must connect to GND on PC board). These pins connected internally. |
| $AV_{CC}$ | 7, 10, 22, 27 | Power | Analog $V_{CC}$ (must connect to $V_{CC}$ on PC board). These pins connected internally. |
| NC | 1, 2, 11, 12, 23, 24, 32, 33, 34, 44 | N/A | Reserved for future use, leave open circuit. |
| DAP | | GND | Must connect to GND plane through vias to achieve the theta ja specified under Absolute Maximum Ratings. The DAP (die attach pad) is the heat transfer material that is centered on the bottom of the WQFN package. Refer to application note AN-1187 for attachment details. |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DS92LV040ATLQA | ACTIVE | WQFN | NJN | 44 | 250 | TBD | Call TI | Call TI | -40 to 85 | LV040A | Samples |
| DS92LV040ATLQA/NOPB | ACTIVE | WQFN | NJN | 44 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | LV040A | Samples |
| DS92LV040ATLQAX | ACTIVE | WQFN | NJN | 44 | | TBD | Call TI | Call TI | -40 to 85 | LV040A | Samples |
| DS92LV040ATLQAX/NOPB | ACTIVE | WQFN | NJN | 44 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | LV040A | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** Only one of markings shown within the brackets will appear on the physical device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS92LV040ATLQA | WQFN | NJN | 44 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| DS92LV040ATLQA/NOPB | WQFN | NJN | 44 | 250 | 178.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |
| DS92LV040ATLQAX/NOPB | WQFN | NJN | 44 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.3 | 12.0 | 16.0 | Q1 |

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

**TAPE AND REEL BOX DIMENSIONS**
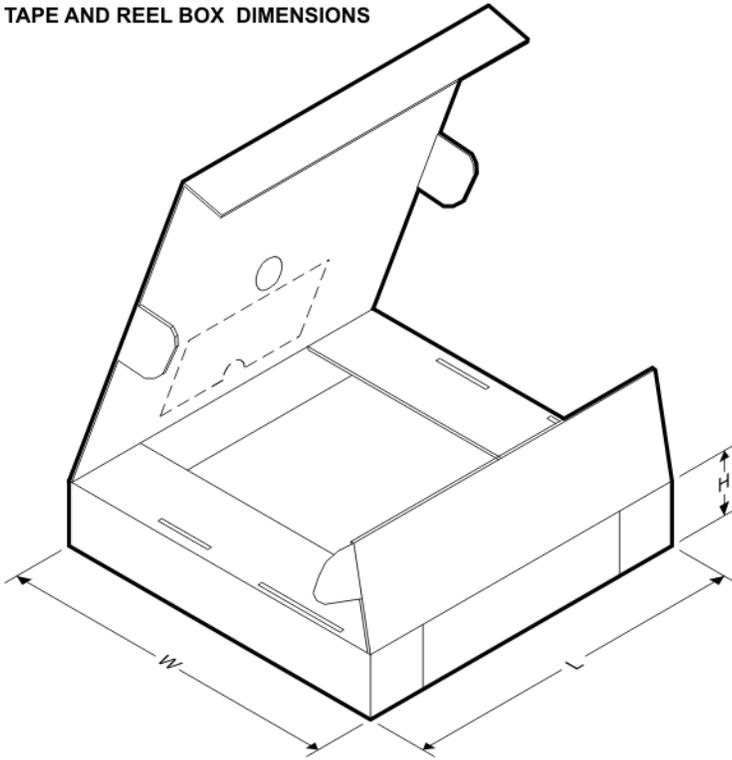


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| DS92LV040ATLQA | WQFN | NJN | 44 | 250 | 213.0 | 191.0 | 55.0 |
| DS92LV040ATLQA/NOPB | WQFN | NJN | 44 | 250 | 213.0 | 191.0 | 55.0 |
| DS92LV040ATLQAX/NOPB | WQFN | NJN | 44 | 2500 | 367.0 | 367.0 | 38.0 |

# NJN0044A



(44X 0.5)

(4.3)

(44X 0.25)

(5.8)

(4.3)

(40X 0.5)

(5.8)
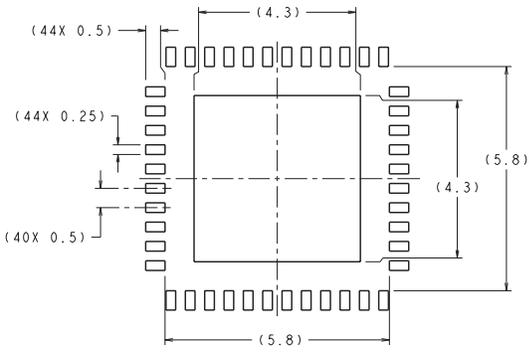
**RECOMMENDED LAND PATTERN**
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS

PIN 1 INDEX AREA

$\boxed{C}$

0.8 MAX

(0.2)

PIN 1 ID

4.3±0.1

0.1 MAX
ALL AROUND

1        12

44        13

2X $\boxed{4.5}$        4.3±0.1

7±0.1

35        22

$\boxed{B}$        7±0.1        $\boxed{A}$

34        23

44X 0.25±0.05        40X $\boxed{0.5}$        44X 0.5±0.1

$\boxed{\oplus}$ $\boxed{0.1 \text{M}}$ $\boxed{C}$ $\boxed{A\text{S}}$ $\boxed{B\text{S}}$

2X $\boxed{5.5}$

LQA44A (REV B)

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