



DS96F172C/DS96F172M/DS96F174C/DS96F174M EIA-485/EIA-422 Quad Differential Drivers

General Description

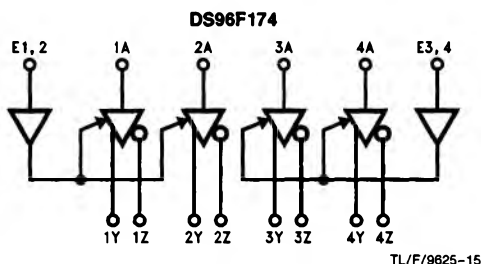
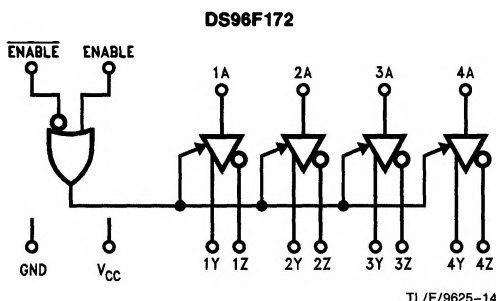
The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA-485 Standards. The DS96F172 and the DS96F174 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F172 and DS96F174 to operate at higher speeds while minimizing power consumption.

The DS96F172 and the DS96F174 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to -7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

Features

- Meets EIA-485 and EIA-422A standards
- Monotonic differential output switching
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: -7.0V to +12V
- Operates from single +5.0V supply
- Reduced power consumption
- Thermal shutdown protection
- DS96F172 and DS96F174 are lead and function compatible with the SN75172/174 or the AM26LS31/MC3487
- Military temperature range available
- Qualified for MIL-STD-883C
- Standard military drawings available (SMD)
- Available in DIP (J), LCC (E), and Flatpak (W) packages

Logic Diagrams



Function Tables (Each Driver)

DS96F172

Input	Enable		Outputs	
A	E	$\bar{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96F174

Input	Enable	Outputs	
A	E	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level

X = Don't Care
Z = High Impedance (Off)

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range (T_{STG})	-65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C	
Ceramic DIP (J)	1500 mW
Supply Voltage	7.0V
Enable Input Voltage	5.5V

*Derate "J" package 10 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F172C/DS96F174C	4.75	5.0	5.25	V
DS96F172M/DS96F174M	4.50	5.0	5.50	
Common Mode				
Output Voltage (V_{OC})	-7.0		+12.0	V
Output Current HIGH (I_{OH})			-60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)				
DS96F172C/DS96F174C	0		+70	°C
DS96F172M/DS96F174M	-55		+125	

Electrical Characteristics

Over recommended supply voltage and operating temperature range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			0.8	V
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			0.7	
V_{OH}	Output Voltage HIGH	$I_{OH} = -33\text{ mA}$ $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	3.0			V
V_{OL}	Output Voltage LOW	$I_{OL} = 33\text{ mA}$ $T_A = 0^\circ\text{C to } +70^\circ\text{C}$			2.0	V
V_{IC}	Input Clamp Voltage	$I_I = -18\text{ mA}$			-1.5	V
$ V_{OD1} $	Differential Output Voltage	$I_O = 0\text{ mA}$			6.0	V
$ V_{OD2} $	Differential Output Voltage	$R_L = 54\Omega$, Figure 1 $T_A = -55^\circ\text{C}$	1.2	2.0		V
			1.5			
		$R_L = 100\Omega$, Figure 1	2.0	2.3		
V_{OD}	Differential Output Voltage	Figure 1a $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	1.0			V
$\Delta V_{OD} $	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω , Figure 1 $-40^\circ\text{C to } +125^\circ\text{C}$			± 0.2	V
		$-55^\circ\text{C to } +125^\circ\text{C}$			± 0.4	V
V_{OC}	Common Mode Output Voltage (Note 5)	$R_L = 54\Omega$ or 100Ω , Figure 1			3.0	V
$\Delta V_{OC} $	Change in Magnitude of Common Mode Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω , Figure 1			± 0.2	V
I_O	Output Current with Power Off	$V_{CC} = 0V$, $V_O = -7.0V$ to $+12V$			± 50	μA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0V$ to $+12V$		± 20	± 50	μA
I_{IH}	Input Current HIGH	$V_I = 2.4V$			20	μA
I_{IL}	Input Current LOW	$V_I = 0.4V$			-50	μA
I_{OS}	Short Circuit Output Current (Note 6)	$V_O = -7.0V$			-250	mA
		$V_O = 0V$			-150	
		$V_O = V_{CC}$			150	
		$V_O = +12V$			250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled		50	mA
I_{CCX}			Outputs Disabled		30	

COMMERCIAL**Switching Characteristics** $V_{CC} = 5.0V$, $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, <i>Figure 2</i>		15	20	ns
t_{TD}	Differential Output Transition Time			15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, <i>Figure 3</i>		12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	16	ns
t_{ZH}	Output Enable Time to High Level	$R_L = 110\Omega$, <i>Figure 4</i>		25	32	ns
t_{ZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, <i>Figure 5</i>		25	32	ns
t_{HZ}	Output Disable Time from High Level	$R_L = 110\Omega$, <i>Figure 4</i>		25	30	ns
t_{LZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, <i>Figure 5</i>		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND (Note 7)	<i>Figure 5</i>		300		ns
t_{SKEW}	Driver Output to Output	$R_L = 60\Omega$		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the $-55^\circ C$ to $+125^\circ C$ temperature range for the DS96F172M/DS96F174M and across the $0^\circ C$ to $+70^\circ C$ range for the DS96F172C/DS96F174C. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA-422A and EIA-485 standards, V_{OC} , which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS} .

Note 6: Only one output at a time should be shorted.

Note 7: For more information see Application Bulletin, contact Product Marketing.

Order Number: DS96F172CJ
DS96F172CN
DS96F172MJ
DS96F174CJ
DS96F174MJ
NS Package Number J16A or N16A

MIL-STD-883C**Absolute Maximum Ratings** (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range (T_{STG})	-65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C	
Ceramic LCC (E)	2000 mW
Ceramic DIP (J)	1800 mW
Ceramic Flatpak (W)	1000 mW

Supply Voltage 7.0V

Enable Input Voltage 5.5V

*Above $T_A = 25^\circ\text{C}$, derate "E" package 13.4, "J" package 12.5, "W" package 7.1 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F172M/DS96F174M	4.50	5.0	5.50	V
Common Mode				
Output Voltage (V_{OC})	-7.0		+12.0	V
Output Current HIGH (I_{OH})			-60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)				
DS96F172M/DS96F174M	-55		+125	

Electrical Characteristics

Over recommended supply voltage and operating temperature range unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input Voltage HIGH		2.0		V
V_{IL}	Input Voltage LOW	$T_A = 25^\circ\text{C}$		0.8	V
		$T_A = -55^\circ\text{C}$, or $+125^\circ\text{C}$		0.7	V
V_{IC}	Input Clamp Voltage	$I_I = -18\text{ mA}$		-1.5	V
$ V_{OD1} $	Differential Output Voltage	$I_O = 0\text{ mA}$		6.0	V
$ V_{OD2} $	Differential Output Voltage	$R_L = 54\Omega$, $V_{CC} = 4.5\text{V}$ <i>Figure 1</i>	$T_A = -55^\circ\text{C}$ 1.2		V
			$T_A = 25^\circ\text{C}$, or $+125^\circ\text{C}$ 1.5		
		$R_L = 100\Omega$, $V_{CC} = 4.5\text{V}$, <i>Figure 1</i>	2.0		
$\Delta V_{OD} $	Change in Magnitude of Differential Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω , $V_{CC} = 4.5\text{V}$, <i>Figure 1</i>	$T_A = 25^\circ\text{C}$, or $+125^\circ\text{C}$ ±0.2		V
			-55°C ±0.4		V
V_{OC}	Common Mode Output Voltage (Note 5)	$R_L = 54\Omega$ or 100Ω , <i>Figure 1</i>		3.0	V
$\Delta V_{OC} $	Change in Magnitude of Common Mode Output Voltage (Note 4)	$R_L = 54\Omega$ or 100Ω , $V_{CC} = 4.5\text{V}$, <i>Figure 1</i>		±0.2	V
I_O	Output Current with Power Off	$V_{CC} = 0\text{V}$, $V_O = -7.0\text{V}$ to $+12\text{V}$		±50	μA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0\text{V}$ to $+12\text{V}$		±50	μA
I_{IH}	Input Current HIGH	$V_I = 2.4\text{V}$		20	μA
I_{IL}	Input Current LOW	$V_I = 0.4\text{V}$		-50	μA
I_{OS}	Short Circuit Output Current (Note 6)	$V_O = -7.0\text{V}$		-250	mA
		$V_O = 0\text{V}$		-150	
		$V_O = V_{CC}$		150	
		$V_O = +12\text{V}$		250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled	50	mA
I_{CCX}			Outputs Disabled	30	

MIL-STD-883C**Switching Characteristics** $V_{CC} = 5.0V$

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		$T_A = 55^\circ C$	$T_A = 125^\circ C$	Units
			Typ	Max	Max	Max	
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, $C_L = 15\text{ pF}$, <i>Figure 2</i>	15	22	30	30	ns
t_{TD}	Differential Output Transition Time		15	22	40	40	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, $C_L = 15\text{ pF}$, <i>Figure 3</i>	12	16	25	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		12	16	25	25	ns
t_{ZH}	Output Enable Time to High Level	$R_L = 110\Omega$, <i>Figure 4</i>	25	32	40	40	ns
t_{ZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, <i>Figure 5</i>	25	35	100	100	ns
t_{HZ}	Output Disable Time from High Level	$R_L = 110\Omega$, <i>Figure 4</i> , Note 13	25	30	80	80	ns
t_{LZ}	Output Disable Time from Low Level		20	25	40	40	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND (Note 12)	<i>Figure 5</i>	300				ns
t_{SKEW}	Driver Output to Output	$R_L = 60\Omega$	1.0	4.0	10	10	ns

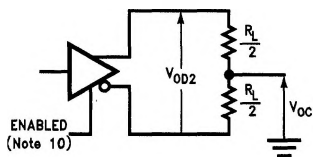
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DS96F172ME/883 5962-9076501M2A

DS96F174MJ/883 5962-9076502MEA
DS96F174MW/883 5962-9076502MFA
DS96F174ME/883 5962-9076502M2A

Order Number: DS96F172MJ/883, DS96F174MJ/883
NS Package Number J16A
DS96F172ME/883, DS96F174ME/883
NS Package Number E20A
DS96F172MW-MIL, DS96F174MW/883
NS Package Number W16A

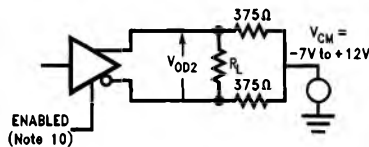
For Complete Military 883 Specifications, see RETS Data Sheet.

Parameter Measurement Information



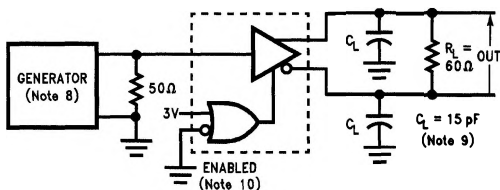
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FIGURE 1. Differential and Common Mode Output Voltage



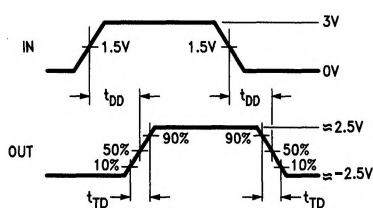
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FIGURE 1a. Differential Output Voltage with Varying Common Mode Voltage

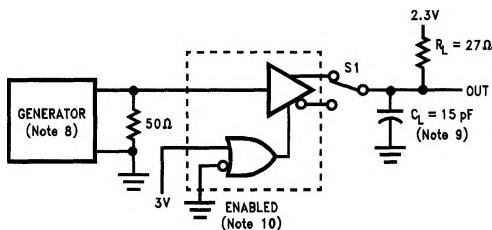


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FIGURE 2. Differential Output Delay and Transition Times

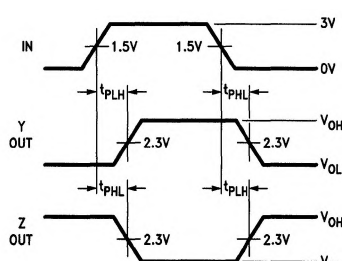


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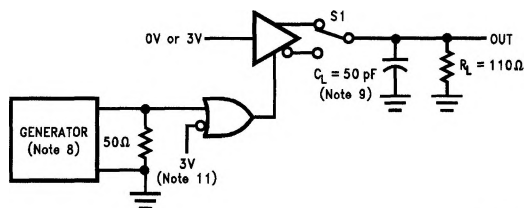


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FIGURE 3. Propagation Delay Times

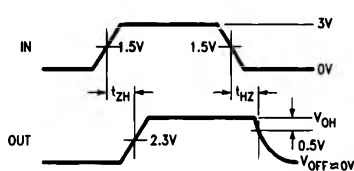


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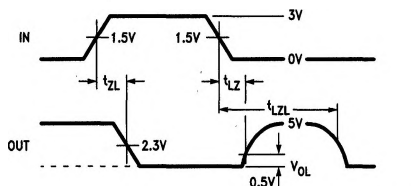
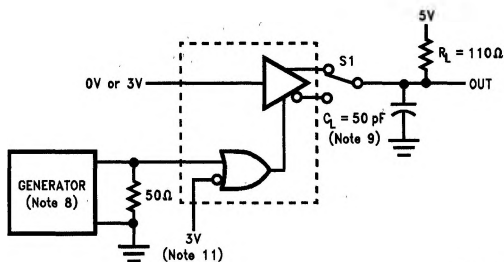
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FIGURE 4. t_{ZH} and t_{HZ}



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Parameter Measurement Information (Continued)



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TL/F/9625-10

FIGURE 5. t_{ZL} , t_{LZ} , t_{LZL}

Note 8: The input pulse is supplied by a generator having the following characteristics: $f = 1.0$ MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $Z_0 = 50\Omega$.

Note 9: C_L includes probe and jig capacitance.

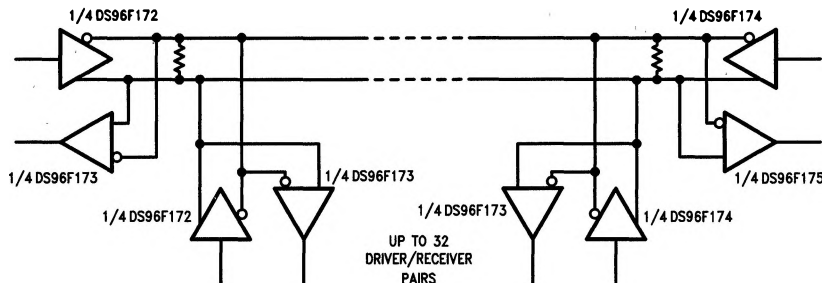
Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Note 11: To test the active low Enable $\bar{E}$ of DS96F172 ground $\bar{E}$ and apply an inverted waveform to $\bar{E}$. DS96F174 has active high Enable only.

Note 12: For more information see Application Bulletin, Contact Product Marketing.

Note 13: Not tested for DS96F172MW-MIL device.

Typical Application



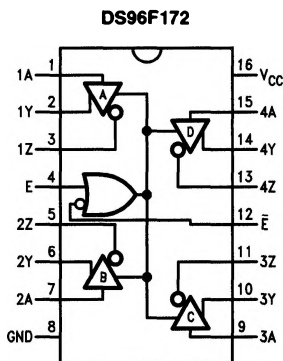
Note:

The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

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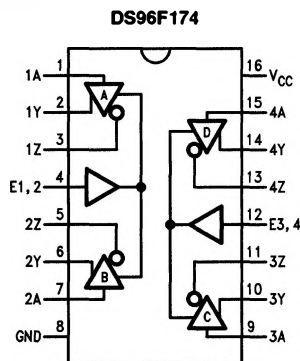
Connection Diagrams

16-Lead Ceramic Dual-In-Line Package NS Package Number J16A



Top View

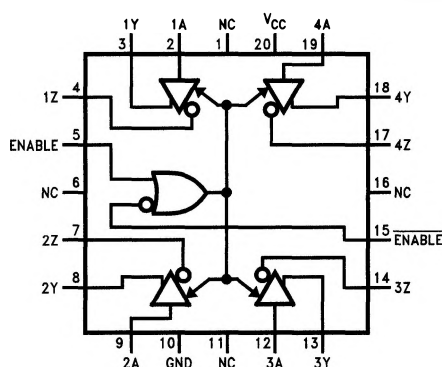
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Top View

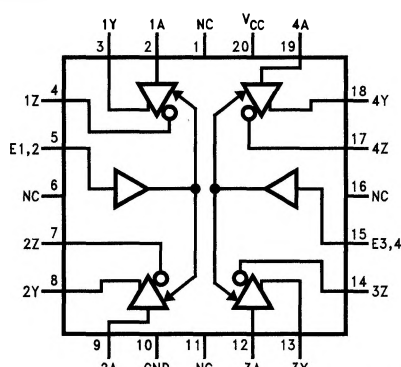
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20-Lead Ceramic Leadless Chip Carrier NS Package Number E20A



Top View

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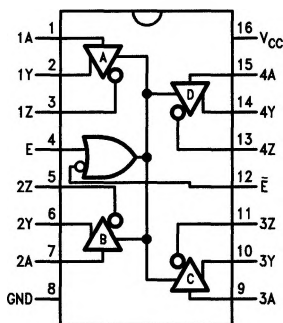


Top View

TL/F/9625-19

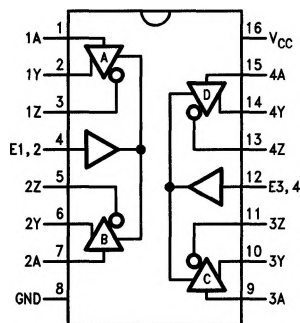
NC = No connection

16-Lead Ceramic Flatpak NS Package Number W16A



Top View

TL/F/9625-1



Top View

TL/F/9625-2

Order Numbers are located at the end of the respective Electrical Tables.