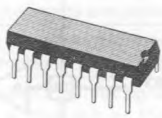
SGS-THOMSON MICROELECTRONICS

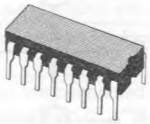
EF73321

PCM LINE TRANSCEIVER

- NMOS TECHNOLOGY
- OPERATES FROM + 5 V SUPPLY
- DIGITAL TECHNOLOGY THROUGHOUT
- EXTRACTS DISTANT CLOCK TRANSMITTED BY A PCM TRUNK
- CAN HANDLE PEAK TO PEAK JITTER AMPLITUDE UP TO 0.25 BIT FOR AN 8-BIT PERIOD
- INTEGRATED TRANSMIT AND RECEIVE AMPLIFIERS
- TTL-COMPATIBLE INPUT/OUTPUT



DIP16
Plastic



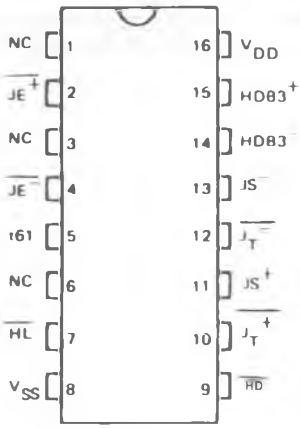
DIP16
Ceramic

ORDER CODE : EF73321P
EF73321C

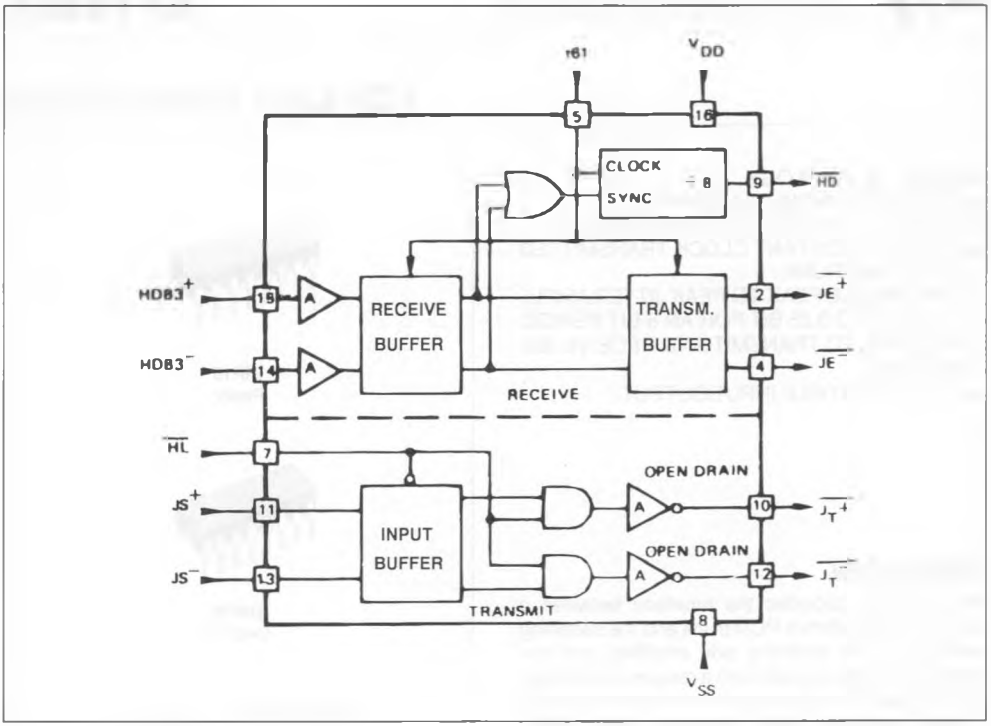
DESCRIPTION

The EF73321 provides the interface between a 2.048 or 1.544 Mbits/s PCM trunk and the switching equipment. The receiving side amplifies and reshapes the bipolar signals from a receive transformer and extracts from the signals the distant clock HD. On the transmitting side it calibrates pulses in terms of duration and amplitude by means of transistor circuits directly coupled to a transmit transformer.

PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

POWER SUPPLY

N°	Name	Type	Function	Description
8	V_{SS}	S	Supply	Ground
16	V_{DD}	S		+ 5 V ± 5 %

RECEIVE

N°	Name	Type	Function	Description
5	t61	I	–	16384 kHz or 12352 kHz Clock. Synchronises outputs $\overline{JE}$+; $\overline{JE}$– and $\overline{HD}$.
15 14	HDB3+ HDB3–	I I	Data Input	Bipolar signals in HDB3 code received from the receive transformer. The amplitude of these signals is between – 5 V and + 5 V. Each positive pulse on HDB3+ (HDB3–) resynchronises the circuit clock and is reconstituted in calibrated form on output $\overline{JE}$+ ($\overline{JE}$–). Negative pulses have no effect on the circuit as the inputs are protected.
2 4	$\overline{JE}$+ $\overline{JE}$–	O O	Data Output	Received HDB3 signals are resynchronised with $\overline{HD}$ and calibrated in terms of amplitude (TTLLS compatible levels).
9	$\overline{HD}$	O	Distant Clock Output	The distant clock recovered from the signal on HDB3+, HBD3–. The nominal frequency is 2048 kHz or 1544 kHz in the absence of jitter.

TRANSMIT

N°	Name	Type	Function	Description
7	$\overline{HL}$	I	Clock	Local clock, nominal frequency 2048 kHz or 1544 kHz.
11 13	JS+ JS–	I I	Data Input	The data is recognised on the falling edge of $\overline{HL}$.
10 12	$\overline{JT}$+ $\overline{JT}$–	O O	Data Output	These open drain outputs are connected to the windings of the transmit transformer. Recognition of a "1" on $\overline{JS}$+ ($\overline{JS}$–) grounds the winding of the transformer connected to $\overline{JT}$+ ($\overline{JT}$–) for the duration of "1" level of HL. These outputs are protected against short-circuits by current limiting internal to the circuit.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	$-0.3\ V \leq V_{DD} \leq 7\ V$	V
V_I	Input Voltage Range (except inputs HDB3 + and HBD3 –)	$-0.3\ V \leq V_I \leq V_{DD} + 0.3\ V$	V
P	Maximum Power	P_{max} = 250 mW in 0 °C to 70 °C Range	mW
T_{stg}	Storage Temperature Range	– 55 °C to + 150 °C	°C

FUNCTIONAL DESCRIPTION

RECEIVE PATH

The PCM Line Transceiver receives directly from the receive transformer on inputs HDB3 + and HDB3– data in HDB3 code. It synchronizes this data by means of the clock on input t61 and converts it to voltage pulses of calibrated duration on outputs $\overline{JE}$+ and $\overline{JE}$– . To be recognized correctly by this circuit the received data must satisfy minimum and maximum duration conditions (Refer to timing diagrams).

Distant clock $\overline{HD}$ is provided by a counter which divides by 8 the frequency of the clock t61. This counter is resynchronized with the data of the PCM trunk on each positive-going edge at HDB3 + or HDB3–. The period of $\overline{HD}$ may vary by 0.25 bit within a period of 8 bits without degradation of the phase relationships between $\overline{JE}$+, $\overline{JE}$– and $\overline{HD}$ (Cf. fig.1). If the variation occurs in an interval exceeding 4 bits but less than 8 bits the phase relationships between $\overline{JE}$+, $\overline{JE}$– and $\overline{HD}$ are modified (Cf. fig. 2 and fig. 3).

In all cases outputs $\overline{JE}$+ and $\overline{JE}$– remain stable on either side of the falling edge of HL so as to be sampled correctly by the EF7333.

TRANSMIT PATH

The signals JS+ and JS– to transmit are sampled on the falling edge of clock signal HL and calibrated by the duration for which this signal is high.

Open drain outputs $\overline{JT}$+ and $\overline{JT}$– drive the primary windings of the transmit transformer directly. They are protected against overcurrents occurring should the secondary windings of this transformer be short-circuited, in which case the primary behaves as a very low resistance connecting the output to supply rail V_{DD}.

RECEIVE TIMING DIAGRAM

Figure 1 : External Signals with Jitter < 0.25 Bit within 8-Bit Period.

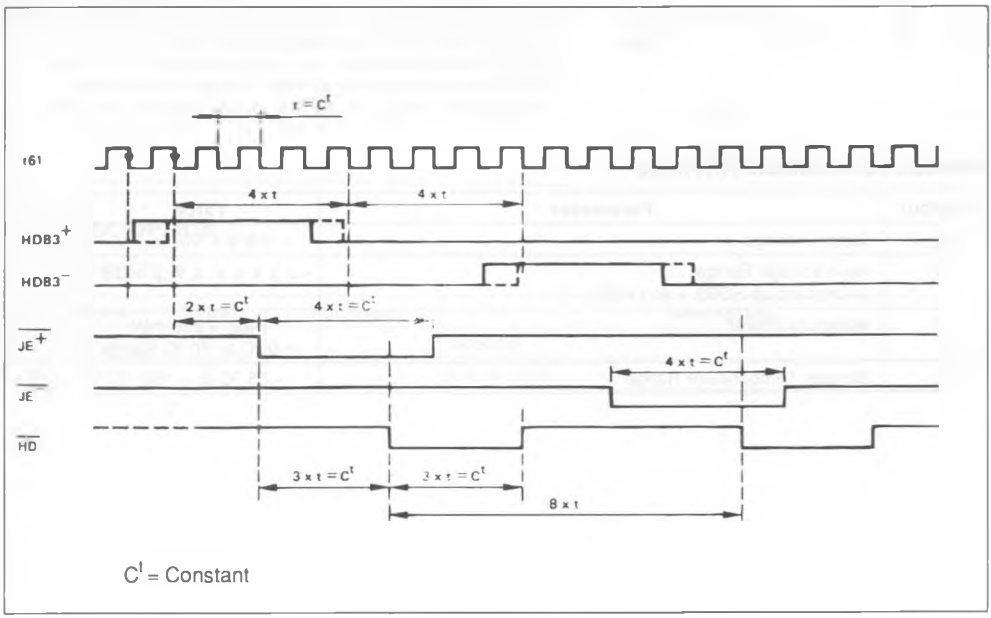


Figure 2 : External Signals with HDB3^{-} and HDB3^{-} Signal Period 6 x t.

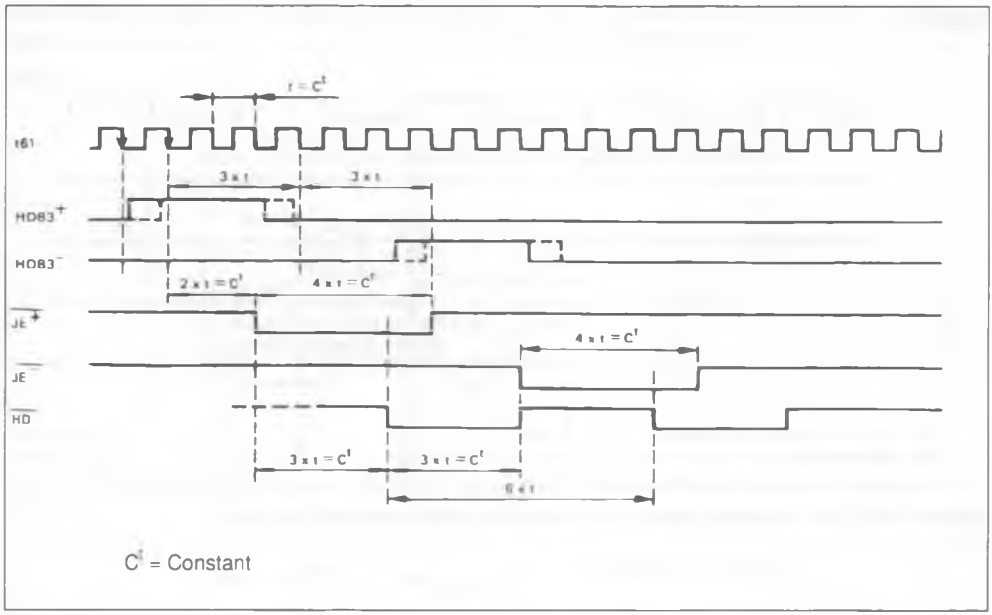
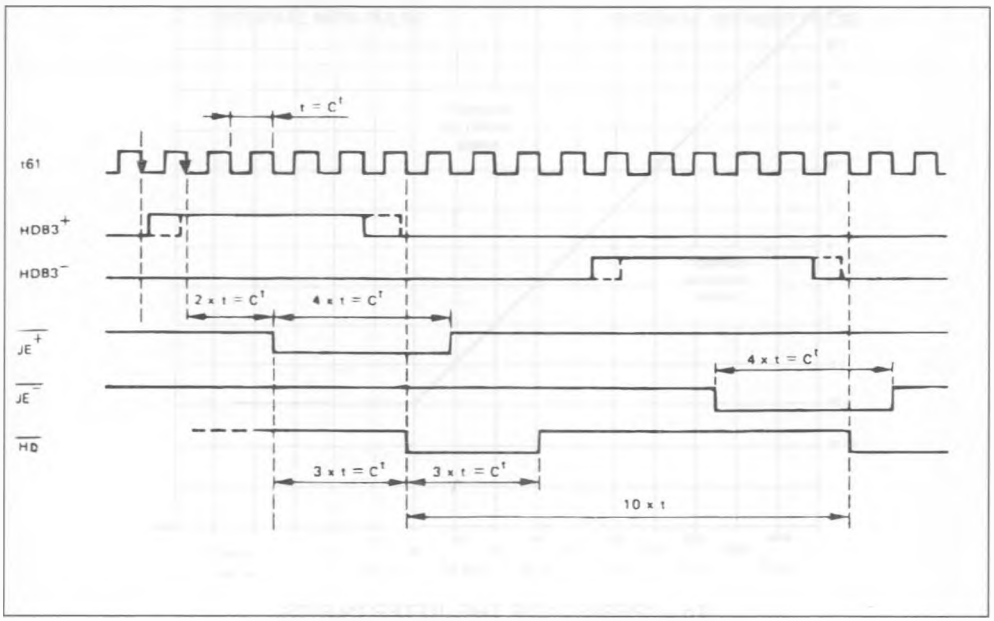


Figure 3 : External Signals with HDB3^{+} and HDB3^{-} Signal Period 10 x t.



TRANSMIT

Figure 4 .

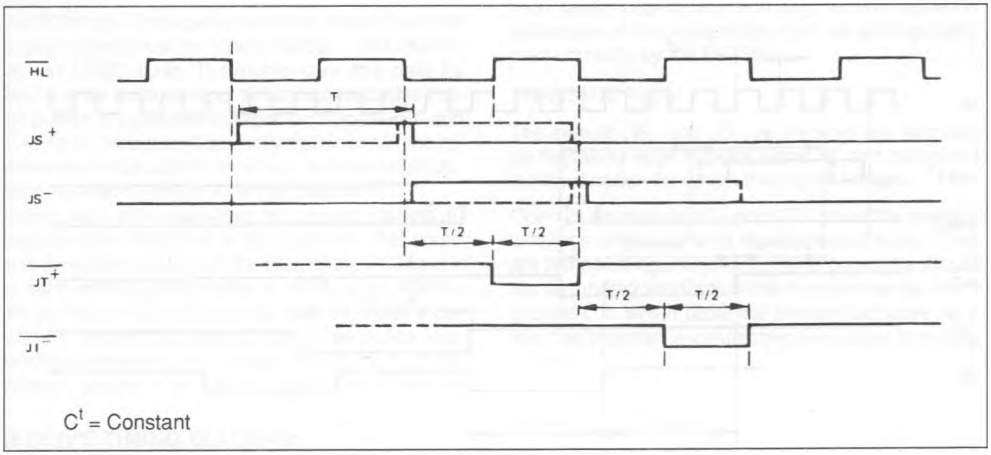
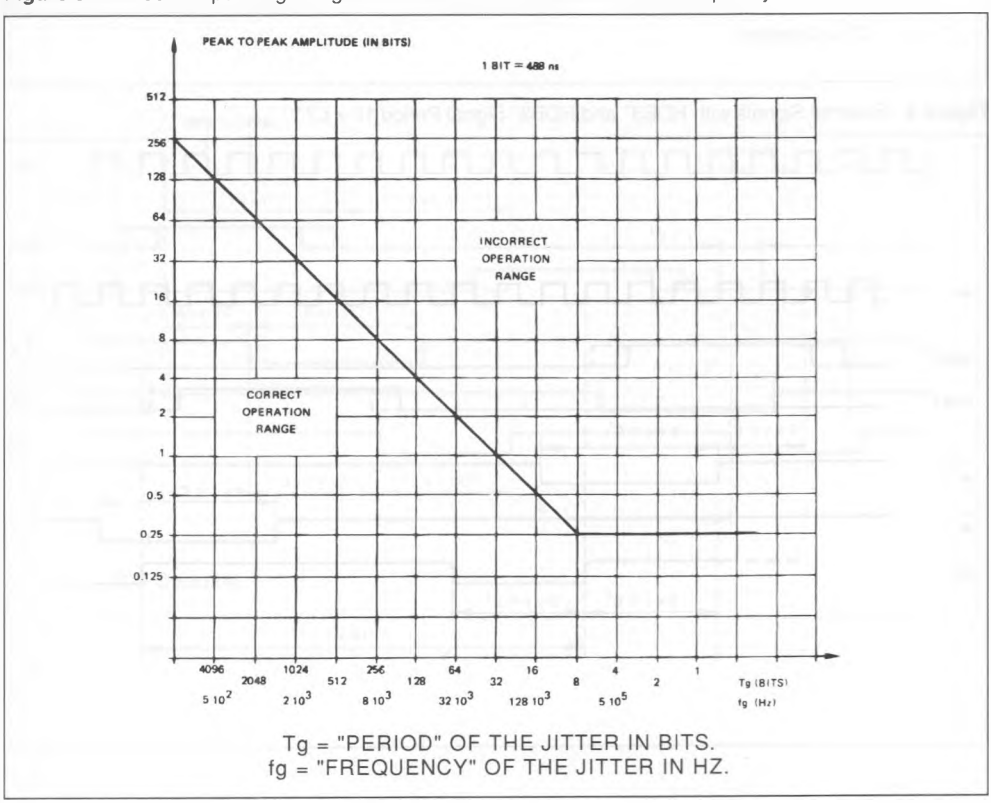


Figure 5 : EF73321 Operating Range as a Function of Jitter Period and Frequency.

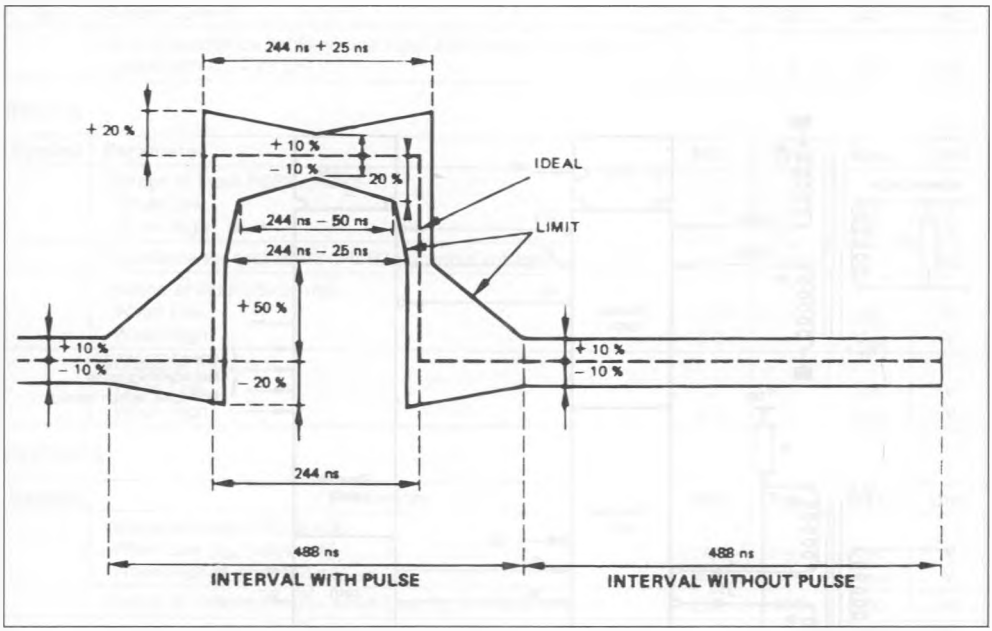


TRANSMIT PATH

Pulse limiting curves for 2 048 kbit/s CEPT PCM trunk.

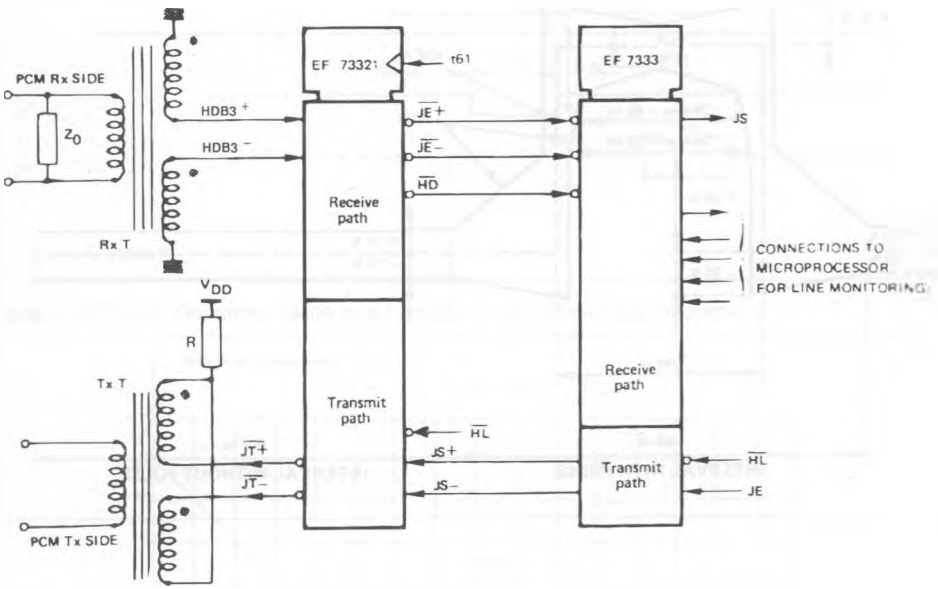
The limiting curves below are for a resistive load of 120 Ω connected across the secondary winding of the transmit transformer.

Figure 6 .



TYPICAL APPLICATION

Using EF7333 and EF73321 in a 2048 kHz PCM line
for Data transmission/reception and frame monitoring.



t61 : 16384 Khz CLOCK

Rx T : LINE RECEIVE TRANSFORMER

Tx T : LINE TRANSMIT TRANSFORMER

$\overline{HL}$: LOCAL 2048 Khz CLOCK

Note : EF73321 layout considerations : for correct operation of transmission drivers a 100 nF decoupling capacitor must be connected between V_{DD} and V_{SS} and located as close as possible to the supply pins.

STATIC ELECTRICAL CHARACTERISTICS

Ambient Temperature Range : 0 °C to + 70 °C - Typical Values at + 25 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Positive Power Supply	4.75	5	5.25	V
I_{DD}	Supply Current	–	20	40	mA
	Stray Capacitance between one Input and Ground (outputs loaded with C_L = 25 pF)	–	5	10	pF

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Voltage at Input HDB3+/HDB3– When Low When High	 – 5 2.2	 — –	 0.6 5	 V V
	Resistance at Input HDB3+/HDB3– (inverse voltage V_I = – 5 V)	—	10	—	kΩ
	Voltage at input JS+/JS–/$\overline{HL}$ When Low When High	 – 0.3 2.2	 — —	 0.6 V_{DD}	 V V
	Voltage at Input t61 When Low When High	 0 2.6	 — —	 0.6 V_{DD}	 V V

OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Voltage at Output $\overline{HD}$/$\overline{JE}$+/$\overline{JE}$– When Low (I_{OL} = 0.4 mA) When High (I_{OH} = – 40 µA)	 0 2.6	 — —	 0.4 V_{DD}	 V V
	Voltage at Output $\overline{JT}$+/$\overline{JT}$– when Low (R_L = 175 Ω to V_{DD})	250	450	750	mV
	Current at Output $\overline{JT}$+/$\overline{JT}$– when High Impedance (V_{OH} = 12 V)	—	—	100	µA
	Current at Output $\overline{JT}$+/$\overline{JT}$– (output current protection)	—	—	35	mA

DYNAMIC CHARACTERISTICS

Typical values at + 25 °C (0 °C < T_A < + 70 °C).

CLOCKS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Clock t61 (fig.8)	— —	12352 16384	— 16500	kHz kHz
t_{PL}	when Low	20	—	—	ns
t_{PH}	when High	20	—	—	ns
	Clock $\overline{HL}$ (fig. 10)	— —	1544 2048	— 2200	kHz kHz
t_{THL}	Fall Time	—	—	30	ns
t_{TLH}	Rise Time	—	—	30	ns

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Inputs HDB3+/HDB3– (fig. 9)				
t_H	Min. Pulse Duration	t			ns
t_L	Max. Pulse Duration			4 x t	ns
	Inputs JS+/JS– (fig. 10)				
$t_{set\text{-}up}$	Set up Time	20			ns
t_{hold}	Hold Time	30			ns

OUTPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Outputs $\overline{JE}$+/$\overline{JE}$– Relative to $\overline{Hd}$ (CL = 25 pF, fig. 11)				
$t_{set\text{-}up}$	Set up Time	150	3 x t		ns
t_{hold}	Hold Time	30	t		ns
t_{THL}	Fall Time		15		ns
t_{TLH}	Rise Time		20		ns
	Outputs $\overline{JT}$+/$\overline{JT}$– (R_L = 175 Ω = to V_{DD}, fig. 12)				
t_{WM}	Pulse Duration (C_L = 25 pF)	219	244	269	ns
	$\overline{HL}$ = 2048 kHz				

Figure 8.

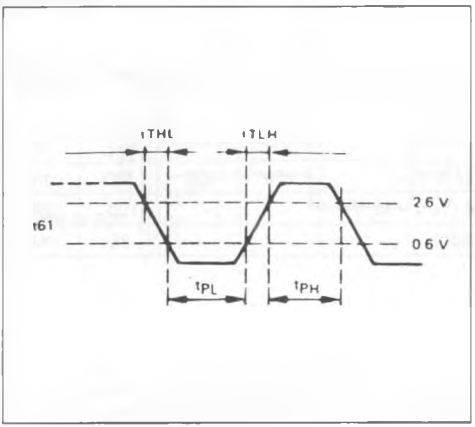


Figure 9.

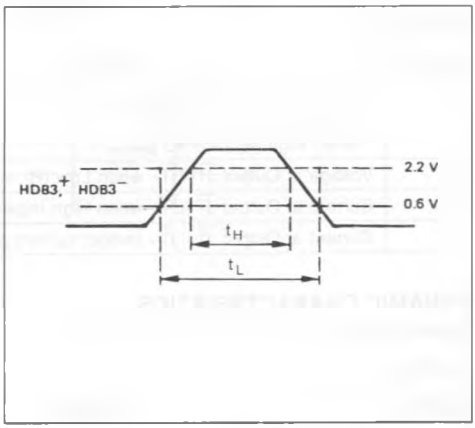


Figure 10.

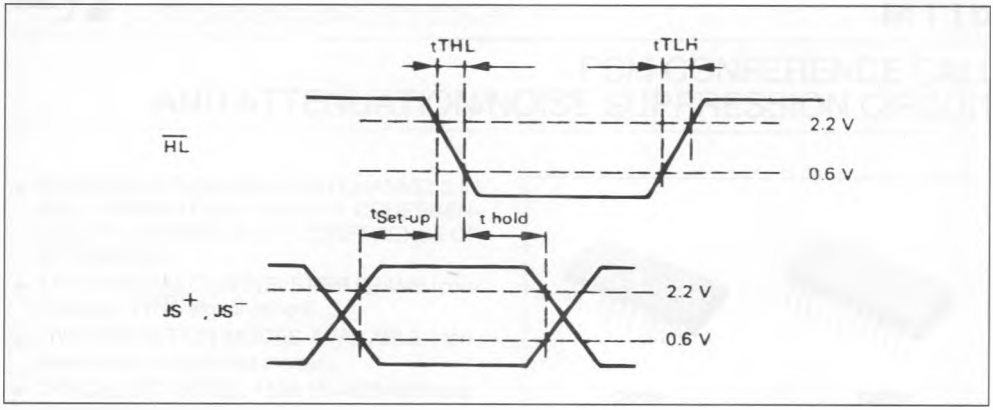


Figure 11.

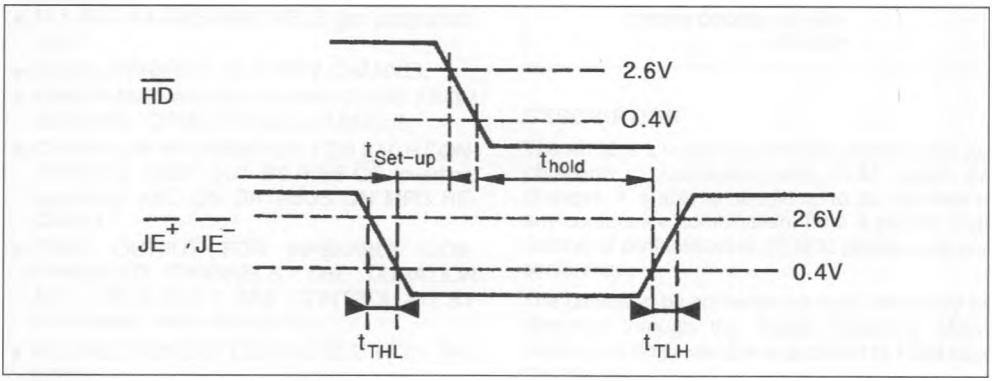


Figure 12.