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FAIRCHILD SEMICONDUCTOR®

February 2014

# FAN4860
# 3 MHz, Synchronous TinyBoost™ Regulator

## Features

- Operates with Few External Components: 1 µH Inductor and 0402 Case Size Input and Output Capacitors
- Input Voltage Range from 2.3 V to 5.4 V
- Fixed 3.3 V, 5.0 V, or 5.4 V Output Voltage Options
- Maximum Load Current >150 mA at $V_{IN}$=2.3 V
- Maximum Load Current 300 mA at $V_{IN}$=3.3 V, $V_{OUT}$=5.4 V
- Maximum Load Current 300 mA at $V_{IN}$=3.3 V, $V_{OUT}$=5.0 V
- Maximum Load Current 300 mA at $V_{IN}$=2.7 V, $V_{OUT}$=3.3 V
- Up to 92% Efficient
- Low Operating Quiescent Current
- True Load Disconnect During Shutdown
- Variable On-time Pulse Frequency Modulation (PFM) with Light-Load Power-Saving Mode
- Internal Synchronous Rectifier (No External Diode Needed)
- Thermal Shutdown and Overload Protection
- 6-Pin 2 x 2 mm UMLP
- 6-Bump WLCSP, 0.4 mm Pitch

## Applications

- USB “On the Go” 5 V Supply
- 5 V Supply – HDMI, H-Bridge Motor Drivers
- Powering 3.3 V Core Rails
- PDAs, Portable Media Players
- Cell Phones, Smart Phones, Portable Instruments

## Description

The FAN4860 is a low-power boost regulator designed to provide a regulated 3.3 V, 5.0 V or 5.4 V output from a single cell Lithium or Li-Ion battery. Output voltage options are fixed at 3.3 V, 5.0 V, or 5.4 V with a guaranteed maximum load current of 200 mA at $V_{IN}$=2.3 V and 300 mA at $V_{IN}$=3.3 V. Input current in Shutdown Mode is less than 1 µA, which maximizes battery life.

Light-load PFM operation is automatic and “glitch-free”. The regulator maintains output regulation at no-load with as low as 37 µA quiescent current.

The combination of built-in power transistors, synchronous rectification, and low supply current make the FAN4860 ideal for battery powered applications.

The FAN4860 is available in 6-bump 0.4 mm pitch Wafer-Level Chip Scale Package (WLCSP) and a 6-lead 2x2 mm ultra-thin MLP package.

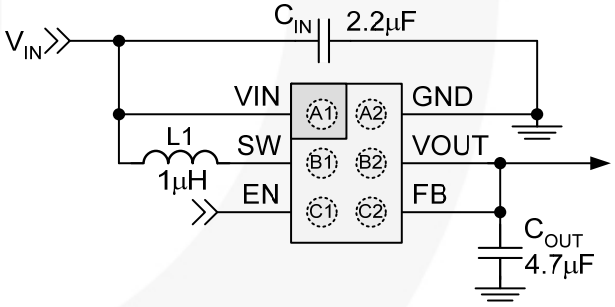



**Figure 1. Typical Application**

## Ordering Information

| Part Number | Operating Temperature Range | Package | Packing Method |
|---|---|---|---|
| FAN4860UC5X | -40°C to 85°C | WLCSP, 0.4 mm Pitch | Tape and Reel |
| FAN4860UMP5X | -40°C to 85°C | UMLP-6, 2 x 2 mm | Tape and Reel |
| FAN4860UC33X | -40°C to 85°C | WLCSP, 0.4 mm Pitch | Tape and Reel |
| FAN4860UC54X | -40°C to 85°C | WLCSP, 0.4 mm Pitch | Tape and Reel |

## Block Diagrams

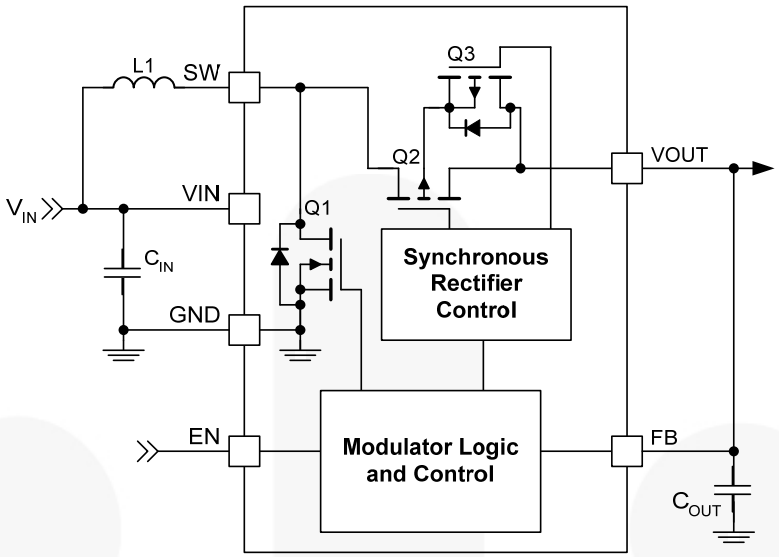



**Figure 2. IC Block Diagram**

## Pin Configurations

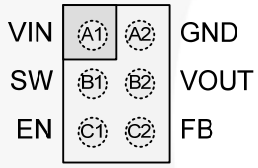



**Figure 3. WLCSP (Top View)**

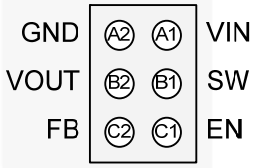



**Figure 4. WLCSP (Bottom View)**

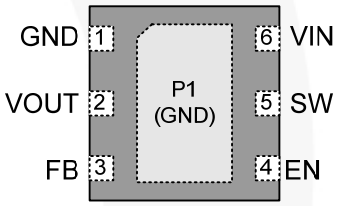



**Figure 5. 2x2 mm UMLP (Top View)**

## Pin Definitions

| Pin # | | Name | Description |
|---|---|---|---|
| WLCSP | UMLP | | |
| A1 | 6 | VIN | **Input Voltage**. Connect to Li-Ion battery input power source and input capacitor ($C_{IN}$). |
| B1 | 5 | SW | **Switching Node**. Connect to inductor. |
| C1 | 4 | EN | **Enable**. When this pin is HIGH, the circuit is enabled. This pin should not be left floating. |
| C2 | 3 | FB | **Feedback**. Output voltage sense point for $V_{OUT}$. Connect to output capacitor ($C_{OUT}$). |
| B2 | 2 | VOUT | **Output Voltage**. This pin is both the output voltage terminal as well as an IC bias supply. |
| A2 | 1, P1 | GND | **Ground**. Power and signal ground reference for the IC. All voltages are measured with respect to this pin. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{IN}$ | VIN Pin | | -0.3 | 5.5 | V |
| $V_{OUT}$ | VOUT Pin | | –2 | 6 | V |
| $V_{FB}$ | FB Pin | | –2 | 6 | V |
| $V_{SW}$ | SW Node | DC | -0.3 | 5.5 | V |
| | | Transient: 10 ns, 3 MHz | -1.0 | 6.5 | |
| $V_{EN}$ | EN Pin | | -0.3 | 5.5 | V |
| ESD | Electrostatic Discharge Protection Level | Human Body Model per JESD22-A114 | 2 | | kV |
| | | Charged Device Model per JESD22-C101 | 1 | | |
| $T_J$ | Junction Temperature | | –40 | +150 | °C |
| $T_{STG}$ | Storage Temperature | | –65 | +150 | °C |
| $T_L$ | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage | 5.4 $V_{OUT}$ | 2.3 | 4.5 | V |
| | | 5.0 $V_{OUT}$ | 2.3 | 4.5 | |
| | | 3.3 $V_{OUT}$ | 2.3 | 3.2 | |
| $I_{OUT}$ | Output Current | | | 200 | mA |
| $T_A$ | Ambient Temperature | | –40 | +85 | °C |
| $T_J$ | Junction Temperature | | –40 | +125 | °C |

## Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate $T_A$.

| Symbol | Parameter | | Typical | Units |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance | WLCSP | 130 | °C/W |
| | | UMLP | 57 | °C/W |

## Electrical Specifications

Minimum and maximum values are at $V_{IN}$=$V_{EN}$=2.3 V to 4.5 V (2.5 to 3.2 $V_{IN}$ for 3.3 $V_{OUT}$ option), $T_A$=-40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at $T_A$=25°C, $V_{IN}$=$V_{EN}$=3.6 V for $V_{OUT}$=5.0 V / 5.4 V, and $V_{IN}$=$V_{EN}$=2.7 V for $V_{OUT}$=3.3 V.

| Symbol | Parameter | | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{IN}$ | $V_{IN}$ Input Current | 5.4 $V_{OUT}$ | Quiescent: $V_{IN}$=3.6 V, $I_{OUT}$=0, EN=$V_{IN}$ | | 37 | 45 | µA |
| | | | Shutdown: EN=0, $V_{IN}$=3.6 V | | 0.5 | 1.5 | |
| | | 5.0 $V_{OUT}$ | Quiescent: $V_{IN}$=3.6 V, $I_{OUT}$=0, EN=$V_{IN}$ | | 37 | 45 | |
| | | | Shutdown: EN=0, $V_{IN}$=3.6 V | | 0.5 | 1.5 | |
| | | 3.3 $V_{OUT}$ | Quiescent: $V_{IN}$=2.7 V, $I_{OUT}$=0, EN=$V_{IN}$ | | 50 | 65 | |
| | | | Shutdown: EN=0, $V_{IN}$=2.7 V | | 0.5 | 1.5 | |
| $I_{LK\_OUT}$ | $V_{OUT}$ Leakage Current | | $V_{OUT}$=0, EN=0, $V_{IN}$≥3 V | | 10 | | nA |
| $I_{LK\_RVSR}$ | $V_{OUT}$ to $V_{IN}$ Reverse Leakage | | $V_{OUT}$=5.4 V, $V_{IN}$=3.6 V, EN=0 | | | 2.5 | µA |
| | | | $V_{OUT}$=5.0 V, $V_{IN}$=3.6 V, EN=0 | | | | |
| | | | $V_{OUT}$=3.3 V, $V_{IN}$=3.0 V, EN=0 | | | | |
| $V_{UVLO}$ | Under-Voltage Lockout | | $V_{IN}$ Rising | | 2.2 | 2.3 | V |
| $V_{UVLO\_HYS}$ | Under-Voltage Lockout Hysteresis | | | | 190 | | mV |
| $V_{ENH}$ | Enable HIGH Voltage | | | 1.05 | | | V |
| $V_{ENL}$ | Enable LOW Voltage | | | | | 0.4 | V |
| $I_{LK\_EN}$ | Enable Input Leakage Current | | | | 0.01 | 1.00 | µA |
| $V_{OUT}$ | Output Voltage Accuracy(1) | 5.4 $V_{OUT}$ | $V_{IN}$ from 2.3 V to 4.5 V, $I_{OUT}$≤200 mA | 5.15 | 5.40 | 5.50 | V |
| | | | $V_{IN}$ from 2.7 V to 4.5 V, $I_{OUT}$≤200 mA | 5.20 | 5.40 | 5.50 | |
| | | | $V_{IN}$ from 3.3 V to 4.5 V, $I_{OUT}$≤300 mA | 5.15 | 5.40 | 5.50 | |
| | | 5.0 $V_{OUT}$ | $V_{IN}$ from 2.3 V to 4.5 V, $I_{OUT}$≤200 mA | 4.80 | 5.05 | 5.15 | |
| | | | $V_{IN}$ from 2.7 V to 4.5 V, $I_{OUT}$≤200 mA | 4.85 | 5.05 | 5.15 | |
| | | | $V_{IN}$ from 3.3 V to 4.5 V, $I_{OUT}$≤300 mA | 4.85 | 5.05 | 5.15 | |
| | | 3.3 $V_{OUT}$ | $V_{IN}$ from 2.5 V to 3.2 V, $I_{OUT}$≤200 mA | 3.17 | 3.33 | 3.41 | |
| $V_{REF}$ | Reference Accuracy | | Referred to $V_{OUT}$=5.4 V | 5.325 | 5.400 | 5.475 | V |
| | | | Referred to $V_{OUT}$=5.0 V | 4.975 | 5.050 | 5.125 | |
| | | | Referred to $V_{OUT}$=3.3 V | 3.280 | 3.330 | 3.380 | |
| $t_{OFF}$ | Off Time | | $V_{IN}$=3.6 V, $V_{OUT}$=5.4 V, $I_{OUT}$=200 mA | 185 | 230 | 255 | ns |
| | | | $V_{IN}$=3.6 V, $V_{OUT}$=5.0 V, $I_{OUT}$=200 mA | 195 | 240 | 265 | |
| | | | $V_{IN}$=2.7 V, $V_{OUT}$=3.3 V, $I_{OUT}$=200 mA | 240 | 290 | 350 | |
| $I_{OUT}$ | Maximum Output Current(1) | 5.4 $V_{OUT}$ | $V_{IN}$=2.3 V | 200 | | | mA |
| | | | $V_{IN}$=3.3 V | 300 | | | |
| | | | $V_{IN}$=3.6 V | | 400 | | |
| | | 5.0 $V_{OUT}$ | $V_{IN}$=2.3 V | 200 | | | |
| | | | $V_{IN}$=3.3 V | 300 | | | |
| | | | $V_{IN}$=3.6 V | | 400 | | |
| | | 3.3 $V_{OUT}$ | $V_{IN}$=2.5 V | 250 | | | |
| | | | $V_{IN}$=2.7 V | 300 | | | |
| $I_{SW}$ | SW Peak Current Limit | 5.4 $V_{OUT}$ | $V_{IN}$=3.6 V, $V_{OUT}$>$V_{IN}$ | 1000 | 1400 | 1500 | mA |
| | | 5.0 $V_{OUT}$ | $V_{IN}$=3.6 V, $V_{OUT}$>$V_{IN}$ | 930 | 1100 | 1320 | |
| | | 3.3 $V_{OUT}$ | $V_{IN}$=2.7 V, $V_{OUT}$>$V_{IN}$ | 650 | 800 | 950 | |

*Continued on the following page…*

## Electrical Specifications

Minimum and maximum values are at $V_{IN}$=$V_{EN}$=2.3 V to 4.5 V (2.5 to 3.2 $V_{IN}$ for 3.3 $V_{OUT}$ option), $T_A$=-40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at $T_A$=25°C, $V_{IN}$=$V_{EN}$=3.6 V for $V_{OUT}$=5.0 V / 5.4 V, and $V_{IN}$=$V_{EN}$=2.7 V for $V_{OUT}$=3.3 V.

| Symbol | Parameter | | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{SS}$ | Soft-Start Input Peak Current Limit(2) | 5.4 $V_{OUT}$ | $V_{IN}$=3.6 V, $V_{OUT}$ < $V_{IN}$ | | 900 | | mA |
| | | 5.0 $V_{OUT}$ | $V_{IN}$=3.6 V, $V_{OUT}$ < $V_{IN}$ | | 850 | | |
| | | 3.3 $V_{OUT}$ | $V_{IN}$=2.7 V, $V_{OUT}$ < $V_{IN}$ | | 700 | | |
| $t_{SS}$ | Soft-Start Time(3) | 5.4 $V_{OUT}$ | $V_{IN}$=3.6 V, $I_{OUT}$=200 mA | | 270 | 400 | µs |
| | | 5.0 $V_{OUT}$ | $V_{IN}$=3.6 V, $I_{OUT}$=200 mA | | 100 | 300 | |
| | | 3.3 $V_{OUT}$ | $V_{IN}$=2.7 V, $I_{OUT}$=200 mA | | 250 | 750 | |
| $R_{DS(ON)}$ | N-Channel Boost Switch | | $V_{IN}$=3.6 V | | 300 | | mΩ |
| | P-Channel Sync Rectifier | | $V_{IN}$=3.6 V | | 400 | | |
| $T_{TSD}$ | Thermal Shutdown | | $I_{LOAD}$=10 mA | | 150 | | °C |
| $T_{TSD\_HYS}$ | Thermal Shutdown Hysteresis | | | | 30 | | °C |

**Notes:**

1. $I_{LOAD}$ from 0 to $I_{OUT}$; also includes load transient response. $V_{OUT}$ measured from mid-point of output voltage ripple. Effective capacitance of $C_{OUT}$ > 1.5 µF.
2. Guaranteed by design and characterization; not tested in production.
3. Elapsed time from rising EN until regulated $V_{OUT}$.

## 5.4 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.6 $V_{IN}$, and $T_A$=25°C.

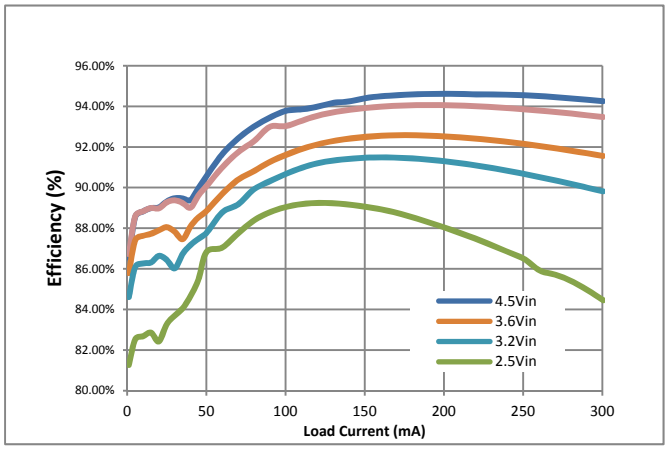



**Figure 6. Efficiency vs. $V_{IN}$**

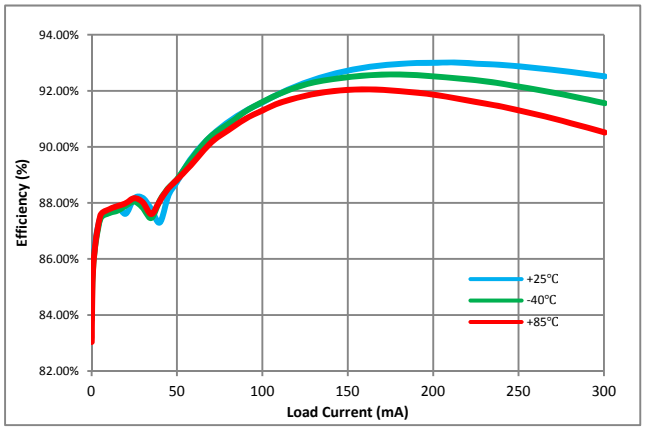



**Figure 7. Efficiency vs. Temperature, 3.6 $V_{IN}$**

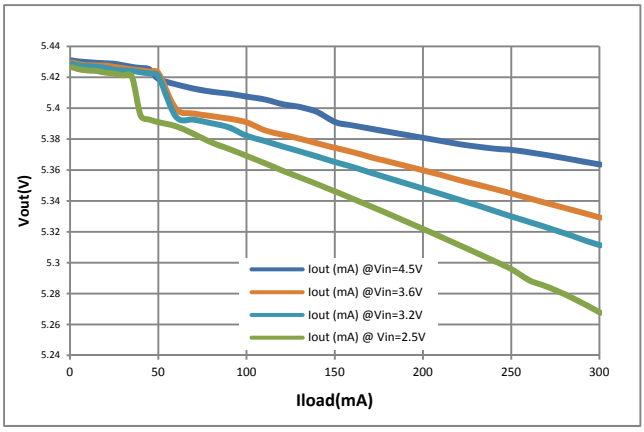



**Figure 8. Line and Load Regulation**

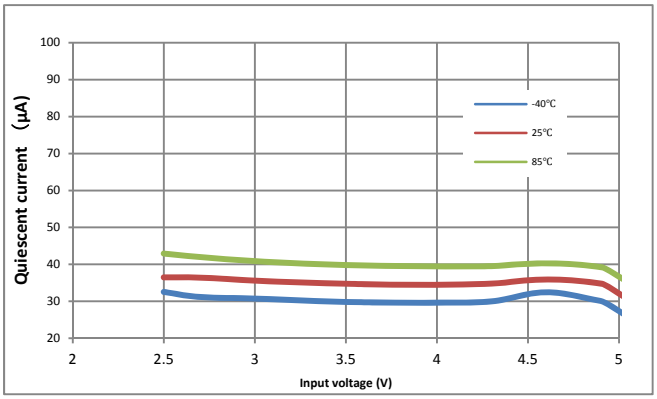



**Figure 9. Quiescent Current**

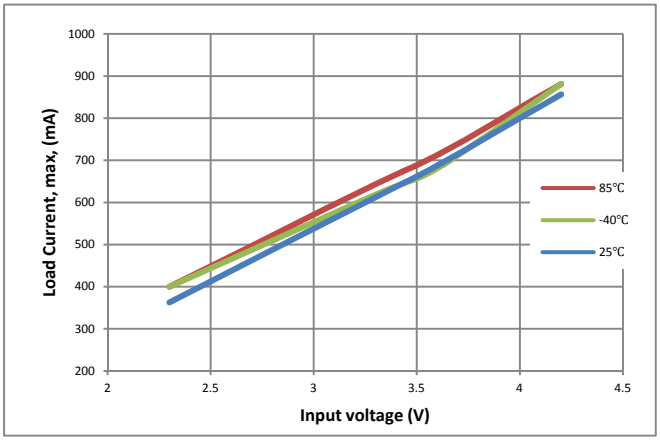



**Figure 10. Maximum DC Load Current**

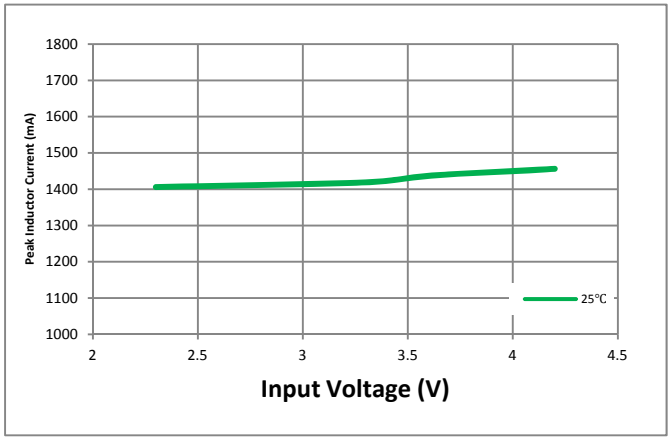



**Figure 11. Peak Inductor Current**

## 5.4 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.6 $V_{IN}$, and $T_A$=25°C.

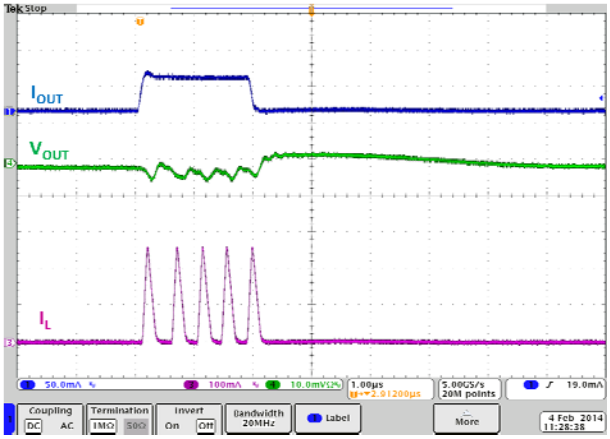



Figure 12. 0-50 mA Load Transient, 100 ns Step

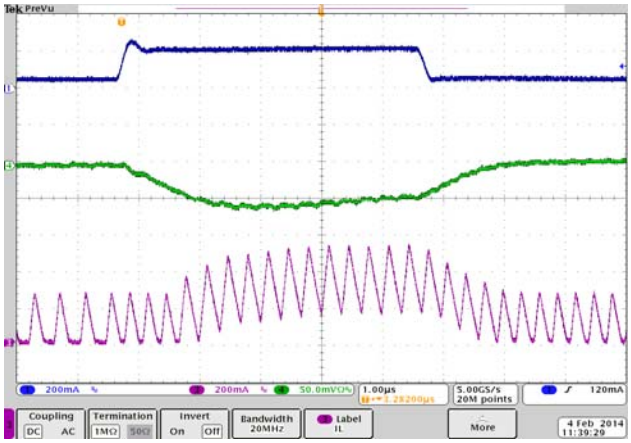



Figure 13. 50-200 mA Load Transient, 100 ns Step

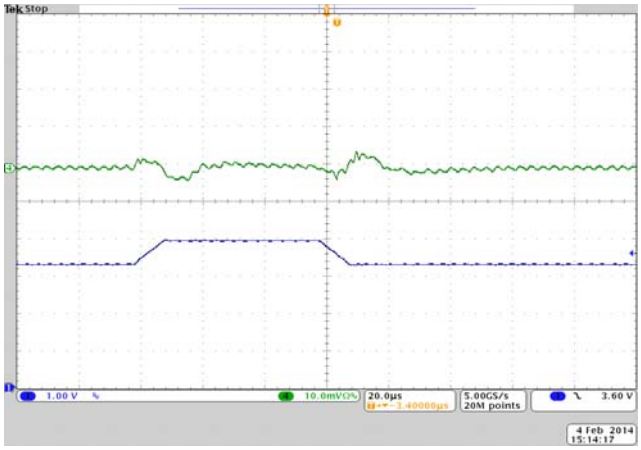



Figure 14. Line Transient, 5 mA Load, 10 µs Step

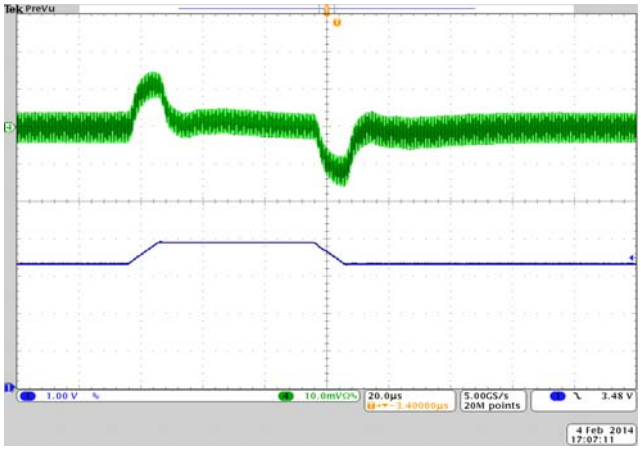



Figure 15. Line Transient, 200 mA Load, 10 µs Step

## 5.0 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.6 $V_{IN}$, and $T_A$=25°C.

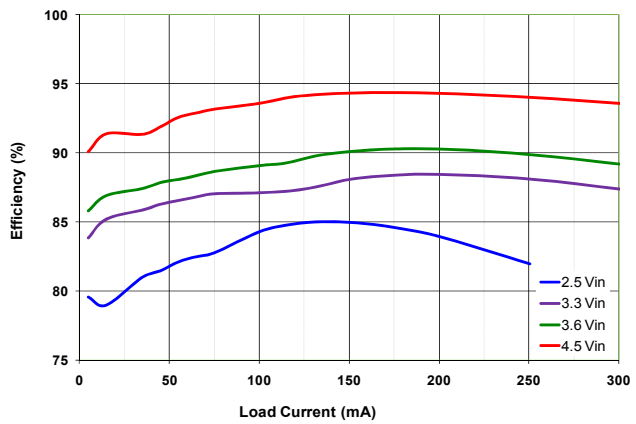



Figure 16. Efficiency vs. $V_{IN}$

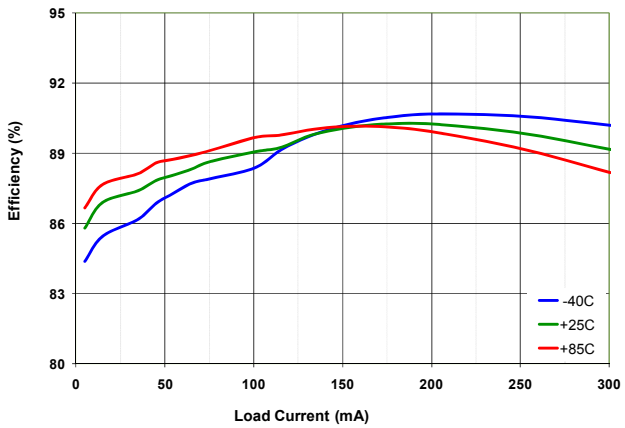



Figure 17. Efficiency vs. Temperature, 3.6 $V_{IN}$

## 5.0 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.6 $V_{IN}$, and $T_A$=25°C.

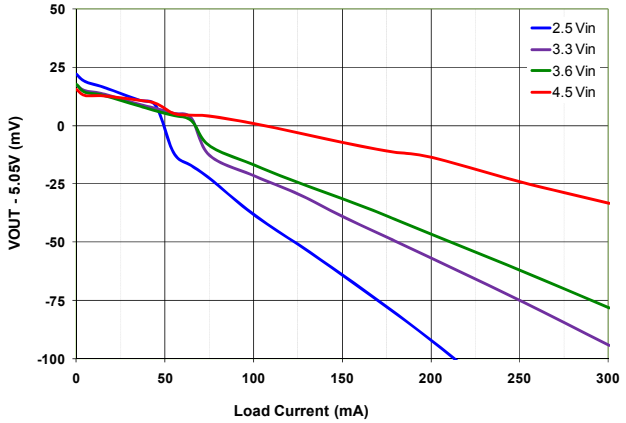



**Figure 18. Line and Load Regulation**

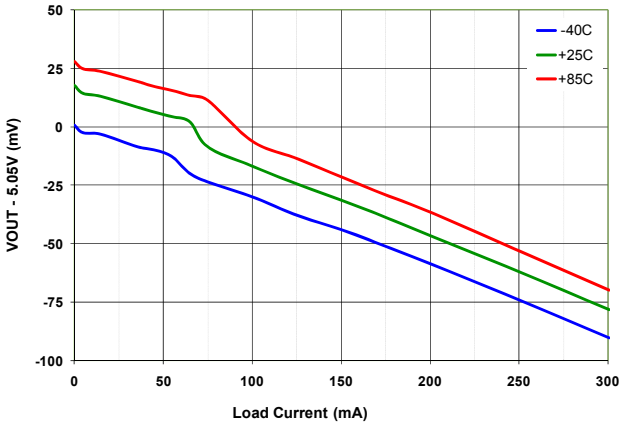



**Figure 19. Load Regulation vs. Temperature, 3.6 $V_{IN}$**

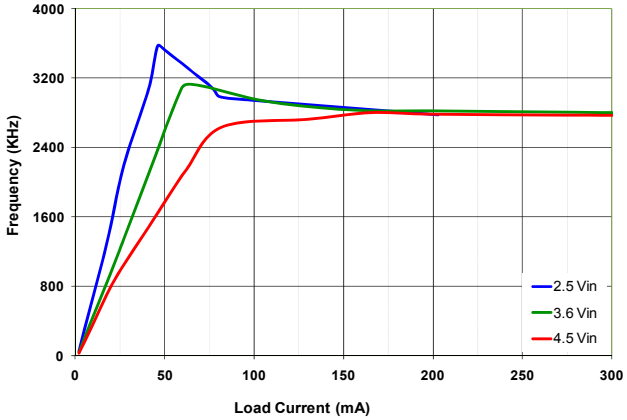



**Figure 20. Switching Frequency**

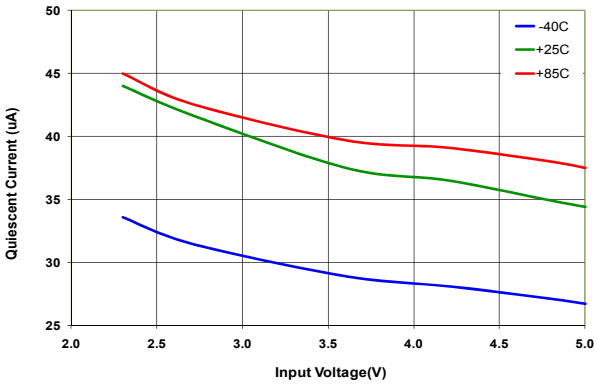



**Figure 21. Quiescent Current**

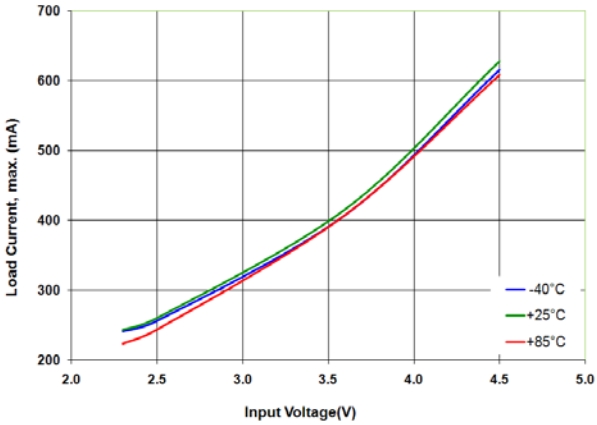



**Figure 22. Maximum DC Load Current**

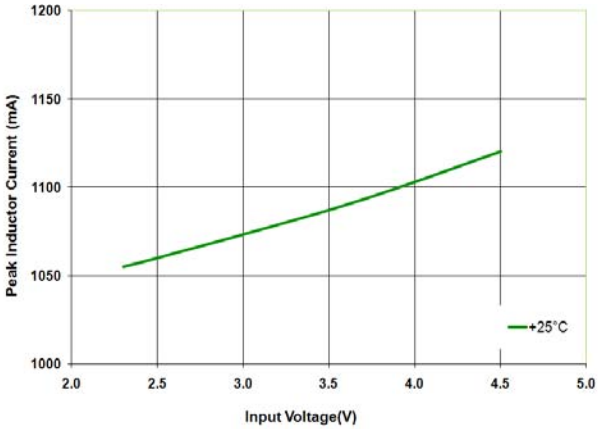



**Figure 23. Peak Inductor Current**

## 5.0 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.6 $V_{IN}$, and $T_A$=25°C.

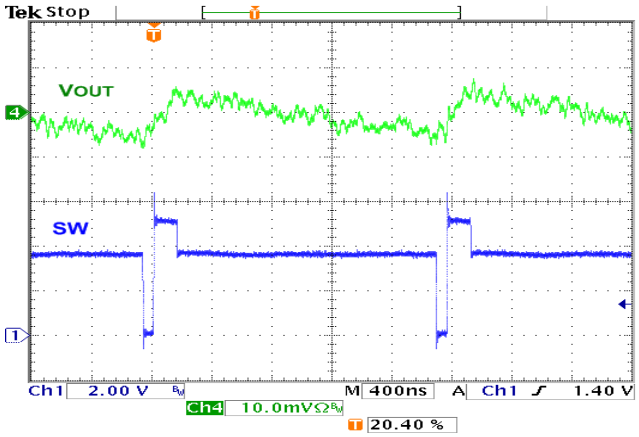



**Figure 24. Output Ripple, 10 mA PFM Load**

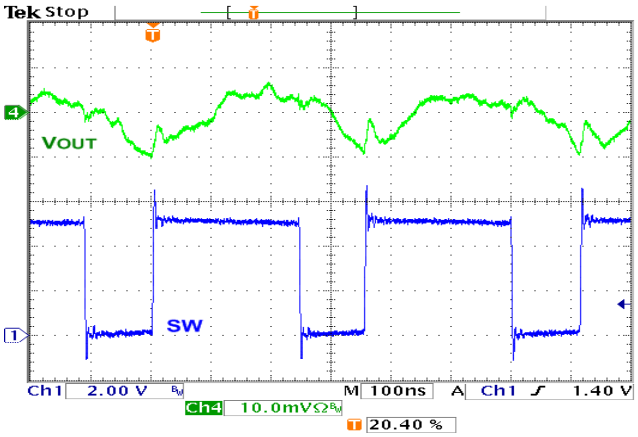



**Figure 25. Output Ripple, 200 mA PWM Load**

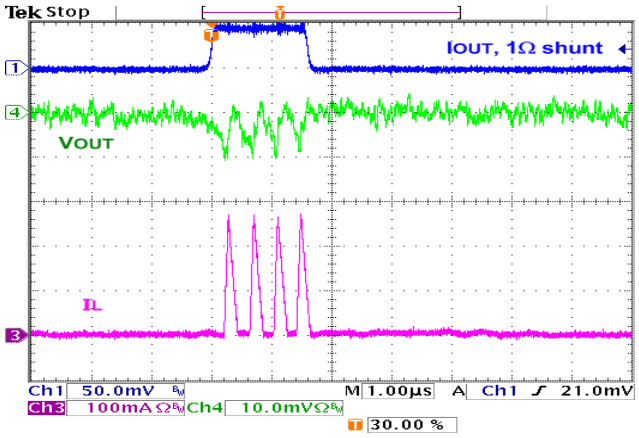



**Figure 26. 0-50 mA Load Transient, 100 ns Step**

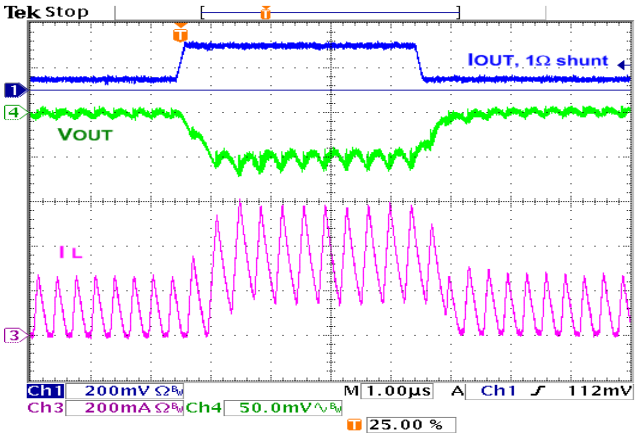



**Figure 27. 50-200 mA Load Transient, 100 ns Step**

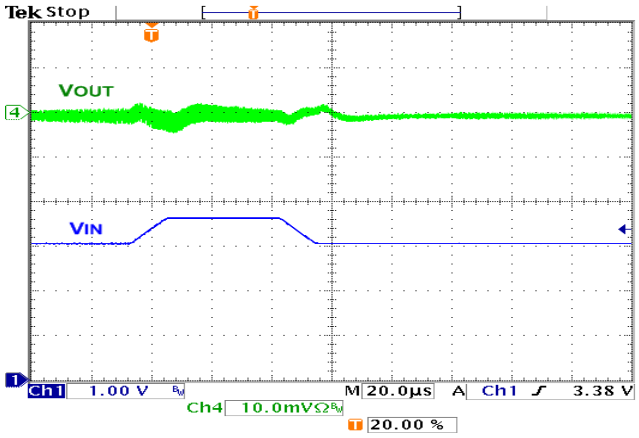



**Figure 28. Line Transient, 5 mA Load, 10 µs Step**

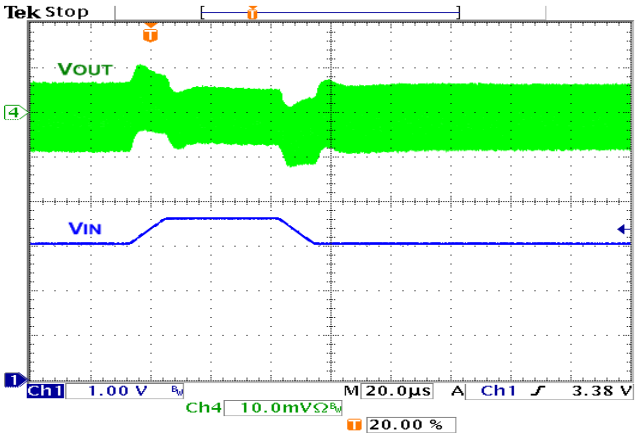



**Figure 29. Line Transient, 200 mA Load, 10 µs Step**

## 5.0 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.6 $V_{IN}$, and $T_A$=25°C.

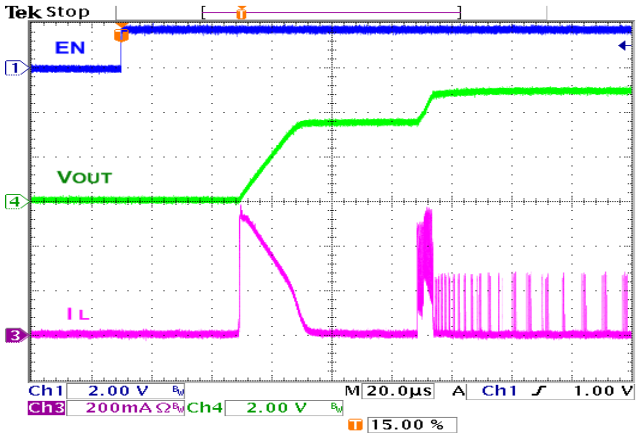



Figure 30. Startup, No Load

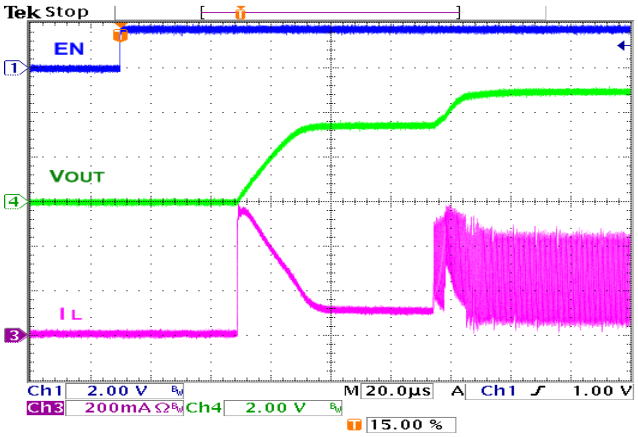



Figure 31. Startup, 33 Ω Load

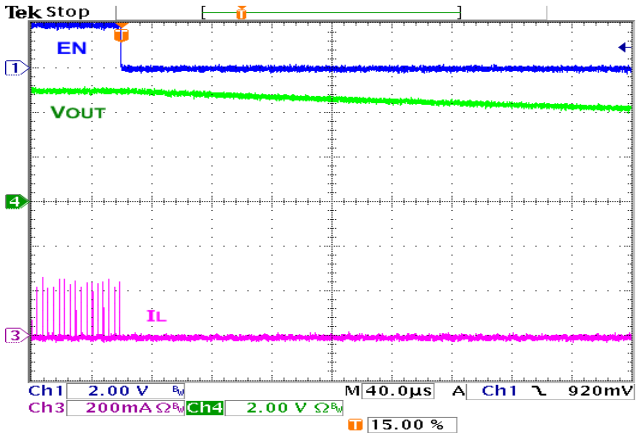



Figure 32. Shutdown, 1 kΩ Load

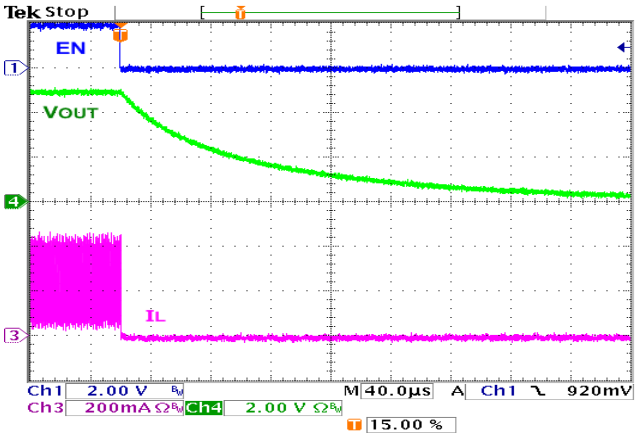



Figure 33. Shutdown, 33 Ω Load

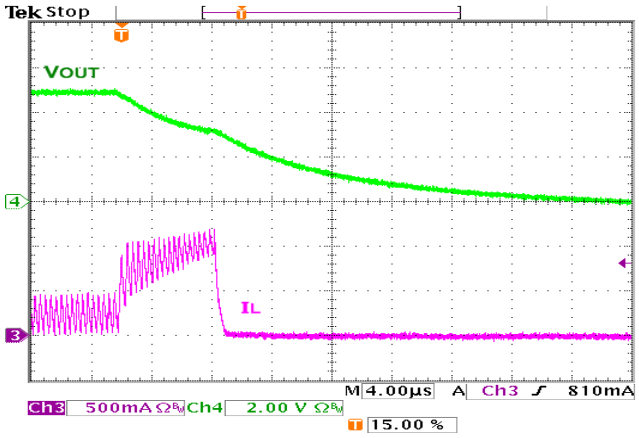



Figure 34. Overload Protection

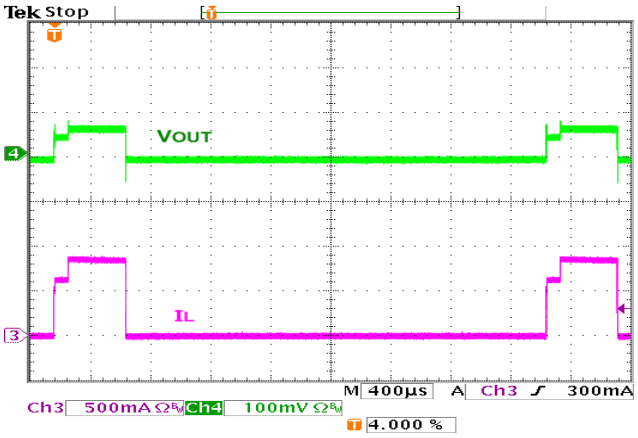



Figure 35. Short-Circuit Response

## 3.3 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.0 $V_{IN}$, and $T_A$=25°C.

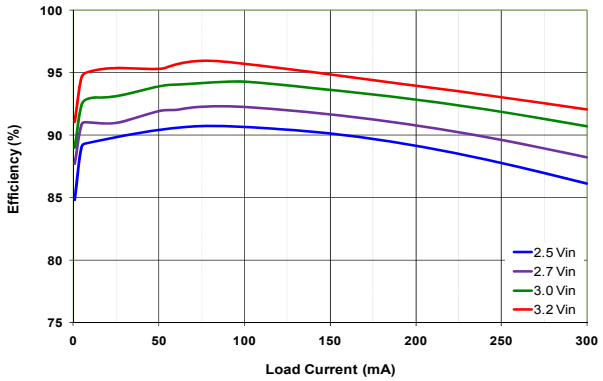



**Figure 36. Efficiency vs. $V_{IN}$**

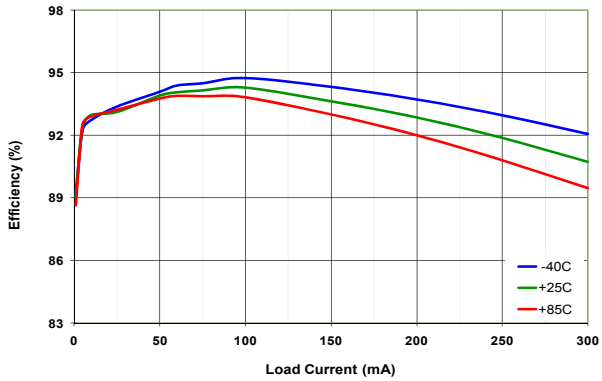



**Figure 37. Efficiency vs. Temperature, 3.0 $V_{IN}$**

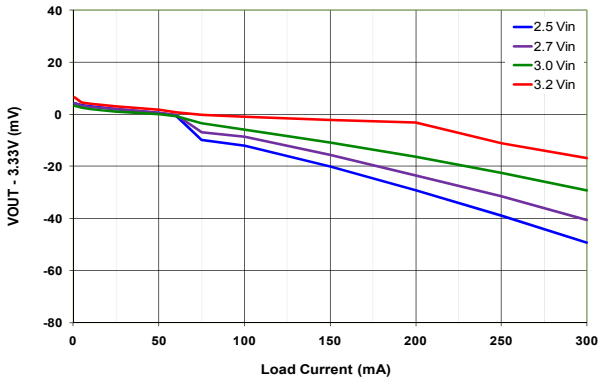



**Figure 38. Line and Load Regulation**

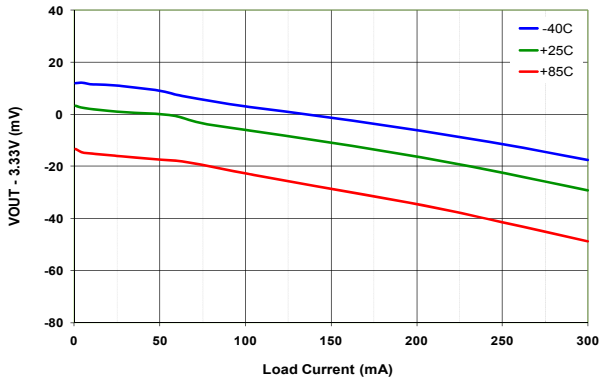



**Figure 39. Load Regulation vs. Temperature, 3.0 $V_{IN}$**

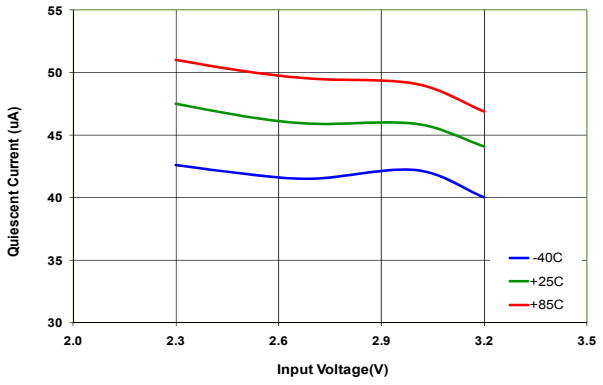



**Figure 40. Quiescent Current**

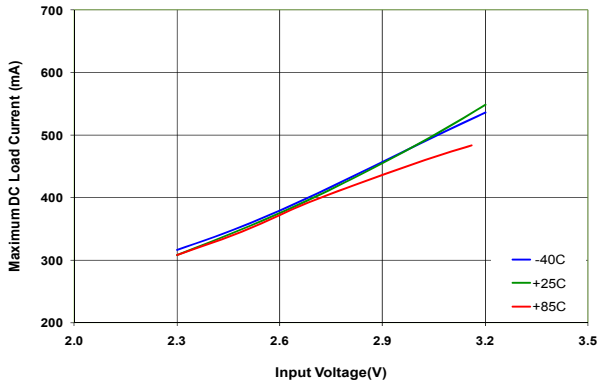



**Figure 41. Maximum DC Load Current**

## 3.3 $V_{OUT}$ Typical Characteristics

Unless otherwise specified; circuit per Figure 1, 3.0 $V_{IN}$, and $T_A$=25°C.

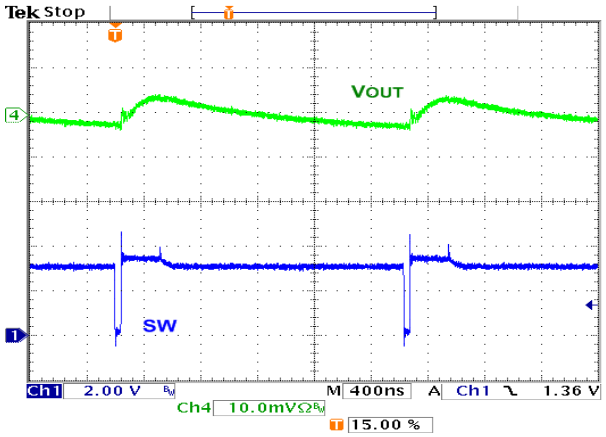



**Figure 42. Output Ripple, 10 mA PFM Load**

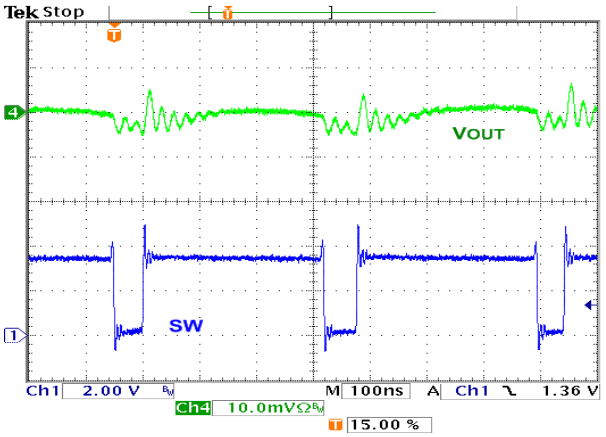



**Figure 43. Output Ripple, 200 mA PWM Load**

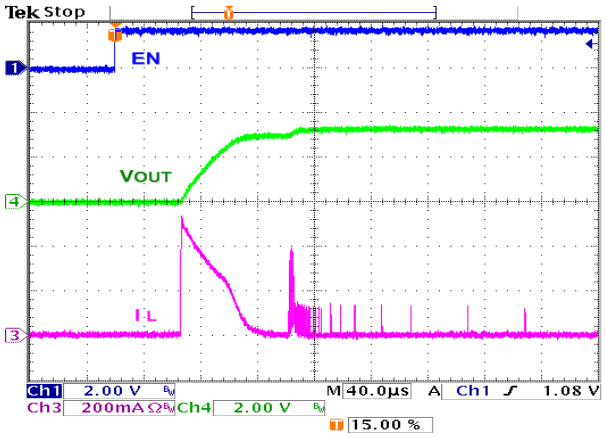



**Figure 44. Startup, No Load**

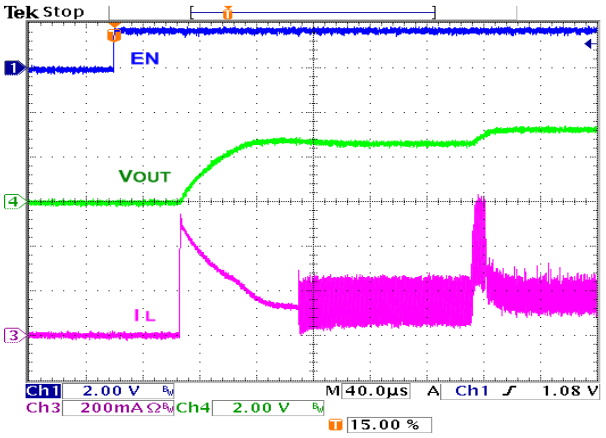



**Figure 45. Startup, 22 Ω Load**

# Functional Description

## Circuit Description

The FAN4860 is a synchronous boost regulator, typically operating at 3 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low $V_{IN}$ voltages.

At light-load currents, the converter switches automatically to power-saving PFM Mode. The regulator automatically and smoothly transitions between quasi-fixed-frequency continuous conduction PWM Mode and variable-frequency PFM Mode to maintain the highest possible efficiency over the full range of load current and input voltage.

## PWM Mode Regulation

The FAN4860 uses a minimum on-time and computed minimum off-time to regulate $V_{OUT}$. The regulator achieves excellent transient response by employing current mode modulation. This technique causes the regulator output to exhibit a load line. During PWM Mode, the output voltage drops slightly as the input current rises. With a constant $V_{IN}$, this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with negligible overshoot.

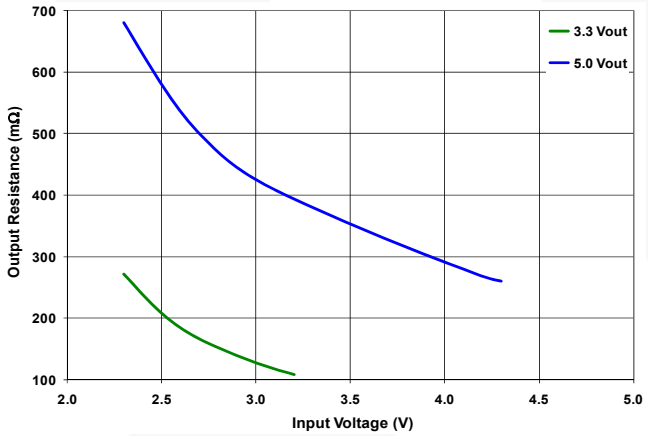



**Figure 46. Output Resistance ($R_{OUT}$)**

When the regulator is in PWM CCM Mode and the target $V_{OUT}$ = 5.05 V, $V_{OUT}$ is a function of $I_{LOAD}$ and can be computed as:

$$V_{OUT} = 5.05 - R_{OUT} \bullet I_{LOAD} \quad (1)$$

For example, at $V_{IN}$=3.3 V, and $I_{LOAD}$=200 mA, $V_{OUT}$ drops to:

$$V_{OUT} = 5.05 - 0.38 \bullet 0.2 = 4.974V \quad (1A)$$

At $V_{IN}$=2.3 V, and $I_{LOAD}$=200 mA, $V_{OUT}$ drops to:

$$V_{OUT} = 5.05 - 0.68 \bullet 0.2 = 4.914V \quad (1B)$$

## PFM Mode

If $V_{OUT} > V_{REF}$ when the minimum off-time has ended, the regulator enters PFM Mode. Boost pulses are inhibited until $V_{OUT} < V_{REF}$. The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore, the regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.05 V in PFM Mode.

**Table 1. Operating States**

| Mode | Description | Invoked When: |
|---|---|---|
| LIN | Linear Startup | $V_{IN} > V_{OUT}$ |
| SS | Boost Soft-Start | $V_{OUT} < V_{REG}$ |
| BST | Boost Operating Mode | $V_{OUT}=V_{REG}$ |

### Shutdown and Startup

If EN is LOW, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, true load disconnect between battery and load prevents current flow from $V_{IN}$ to $V_{OUT}$, as well as reverse flow from $V_{OUT}$ to $V_{IN}$.

### LIN State

When EN rises, if $V_{IN}$ > UVLO, the regulator first attempts to bring $V_{OUT}$ within about 1V of $V_{IN}$ by using the internal fixed current source from $V_{IN}$ ($I_{LIN1}$). The current is limited to about 630 mA during LIN1 Mode.

If $V_{OUT}$ reaches $V_{IN}$-1V during LIN1 Mode, the SS state is initiated. Otherwise, LIN1 times out after 16 clock counts and the LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented to 850 mA. If $V_{OUT}$ fails to reach $V_{IN}$-1 V after 64 clock counts, a fault condition is declared.

### SS State

Upon the successful completion of the LIN state ($V_{OUT} \geq V_{IN}$-1 V), the regulator begins switching with boost pulses current limited to about 50% of nominal level, incrementing to full scale over a period of 32 clock counts.

If the output fails to achieve 90% of its set point within 96 clock counts at full-scale current limit, a fault condition is declared.

### BST State

This is the normal operating mode of the regulator. The regulator uses a minimum $t_{OFF}$-minimum $t_{ON}$ modulation scheme. Minimum $t_{OFF}$ is proportional to $\frac{V_{IN}}{V_{OUT}}$, which keeps the regulator’s switching frequency reasonably constant in CCM. $t_{ON(MIN)}$ is proportional to $V_{IN}$ and is higher if the inductor current reaches 0 before $t_{OFF(MIN)}$ during the prior cycle.

To ensure that $V_{OUT}$ does not pump significantly above the regulation point, the boost switch remains off as long as FB > $V_{REF}$.

## Fault State

The regulator enters the FAULT state under any of the following conditions:

- $V_{OUT}$ fails to achieve the voltage required to advance from LIN state to SS state.
- $V_{OUT}$ fails to achieve the voltage required to advance from SS state to BST state.
- Sustained (32 CLK counts) pulse-by-pulse current limit during the BST state.
- The regulator moves from BST to LIN state due to a short circuit or output overload ($V_{OUT}$ < $V_{IN}$-1 V).

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between $V_{IN}$ and $V_{OUT}$. After waiting 480 CLK counts, a restart is attempted.

## Soft-Start and Fault Timing

The soft-start timing for each state, and the fault times, are determined by the fault clock, whose period is inversely proportional to $V_{IN}$. This allows the regulator more time to charge larger values of $C_{OUT}$ when $V_{IN}$ is lower. With higher $V_{IN}$, this also reduces power delivered to $V_{OUT}$ during each cycle in current limit.

The number of clock counts for each state is illustrated in Figure 47.

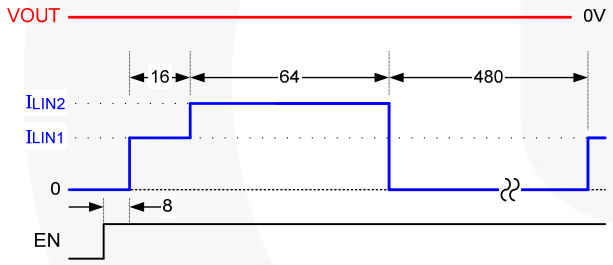



**Figure 47. Fault Response into Short Circuit**

The fault clock period as a function of $V_{IN}$ is shown in Figure 48.

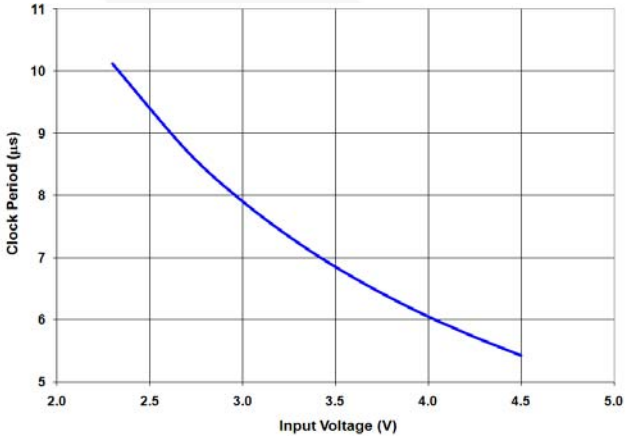



**Figure 48. Fault Clock Period vs. $V_{IN}$**

The $V_{IN}$-dependent LIN Mode charging current is illustrated in Figure 49.

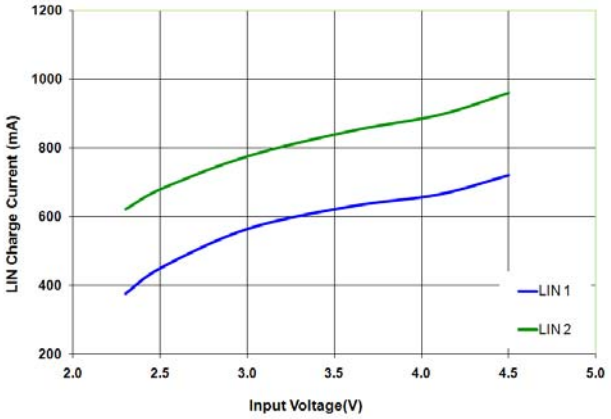



**Figure 49. LIN Mode Current vs. $V_{IN}$**

## Over-Temperature Protection (OTP)

The regulator shuts down when the thermal shutdown threshold is reached. Restart, with soft-start, occurs when the IC has cooled by about 30°C.

## Over-Current Protection (OCP)

During Boost Mode, the FAN4860 employs a cycle-by-cycle peak current limit to protect switching elements. Sustained current limit, for 32 consecutive fault clock counts, initiates a fault condition.

During an overload condition, as $V_{OUT}$ collapses to approximately $V_{IN}$-1 V, the synchronous rectifier is immediately switched off and a fault condition is declared.

Automatic restart occurs once the overload/short is removed and the fault timer completes counting.

# Application Information

## External Component Selection

Table 2 shows the recommended external components for the FAN4860:

**Table 2. External Components**

| REF | Description | Manufacturer |
|---|---|---|
| L1 | 1.0 µH, 0.8 A, 190 mΩ, 0805 | Murata LQM21PN1R0MC0, or equivalent |
| $C_{IN}$ | 2.2 µF, 6.3 V, X5R, 0402 | Murata GRM155R60J225M |
| | | TDK C1005X5R0J225M |
| $C_{OUT}$ | 4.7 µF, 10 V, X5R, 0603(4) | Kemet C0603C475K8PAC |
| | | TDK C1608X5R1A475K |

**Note:**

4. A 6.3 V-rated 0603 capacitor may be used for $C_{OUT}$, such as Murata GRM188R60J225M. All datasheet parameters are valid with the 6.3 V-rated capacitor. Due to DC bias effects, the 10 V capacitor offers a performance enhancement; particularly output ripple and transient response, without any size increase.

## Output Capacitance ($C_{OUT}$)

### Stability

The effective capacitance ($C_{EFF}$) of small, high-value, ceramic capacitors decrease as their bias voltage increases, as shown in Figure 50.

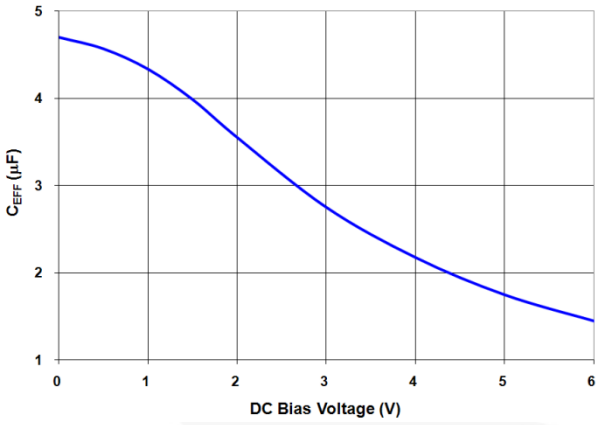



**Figure 50. $C_{EFF}$ for 4.7 µF, 0603, X5R, 6.3 V (Murata GRM188R60J475K)**

FAN4860 is guaranteed for stable operation with the minimum value of $C_{EFF}$ ($C_{EFF(MIN)}$) outlined in Table 3.

**Table 3. Minimum $C_{EFF}$ Required for Stability**

| Operating Conditions | | $C_{EFF(MIN)}$ (µF) |
|---|---|---|
| $V_{IN}$ (V) | $I_{LOAD}$ (mA) | |
| 2.3 to 4.5 | 0 to 200 | 1.5 |
| 2.7 to 4.5 | 0 to 200 | 1.0 |
| 2.3 to 4.5 | 0 to 150 | 1.0 |

$C_{EFF}$ varies with manufacturer, dielectric material, case size, and temperature. Some manufacturers may be able to provide an X5R capacitor in 0402 case size that retains $C_{EFF}$ >1.5 µF with 5V bias; others may not. If this $C_{EFF}$ cannot be economically obtained and 0402 case size is required, the IC can work with the 0402 capacitor as long as the minimum $V_{IN}$ is restricted to >2.7 V.

For best performance, a 10 V-rated 0603 output capacitor is recommended (Kemet C0603C475K8PAC, or equivalent). Since it retains greater $C_{EFF}$ under bias and over temperature, output ripple can is reduced and transient capability enhanced.

### Output Voltage Ripple

Output voltage ripple is inversely proportional to $C_{OUT}$. During $t_{ON}$, when the boost switch is on, all load current is supplied by $C_{OUT}$.

$$V_{RIPPLE(P-P)} = t_{ON} \bullet \frac{I_{LOAD}}{C_{OUT}} \quad (2)$$

and

$$t_{ON} = t_{SW} \bullet D = t_{SW} \bullet \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (3)$$

Therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \bullet \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \bullet \frac{I_{LOAD}}{C_{OUT}} \quad (4)$$

where:

$$t_{SW} = 1/f_{SW} \quad (5)$$

As can be seen from Equation 4, the maximum $V_{RIPPLE}$ occurs when $V_{IN}$ is minimum and $I_{LOAD}$ is maximum.

### Startup

Input current limiting is in effect during soft-start, which limits the current available to charge $C_{OUT}$. If the output fails to achieve regulation within the time period described in the soft-start section above; a FAULT occurs, causing the circuit to shut down, then restart after a significant time period. If $C_{OUT}$ is a very high value, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high-current load and high capacitance are both present during soft-start, the circuit may fail to achieve regulation and continually attempt soft-start, only to have $C_{OUT}$ discharged by the load when in the FAULT state.

The circuit can start with higher values of $C_{OUT}$ under full load if $V_{IN}$ is higher, since:

$$I_{OUT} = \left(I_{LIM(PK)} - \frac{I_{RIPPLE}}{2}\right) \bullet \frac{V_{IN}}{V_{OUT}} \quad (6)$$

Generally, the limitation occurs in BST Mode.

The FAN4860 starts on the first pass (without triggering a FAULT) under the following conditions for $C_{EFF(MAX)}$:

**Table 4. Maximum $C_{EFF}$ for First-Pass Startup**

| Operating Conditions | | | | $C_{EFF(MAX)}$ (µF) |
|---|---|---|---|---|
| $V_{IN}$ (V) | $R_{LOAD(MIN)}$ (Ω) | | | |
| | 5.4 $V_{OUT}$ | 5.0 $V_{OUT}$ | 3.3 $V_{OUT}$ | |
| > 2.3 | 27 | 25 | 16 | 10 |
| > 2.7 | 27 | 25 | 16 | 15 |
| > 2.7 | 37 | 33 | 20 | 22 |

$C_{EFF}$ values shown in Table 4 typically apply to the lowest $V_{IN}$. The presence of higher $V_{IN}$ enhances ability to start into larger $C_{EFF}$ at full load.

## Transient Protection

To protect against external voltage transients caused by ESD discharge events, or improper external connections, some applications employ an external transient voltage suppressor (TVS) and Schottky diode (D1 in Figure 51).

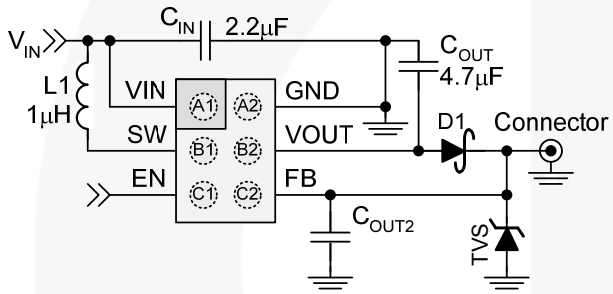



**Figure 51. FAN4860 with External Transient Protection**

The TVS is designed to clamp the FB line (system $V_{OUT}$) to +10 V or –2 V during external transient events. The Schottky diode protects the output devices from the positive excursion. The FB pin can tolerate up to 14 V of positive excursion, while both the FB and VOUT pins can tolerate negative voltages.

The FAN4860 includes a circuit to detect a missing or defective D1 by comparing $V_{OUT}$ to FB. If $V_{OUT}$ – FB > about 0.7 V, the IC shuts down. The IC remains shut down until $V_{OUT}$ < UVLO and $V_{IN}$ < UVLO+0.7 or EN is toggled.

$C_{OUT2}$ may be necessary to preserve load transient response when the Schottky is used. When a load is applied at the FB pin, the forward voltage of the D1 rapidly increases before the regulator can respond or the inductor current can change. This causes an immediate drop of up to 300 mV, depending on D1's characteristics if $C_{OUT2}$ is absent. $C_{OUT2}$ supplies instantaneous current to the load while the regulator adjusts the inductor current. A value of at least half of the minimum value of $C_{OUT}$ should be used for $C_{OUT2}$. $C_{OUT2}$ needs to withstand the maximum voltage at the FB pin as the TVS is clamping.

The maximum DC output current available is reduced with this circuit, due to the additional dissipation of D1.

## Layout Guideline

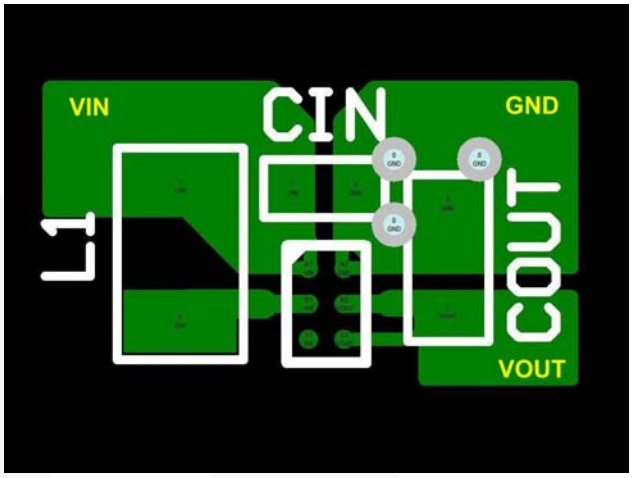



**Figure 52. WLCSP Suggested Layout (Top View)**

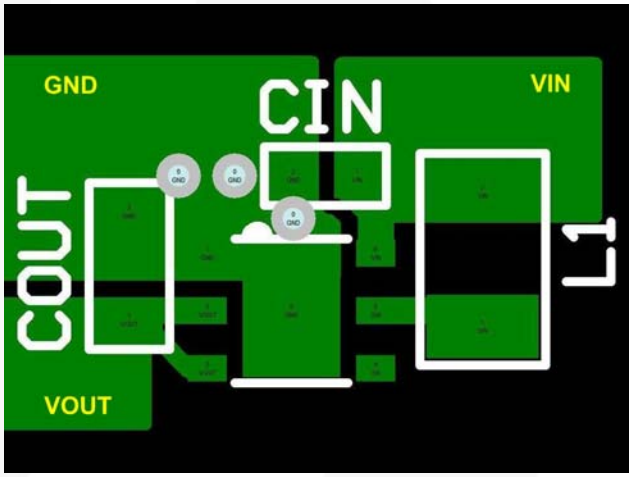
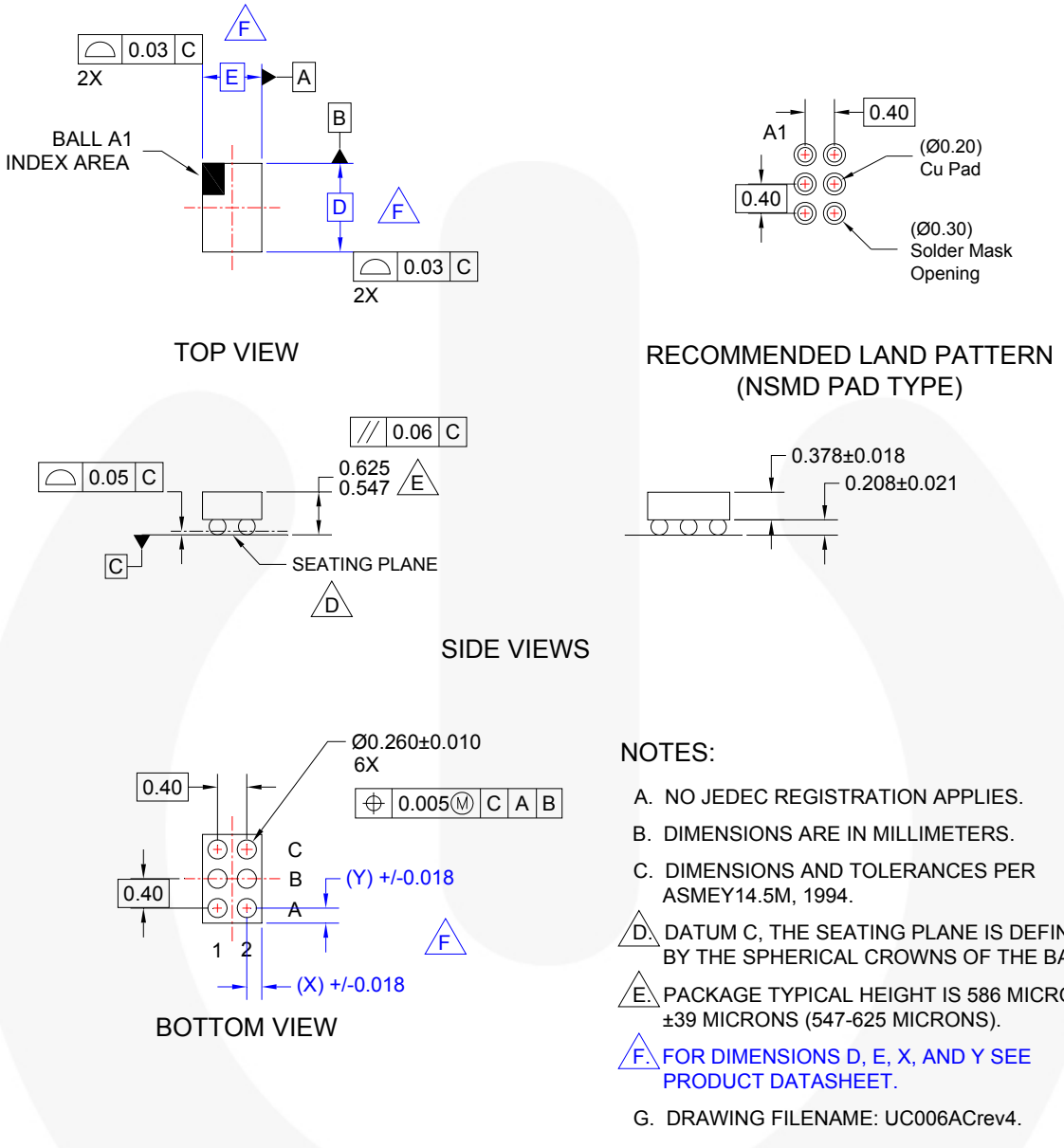



**Figure 53. UMLP Suggested Layout (Top View)**

## Physical Dimensions




NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 1994.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: UC006ACrev4.

**Figure 54. 6-Lead, 0.4 mm Pitch, WLCSP Package**

### Product-Specific Dimensions

| Product | D | E | X | Y |
|---|---|---|---|---|
| FAN4860UC5X | 1.230mm ±0.030 mm | 0.880 mm ±0.030 mm | 0.240 mm | 0.215 mm |
| FAN4860UC33X | | | | |

*Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.*

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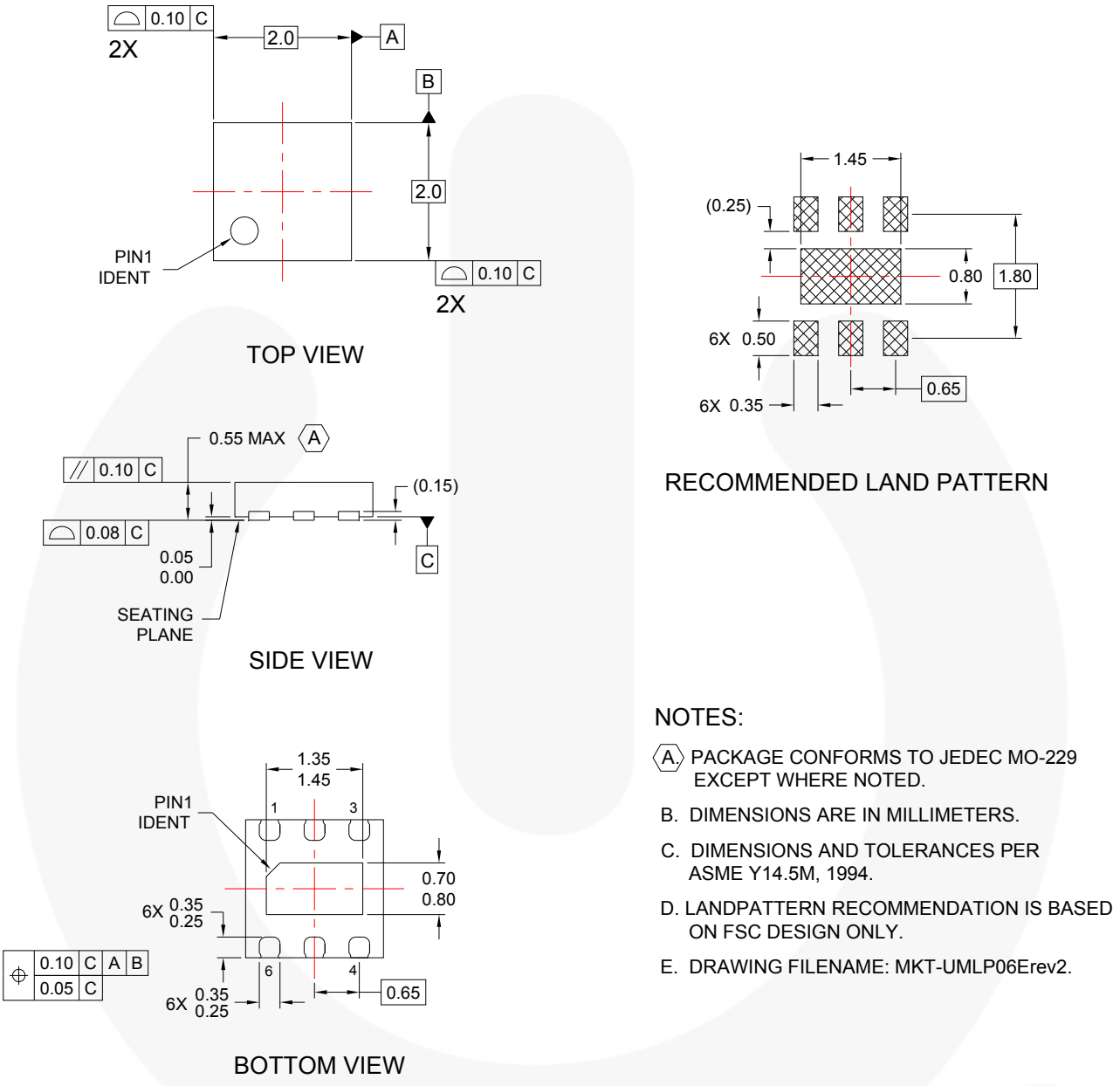
## Physical Dimensions




NOTES:

A. PACKAGE CONFORMS TO JEDEC MO-229 EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.

E. DRAWING FILENAME: MKT-UMLP06Erev2.

**Figure 55. 6-Lead, UMLP Package**

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