FAIRCHILD SEMICONDUCTOR®

October 2012

FAN6749
Highly Integrated Ultra Green-Mode PWM Controller

Features

- High-Voltage Startup
- Low Operating Current: 1.8 mA
- Linearly Decreasing PWM Frequency to 24 kHz
- Proprietary Frequency Hopping to Reduce EMI
- Two-Level Over-Current Protection (OCP), 1400 ms Delay for Normal Peak Load
- Two-Level OCP, 56 ms Delay for Super Peak Load
- Output Short-Circuit Protection (SCP)
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- HV Pin Brown-in/out Protection with Hysteresis
- Constant Power Limit by HV Sampling
- Internal FB Open-Loop Protection (OLP)
- GATE Output Maximum Voltage Clamp: 14.5V
- V_{DD} Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)
- Integrated 6ms Soft-Start Function
- Internal Latch Circuit (OVP, OTP, OCP, OLP, SCP)
- Internal OTP Sensor with Hysteresis

Applications

General-Purpose Switched-Mode Power Supplies and Flyback Power Converters, including:

- Power Adapters
- Open-Frame SMPS; Specifically for SMPS with Surge-Current Output, such as for Printer, Scanner, Motor Drivers

Description

The FAN6749 highly integrated PWM controller enhances the performance of flyback converters. To minimize standby power consumption, a proprietary Green-Mode function continuously decreases the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters Burst Mode and completely shuts off PWM output. Green Mode helps power supplies meet international power conservation requirements.

The FAN6749 is designed for SMPS with surge-current output and incorporates a two-level Over-Current Protection (OCP) function. Besides the cycle-by-cycle current limiting, two-level OCP can handle peak loading within a specified delay time.

FAN6749 also integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. Built-in synchronized slope compensation helps achieve stable peak-current control. To keep constant output power limit over universal AC input range, the current limit and OCP threshold voltage are adjusted according to AC line voltage detected by the HV pin. Gate output is clamped at 14.5 V to protect the external MOSFET from over-voltage damage.

Other protection functions include: AC input brownout protection with hysteresis, Short-Circuit Protection (SCP) for output-short condition, and V_{DD} Over-Voltage Protection (OVP). For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When OLP, OCP, SCP, V_{DD} OVP, or OTP is activated, an internal latch circuit latches off the controller. The latch resets when V_{DD} is removed.

OVP	OCP	OLP	OTP	SCP
Latch	Latch	Latch	Latch	Latch

There are three differences from FAN6748 to FAN6749:

- Over-current protection debounce time is extended to 1400 ms.
- Brown-out debounce time is extended to 100 ms.
- No SENSE short-circuit protection function.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6749MLM	-40 to +105°C	8-Pin Small Outline Package (SOP)	Reel & Tape

Application Diagram

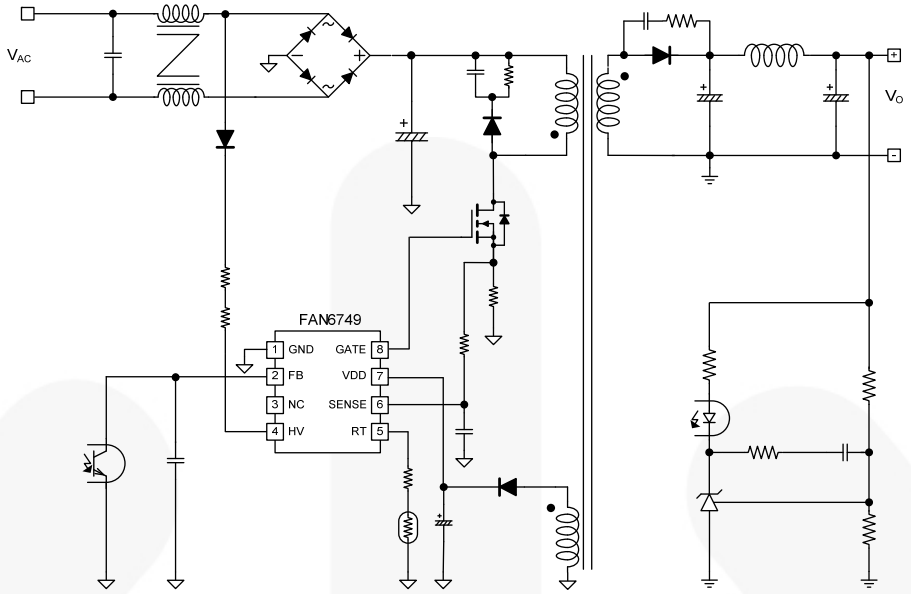


Figure 1. Typical Application

Internal Block Diagram

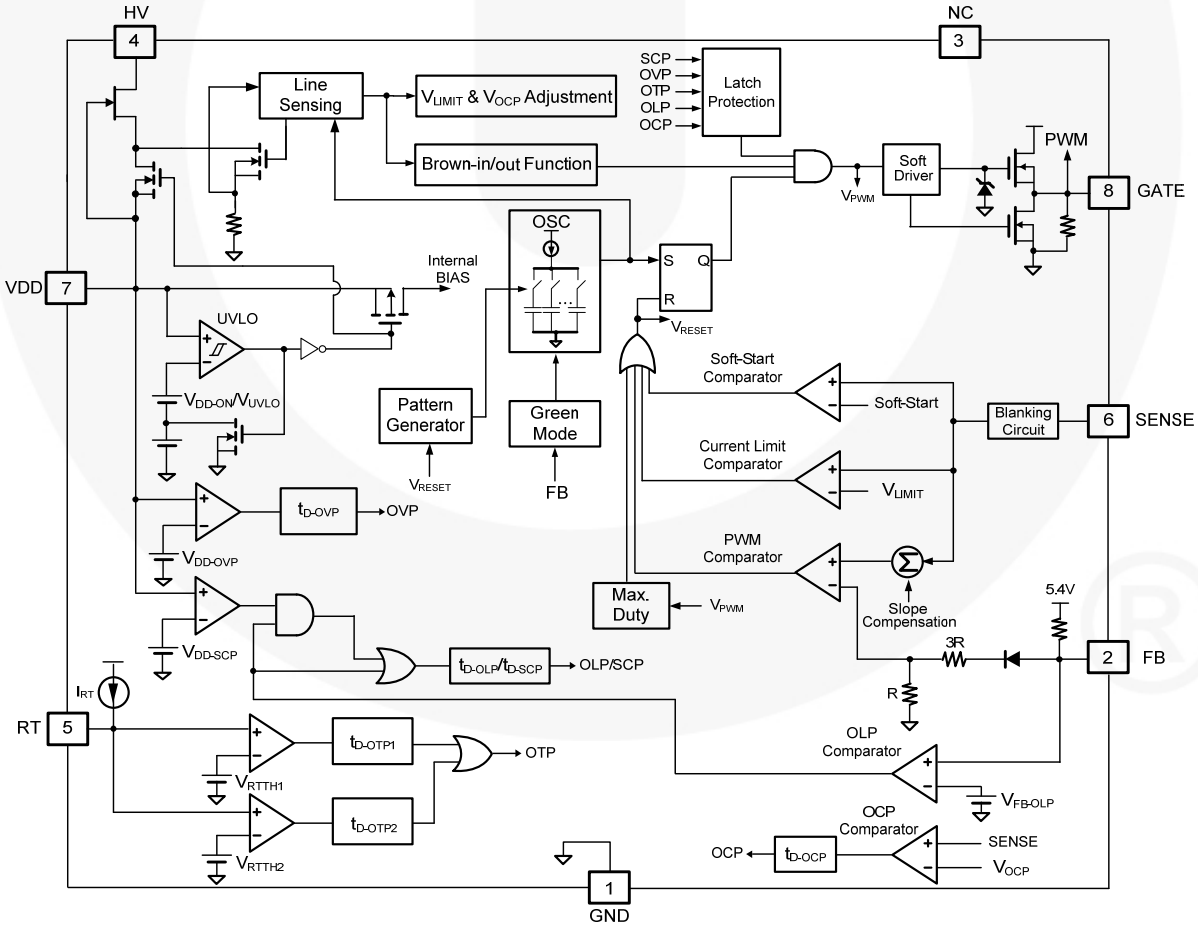
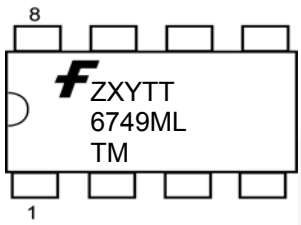


Figure 2. Functional Block Diagram

Marking Information



F - Fairchild Logo
Z - Plant Code
X - 1-Digit Year Code
Y - 1-Digit Week Code
TT - 2-Digit Die Run Code
T - Package Type (M=SOP)
M - Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

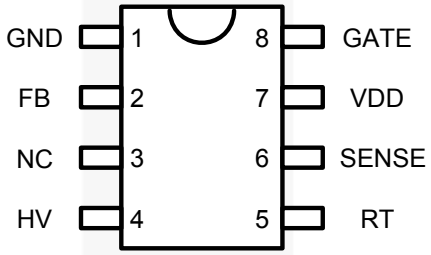


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground Pin**. A 0.1 µF decoupling capacitor between VDD and GND is recommended.
2	FB	**Feedback Pin**. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined by comparing the FB signal with current-sense signal from the SENSE pin.
3	NC	No Connection
4	HV	**High-Voltage Startup**. The HV pin is typically connected to the AC line input through an external diode and a resistor (R_{HV}). This pin is used not only to charge V_{DD} capacitor during startup, but also to sense the line voltage. The line voltage information is used for brown-out protection and power limit line compensation.
5	RT	**Over-Temperature Protection**. An external NTC thermistor is connected from this pin to the GND pin. Once the voltage of the RT pin drops below the threshold voltage, the controller latches off the PWM. The RT pin also provides external latch protection. If the RT pin is not connected to an NTC resistor for over-temperature protection, place a 100 kΩ resistor to ground to prevent noise interference.
6	SENSE	**Current Sense**. The sensed voltage is used for peak-current-mode control, over-current protection, short-circuit protection, and cycle-by-cycle current limiting.
7	VDD	**Power Supply of IC**. A holdup capacitor typically connects from this pin to ground. A rectifier diode in series with the transformer auxiliary winding connects to this pin to supply bias during normal operation.
8	GATE	**Gate Drive Output**. The totem-pole output driver for the power MOSFET; internally limited to $V_{GATE-CLAMP}$.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage[1,2]			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{SENSE}	SENSE Pin Input Voltage		-0.3	7.0	V
V_{RT}	RT Pin Input Voltage		-0.3	7.0	V
V_{HV}	Continuous Input Voltage			500	V
	Pulse Input Voltage[3]			640	
P_D	Power Dissipation ($T_A < 50°C$)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			150	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Human Body Model[4], JEDEC:JESD22-A114	All Pins Except HV Pin		6	kV
	Charged Device Model[4], JEDEC:JESD22-C101	All Pins Except HV Pin		2	kV

Notes:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Duration of pulse input voltage is less than or equal to ≤ 1 second.
4. ESD with the HV pin CDM=1000 V and HBM=500 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{HV}	HV Startup Resistor	150	200	250	kΩ

Electrical Characteristics

V_{DD}=15 V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{OP}	Continuously Operating Voltage	Limited by V_{DD} OVP			25	V
V_{DD-ON}	Threshold Voltage to Startup	V_{DD} Rising	16	17	18	V
V_{DD-OFF}	Threshold Voltage to Stop Switching in Protection Mode	V_{DD} Falling	10	11	12	V
V_{DD-OLP}	Threshold Voltage to Turn On HV Startup in Protection Mode	V_{DD} Falling	6.5	7.5	8.5	V
V_{UVLO}	Threshold Voltage to Stop Switching in Normal Mode	V_{DD} Falling	6.0	6.5	7.0	V
$V_{RESTART}$	Threshold Voltage to Enable HV Startup to Charge V_{DD} in Normal Mode	V_{DD} Falling	4.5	5.0	5.5	V
V_{DD-LH}	Threshold Voltage to Release Latch Mode	V_{DD} Falling	3.5	4.0	4.5	V
V_{DD-AC}	Threshold Voltage on VDD Pin for Disable Brown-in to Avoid Startup Failure		V_{UVLO} +2.5	V_{UVLO} +3	V_{UVLO} +3.5	V
V_{DD-SCP}	Threshold Voltage on VDD Pin for Short-Circuit Protection (SCP)	V_{FB} > V_{FB-OLP}	V_{DD-OFF} +1.0	V_{DD-OFF} +1.5	V_{DD-OFF} +2.0	V
t_{D-SCP}	Debounce Time for SCP	V_{FB}>V_{FB-OLP} & V_{DD}< V_{DD-SCP}	12	17	22	ms
I_{DD-ST}	Startup Current	V_{DD-ON} – 0.16 V			30	µA
I_{DD-OP1}	Supply Current in PWM Operation	V_{DD}=20 V, V_{FB} = 3 V Gate Open		1.8	2.4	mA
I_{DD-OP2}	Supply Current when PWM Stops	V_{DD}=15 V, V_{FB} < 1.4 V		1.0	1.9	mA
I_{LH}	Operating Current when V_{DD}<V_{DD-OFF} in Protection Mode	V_{DD} = 5 V	100	120	140	µA
I_{DD-OLP}	Internal Sink Current	V_{DD-OLP}+0.1 V	265	325	385	µA
V_{DD-OVP}	Threshold Voltage for V_{DD} Over-Voltage Protection		28.5	29.0	29.9	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		160	200	240	µs

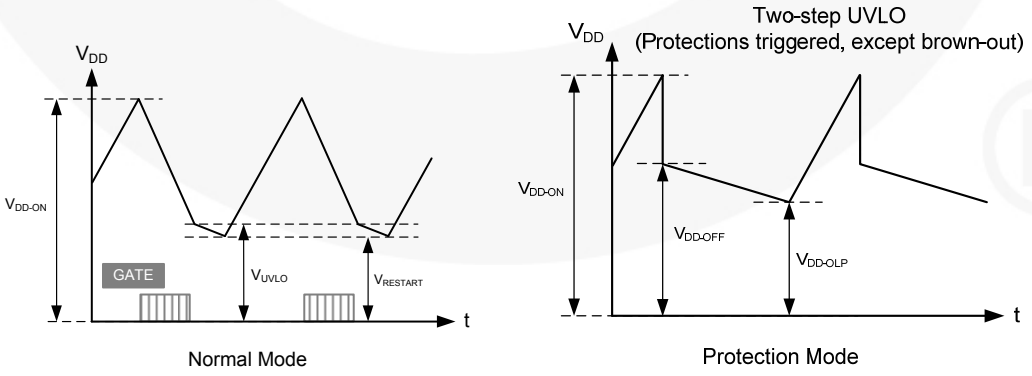


Figure 5. V_{DD} Behavior

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Electrical Characteristics (Continued)

V_{DD}=15 V and T_A=25°C unless otherwise noted.

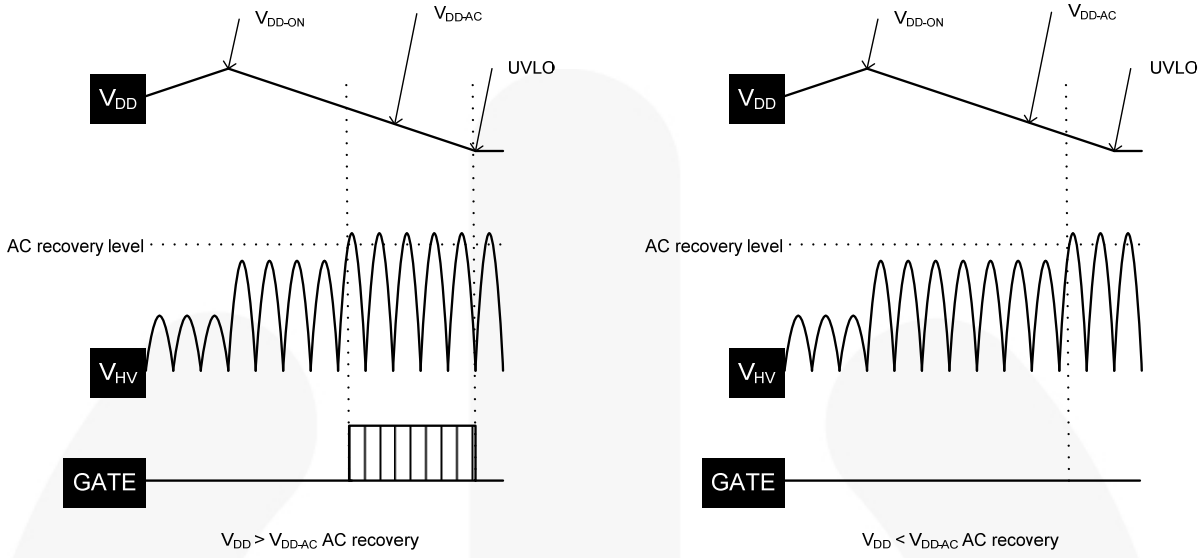

Figure 6. V_{DD-AC} & AC Recovery

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HV Section						
I_{HV}	Supply Current from HV Pin	V_{DC}=120 V, V_{DD}=0 V	2.0	3.5	5.0	mA
I_{HV-LC}	Leakage Current after Startup	HV=500 V, V_{DD}=V_{DD-OFF}+1 V		1	20	µA
V_{AC-OFF}	Threshold Voltage for Brownout	DC Source Series R=200 kΩ to HV Pin	90	100	110	V
V_{AC-ON}	Threshold Voltage for Brown-In	DC Source Series R=200 kΩ to HV Pin	100	110	120	V
ΔV_{AC}	V_{AC-ON} - V_{AC-OFF}	DC Source Series R=200 kΩ to HV Pin	8	10	17	V
$t_{S-CYCLE}$	Line Voltage Sample Cycle[7]	V_{FB} > V_{FB-N}	170	200	230	µs
		V_{FB} < V_{FB-G}	400	520	640	
t_{H-TIME}	Line Voltage Hold Period[7]		18	23	28	µs
t_{UPDATE}	Peak Line Voltage Data Update Cycle for High / Low Line Compensation[7]	V_{FB} > V_{FB-N}	20	24	28	ms
		V_{FB} = V_{FB-G}	64	72	80	
$t_{D-AC-OFF}$	Debounce Time for Brownout		70	100	130	ms
Oscillator Section						
f_{OSC}	Switching Frequency when V_{FB}>V_{FB-N}	Center Frequency	62	65	68	kHz
		Hopping Range	±3.5	±4.0	±4.5	
t_{HOP}	Hopping Period		16	20	24	ms
f_{OSC-G}	Switching Frequency When V_{FB}<V_{FB-G}	Center Frequency	20	24	28	kHz
		Hopping Range	±1.25	±1.55	±1.85	
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11 V to 22 V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-40 to 105°C			5	%

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Electrical Characteristics (Continued)

V_{DD}=15 V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Feedback Input Section						
A_V	Input Voltage to Current-Sense Attenuation		1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	FB Internal Pull-High Impedance		15	17	19	kΩ
$V_{FB-OPEN}$	FB internal Biased Voltage	FB Pin Open	5.2	5.4	5.6	V
V_{FB-OLP}	Threshold Voltage for OLP		4.3	4.6	4.9	V
t_{D-OLP}	Debounce Time for OLP		40	56	72	ms
V_{FB-N}	Threshold Voltage for Maximum Switching Frequency	Pin, FB Voltage(V_{FB}=V_{FB-N})	2.5	2.7	2.9	V
V_{FB-G}	Threshold Voltage for Minimum Switching Frequency	Pin, FB Voltage(V_{FB}=V_{FB-G})	2.05	2.25	2.45	V
S_G	Slope for Green-Mode Modulation			85		Hz/mV
$V_{FB-ZDCR}$	Threshold Voltage for Zero Duty Cycle Recovery		1.9	2.1	2.3	V
V_{FB-ZDC}	Threshold Voltage for Zero Duty Cycle		1.8	2.0	2.2	V
$V_{FB-ZDCR}$ - V_{FB-ZDC}	Zero Duty Cycle Hysteresis		0.05	0.10	0.15	V
Current-Sense Section						
t_{PD}	Delay to Output			65	200	ns
t_{LEB}	Leading-Edge Blanking		230	270	310	ns
$V_{LIMIT-L}$	Current Limit Level at Low Line (V_{AC-RMS}=86 V)	V_{DC}=122 V, Series R=200 kΩ to HV	0.790	0.825	0.860	V
$V_{LIMIT-H}$	Current Limit Level at High Line (V_{AC-RMS}=259 V)	V_{DC}=366 V, Series R=200 kΩ to HV	0.690	0.725	0.760	V
V_{OCP-L}	OCP Trigger Level at Low Line (V_{AC-RMS}=86 V)	V_{DC}=122 V, eries R=200 kΩ to HV	0.45	0.48	0.51	V
V_{OCP-H}	OCP Trigger Level at High Line (V_{AC-RMS}=259 V)	V_{DC}=366 V, Series R=200 kΩ to HV	0.39	0.42	0.45	V
t_{SS}	Soft-start time	Startup Time	4.5	6.0	7.5	ms
t_{D-OCP}	Debounce Time for OCP	V_{SENSE}>V_{OCP}	1000	1400	1800	ms

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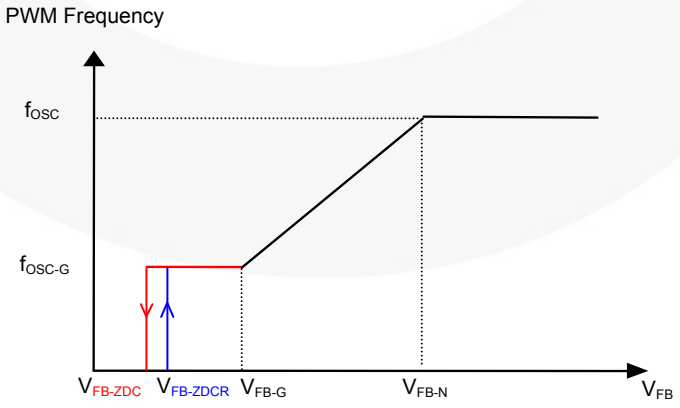

Figure 7. V_{FB} vs. PWM Frequency

Electrical Characteristics (Continued)

V_{DD}=15 V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GATE Section						
D_{MAX}	Maximum Duty Cycle		80	85	90	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15 V, I_O=50 mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12 V, I_O=50 mA	8			V
t_r	Gate Rising Time (20-80%)	V_{DD}=15 V, C_L=1 nF	60	75	90	ns
t_f	Gate Falling Time (80-20%)	V_{DD}=15 V, C_L=1 nF	15	25	35	ns
$I_{GATE-SINK}$	Gate Sink Current(7)	V_{DD}=15 V	300			mA
$I_{GATE-SOURCE}$	Gate Sourcing Current(7)	V_{DD}=15 V, GATE=6 V	250			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22 V	11.0	14.5	18.0	V
RT Section						
I_{RT}	Output Current of RT Pin		90	100	110	µA
V_{RTTH1}	Threshold Voltage for Over-Temperature Protection	0.7 V < V_{RT} < 1.05 V, After 14 ms Latch Off	1.015	1.050	1.085	V
V_{RTTH2}	Threshold Voltage for Latch Triggering	V_{RT} < 0.7 V, After 165 µs Latch Off	0.65	0.70	0.75	V
R_{OTP}	Maximum External Resistance of RT Pin to Trigger Latch Protection		9.66	10.50	11.34	kΩ
t_{D-OTP1}	Debounce Time for Over-Temperature Protection Triggering	V_{RTTH2} < V_{RT} < V_{RTTH1}	11	14	18	ms
t_{D-OTP2}	Debounce Time for Latch Triggering	V_{RT} < V_{RTTH2}	90	165	240	µs
Over-Temperature Protection Section (OTP)						
T_{OTP}	Protection Junction Temperature(5,7)		+135		°C	
$T_{Restart}$	Restart Junction Temperature(6,7)		T_{OTP}-25		°C	

Notes:
5. When activated, the output is disabled and the latch is turned off.
6. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.
7. Guaranteed by design.

Typical Performance Characteristics

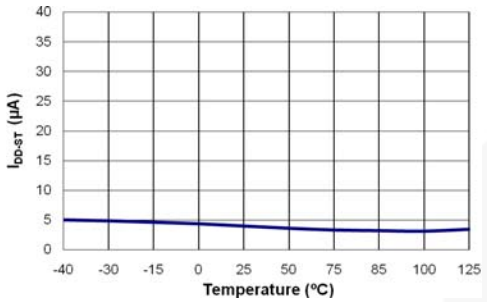

Figure 8. Startup Current (I_{DD-ST}) vs. Temperature

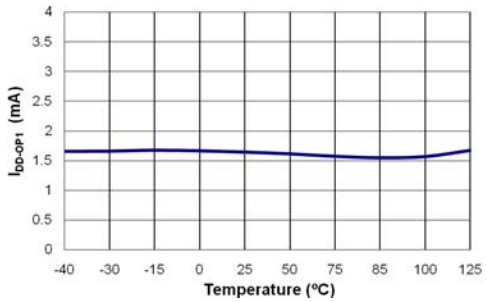

Figure 9. Operation Supply Current (I_{DD-OP1}) vs. Temperature

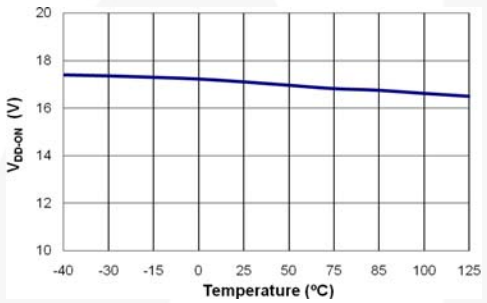

Figure 10. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

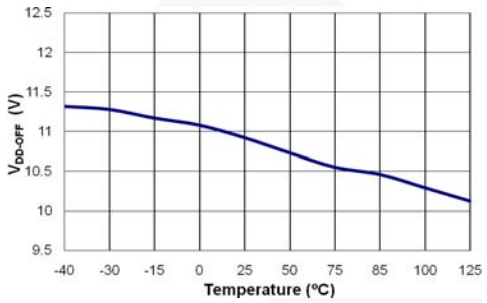

Figure 11. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

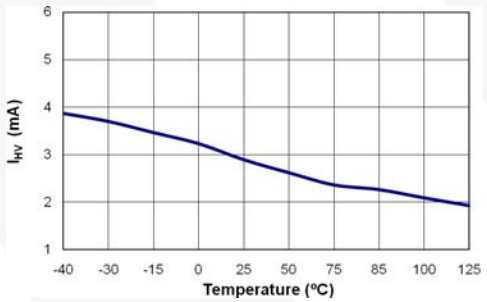

Figure 12. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

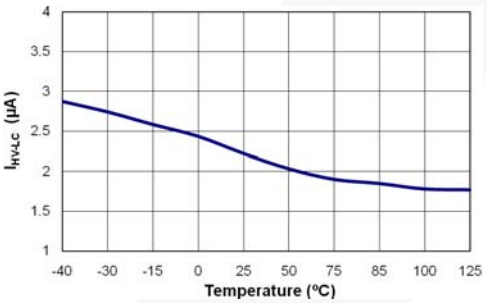

Figure 13. HV Pin Leakage Current After Startup (I_{HV-LC}) vs. Temperature

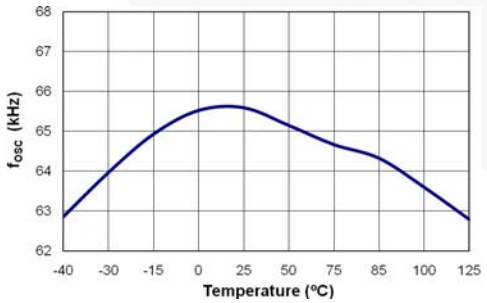

Figure 14. Frequency in Normal Mode (f_{OSC}) vs. Temperature

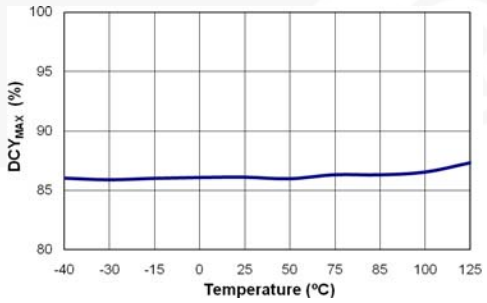

Figure 15. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Typical Performance Characteristics

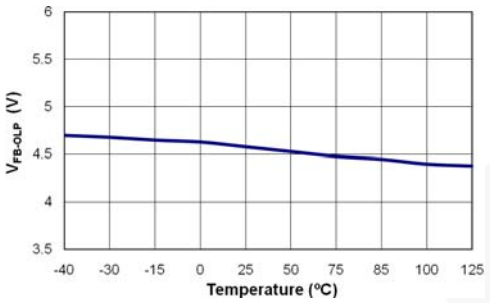

Figure 16. FB Open-Loop Trigger Level (V_{FB-OLP}) vs. Temperature

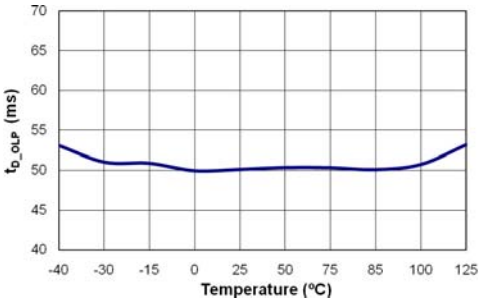

Figure 17. Delay of FB Pin Open-Loop Protection (t_{D-OLP}) vs. Temperature

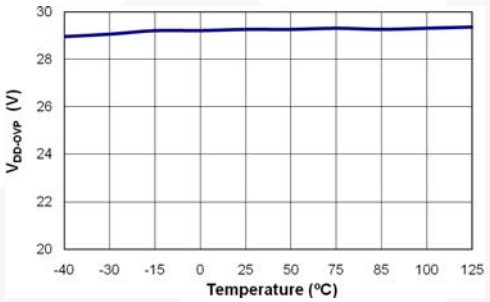

Figure 18. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

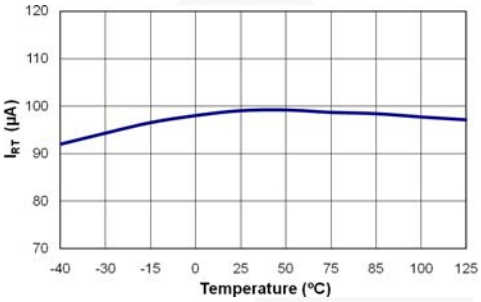

Figure 19. Output Current from RT Pin (I_{RT}) vs. Temperature

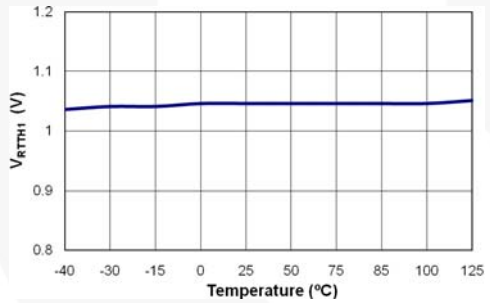

Figure 20. Over-Temperature Protection Threshold Voltage (V_{RTTH1}) vs. Temperature

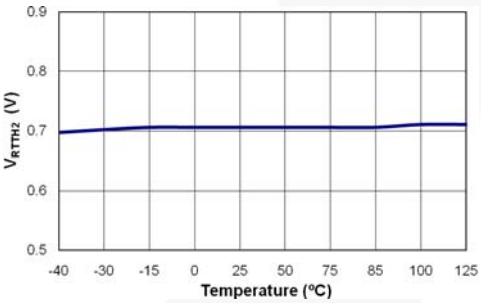

Figure 21. Over-Temperature Protection Threshold Voltage (V_{RTTH2}) vs. Temperature

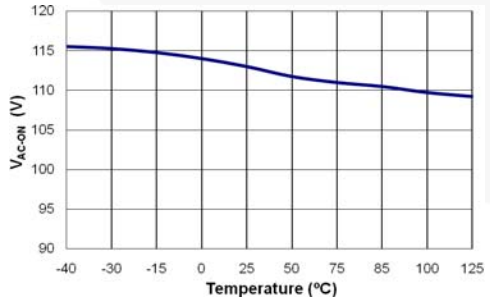

Figure 22. Brown-in (V_{AC-ON}) vs. Temperature

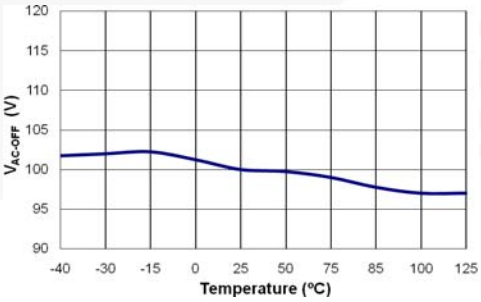

Figure 23. Brown-out (V_{AC-OFF}) vs. Temperature

Functional Description

Current Mode Control

FAN6749 employs peak current mode control, as shown in Figure 24. An opto-coupler (such as the H11A817A) and a shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

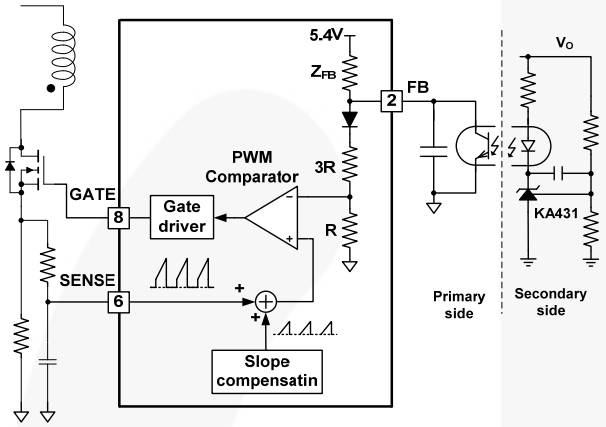

Figure 24. Current Mode Control Circuit Diagram

Green-Mode Operation

FAN6749 modulates the PWM frequency as a function of the FB voltage to improve the medium- and light-load efficiency, as shown in Figure 25. Since the output power is proportional to the FB voltage in current mode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is fixed at 65 kHz. Once V_{FB} decreases below V_{FB-N} (2.7 V), the PWM frequency starts linearly decreasing from 65 kHz to 24 kHz to reduce switching losses. As V_{FB} drops to V_{FB-G} (2.25 V), where switching frequency is decreased to 24 kHz, the switching frequency is fixed to avoid acoustic noise.

When V_{FB} falls below V_{FB-ZDC} (2.0 V) as load decreases further, FAN6749 enters Burst Mode, where PWM switching is disabled. Then the output voltage starts to drop, causing the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$ (2.1 V), switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss for lower power consumption, as shown in Figure 26

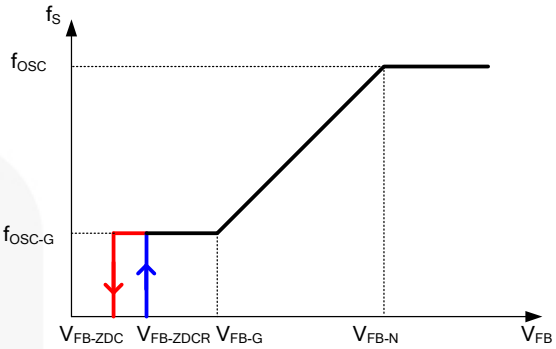

Figure 25. V_{FB} vs. PWM Frequency

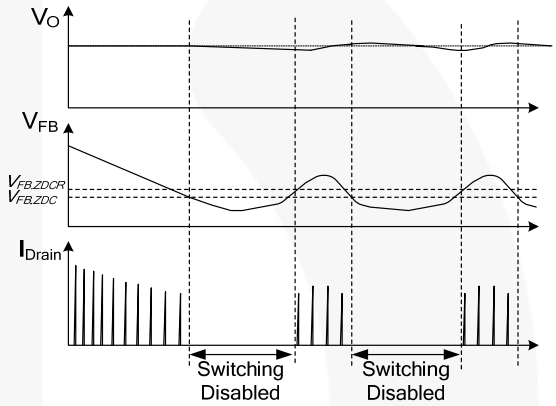

Figure 26. Burst Switching in Green Mode

Operating Current

In normal condition, operating current is around 1.8 mA (I_{DD-OP1}); when V_{FB}<1.4 V, operating current is further reduced to 1 mA (I_{DD-OP2}) by disabling several blocks of FAN6749. The low operating current improves light-load efficiency and reduces the requirement of V_{DD} hold-up capacitance.

High-Voltage Startup and Line Sensing

The HV pin is typically connected to the AC line input through an external diode and a resistor (R_{HV}), as shown in Figure 27. When AC line voltage is applied, the V_{DD} hold-up capacitor is charged by the line voltage through the diodes and resistor. After V_{DD} voltage reaches the turn-on threshold voltage (V_{DD-ON}), the startup circuit charging V_{DD} capacitor is switched off and V_{DD} is supplied by the auxiliary winding of the transformer. Once FAN6749 starts up, it continues operation until V_{DD} drops below 6.5 V (V_{UVLO}). The IC startup time with a given AC line input voltage is given as:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{AC-IN} \cdot \frac{\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{\sqrt{2}}{\pi} - V_{DD-ON}} \quad (1)$$

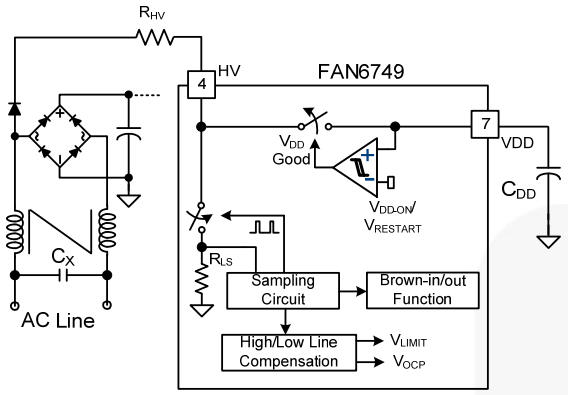

Figure 27. Startup Circuit

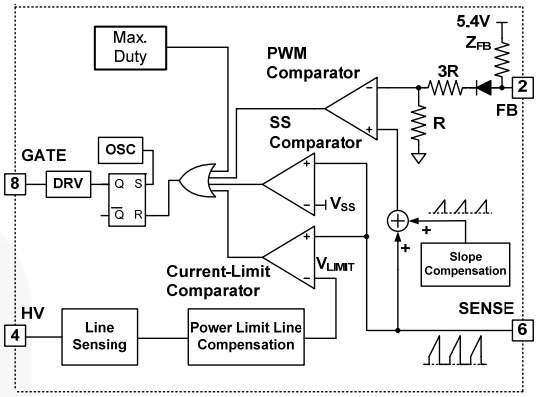

Figure 28. Cycle-by-Cycle Current-Limit Circuit

The HV pin detects the AC line voltage using a switched voltage divider that consists of external resistor (R_{HV}) and internal resistor (R_{LS}), as shown in Figure 27. The internal line-sensing circuit detects line voltage using a sampling circuit and a peak-detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize the power consumption in the light-load condition.

Based on the detected line voltage, brown-in and brown-out thresholds are determined as:

$$V_{BROWN\text{-}IN}\ (\text{RMS}) = \frac{R_{HV}}{200\text{k}} \cdot \frac{V_{AC\text{-}ON}}{\sqrt{2}} \quad (2)$$

$$V_{BROWN\text{-}OUT}\ (\text{RMS}) = \frac{R_{HV}}{200\text{k}} \cdot \frac{V_{AC\text{-}OFF}}{\sqrt{2}} \quad (3)$$

Since the internal resistor (R_{LS}=1.62 kΩ) of the voltage divider is much smaller than R_{HV}, the thresholds are given as s function of R_{HV}.

Note that V_{DD} must be larger than $V_{DD\text{-}AC}$ to start up, even though sensed line voltage satisfies Equation 2.

High/Low Line Compensation for Constant Power Limit

FAN6749 has cycle-by-cycle current limit, as shown in Figure 28, which limits the maximum input power with a given input voltage. If the output consumes beyond this maximum power, the dropping output voltage triggers the overload protection.

As shown in Figure 28, the high/low line compensation block adjusts the current limit level, V_{LIMIT}, based on the line voltage. Figure 29 shows how the cycle-by-cycle current-limit level changes with the line voltage for different R_{HV} resistors. To maintain the constant output power limit regardless of line voltage, the cycle-by-cycle current limit level, V_{LIMIT}, decreases as line voltage increases. The current-limit level is also proportional to the R_{HV} resistor value and power limit level can be tuned using different R_{HV} resistors.

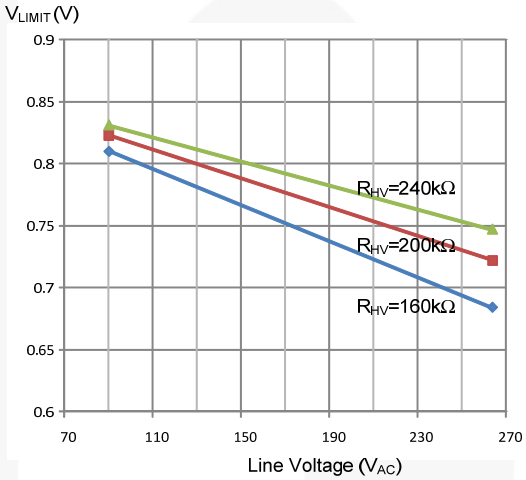

Figure 29. Current Limit vs. Line Voltage

Two-Level Over-Current Protection (OCP)

Other than cycle-by-cycle current limiting, FAN6749 applies another threshold voltage, V_{OCP}, for current sense. As shown in Figure 28, when peak of V_{SENSE} exceeds V_{OCP} at each pulse for a period of time, $t_{D\text{-}OCP}$; over-current protection (OCP) is triggered. This protection is designed for applications with surge-current outputs. If a peak load is present for less than $t_{D\text{-}OCP}$, the controller operates as usual. If the peak load continues longer than $t_{D\text{-}OCP}$, GATE output is stopped to protect the converter from overload condition.

Like V_{LIMIT}, the V_{OCP} is adjusted by high/low line compensation block to maintain a constant over-current protection level, regardless of line voltage. Figure 31 shows how V_{OCP} changes with the line voltage with different R_{HV} resistors.

When OCP is triggered, it is recommended to have V_{FB}>$V_{FB\text{-}N}$ for whole AC input range. V_{FB}>$V_{FB\text{-}N}$ ensures switching frequency is fixed at 65 kHz. If OCP is triggered in the frequency-reduction region (V_{FB}<$V_{FB\text{-}N}$), output current is reduced due to lower switching frequency. It causes the difference of OCP-triggering point between high and low AC input voltages.

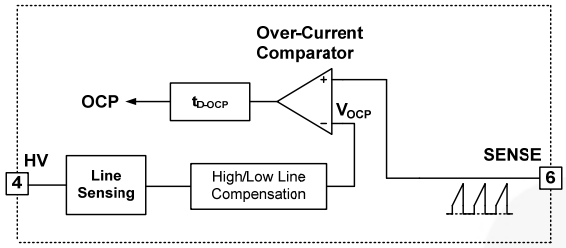

Figure 30. Over-Current Protection Circuit

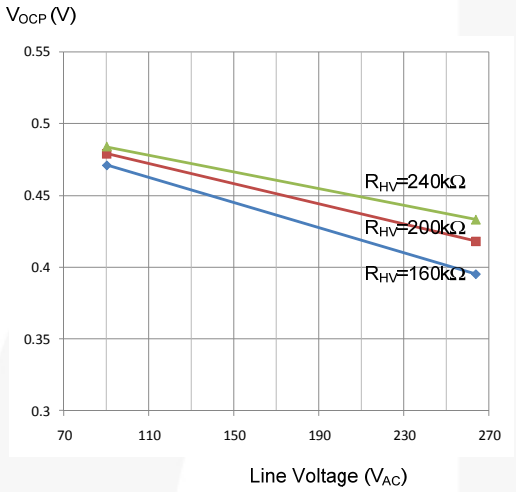

Figure 31. V_{OCP} vs. Line Voltage

Short Circuit Protection (SCP)

The V_{DD} voltage decreases every time the output of the power supply is shorted because the impedance at secondary windings becomes far lower than at auxiliary winding and currents choose the low-impedance path. When V_{FB} is larger than V_{FB-OLP} over a debounce time of t_{D-SCP}; if V_{DD} is lower than V_{DD-SCP}, PWM output is latched off.

Under-Voltage Lockout (UVLO)

As shown in Figure 32, as long as protection is not triggered, the turn-off threshold of V_{DD} is fixed internally at V_{UVLO} (6.5 V). When a protection is triggered, the V_{DD} level to terminate PWM gate switching is changed to V_{DD-OFF} (11 V), as shown in Figure 33. When V_{DD} drops below V_{DD-OFF}, the switching is terminated and the operating current from V_{DD} is reduced to I_{DD-OLP}, to slow down the discharge of V_{DD} until V_{DD} reaches V_{DD-OLP}. This delays restart after shutdown by protection to minimize the input power and voltage/current stress of switching devices during fault condition.

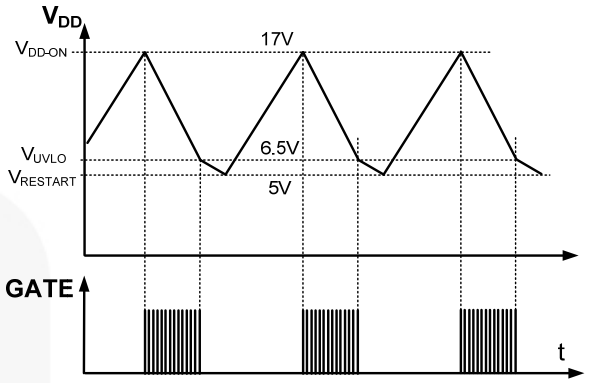

Figure 32. V_{DD} UVLO in Normal Mode

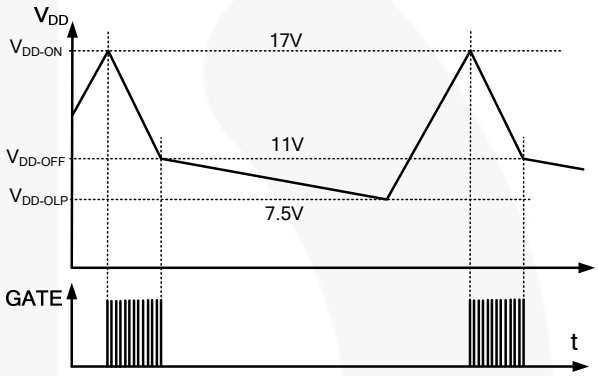

Figure 33. V_{DD} UVLO in Protection Mode

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time, t_{LEB}, is introduced. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Gate Output / Soft Driving

The BiCMOS output stage has a fast totem-pole gate driver. The output driver is clamped by an internal 14.5 V Zener diode to protect power MOSFET gate from over voltage. A soft driving is implemented to minimize electromagnetic interference (EMI) by reducing the switching noise.

V_{DD} Over-voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage from over-voltage exceeding the IC voltage rating. When the V_{DD} voltage exceeds 29 V, the protection is triggered. This protection is typically caused by an open circuit in the secondary-side feedback network.

Soft-Start

FAN6749 has an internal soft-start circuit that progressively increases the cycle-by-cycle current limit level of the MOSFET for 6 ms during startup to establish the correct working conditions for transformers and capacitors to operate.

Over-Temperature Protection (OTP)

The RT pin provides adjustable Over-Temperature Protection (OTP) and an external latch-triggering function. For OTP application, an NTC thermistor, R_{NTC}, usually in series with a resistor, R_A, is connected between the RT pin and ground. The internal current source, I_{RT}, (100 μA) introduces voltage on RT as:

$$V_{RT} = I_{RT} \cdot (R_{NTC} + R_A) \quad (4)$$

At high ambient temperature, R_{NTC} decreases, which reduces V_{RT}. When V_{RT} is lower than V_{RTTH1} (1.050 V) for longer than t_{D-OTP1} (14 ms), the protection is triggered and FAN6749 enters Latch Mode protection.

The OTP can be also trigged by pulling down the RT pin voltage using an opto-coupler or transistor. Once V_{RT} is less than V_{RTTH2} (0.7 V) for longer than t_{D-OTP2} (165 μs), the protection is triggered and FAN6749 enters Latch Mode protection.

When V_{FB} falls below 1.9 V, the RT pin function is disabled for lower power consumption. If OTP is not used, place a 100 kΩ resistor between this pin and ground to prevent noise interference.

Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6749, and increasing the power MOS gate resistance improve performance.

Physical Dimensions

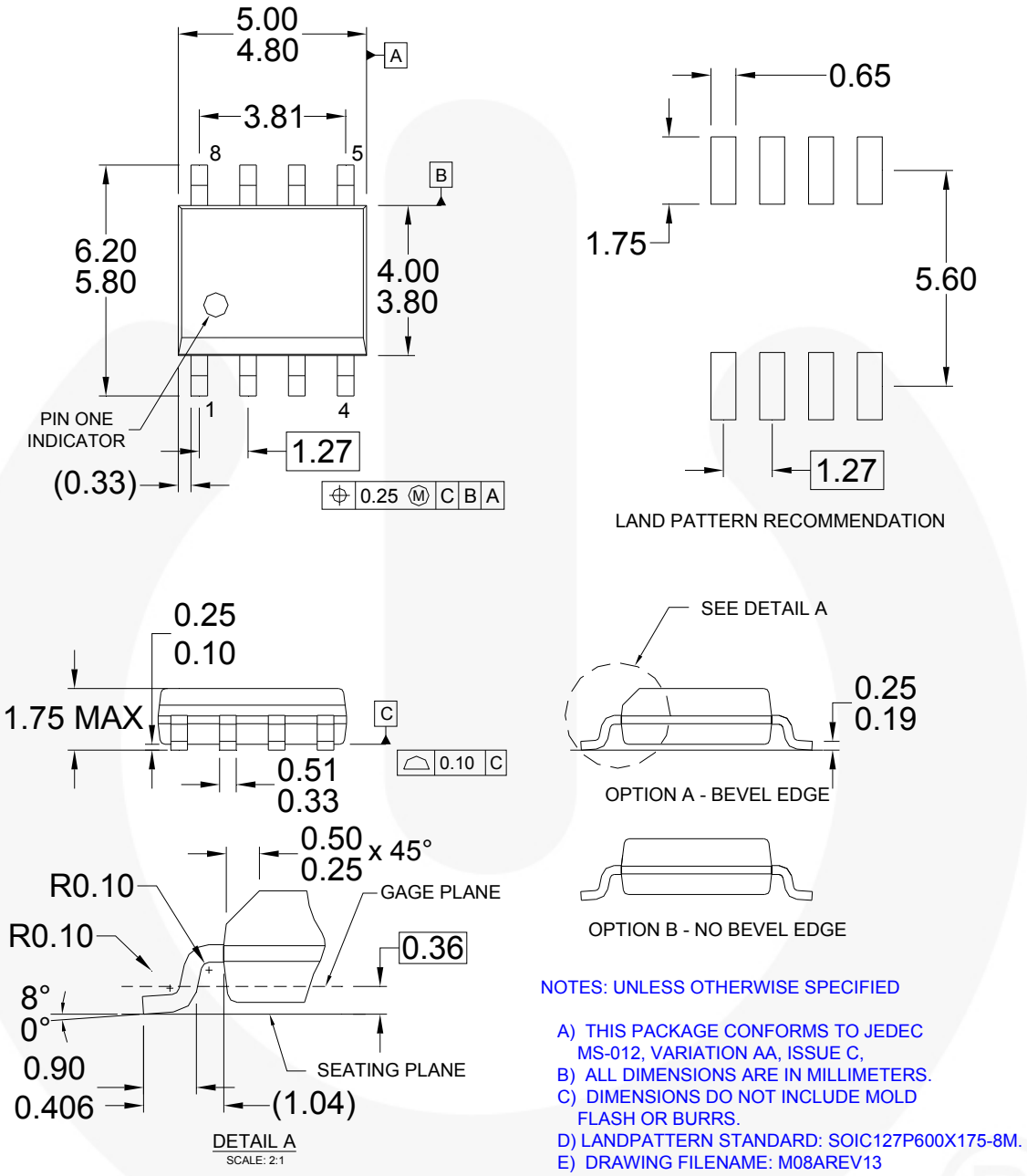

Figure 34. 8-Pin SOP-8 Package

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