FAIRCHILD SEMICONDUCTOR®

August 2012

FAN6754WA
Highly Integrated Green-Mode PWM Controller
Brownout and V_{Limit} Adjustment by HV Pin

Features

- High-Voltage Startup
- AC Input Brownout Protection with Hysteresis
- Monitor HV to Adjust V_{Limit}
- Low Operating Current: 1.5mA
- Linearly Decreasing PWM Frequency to 22KHz
- Frequency Hopping to Reduce EMI Emission
- Fixed PWM Frequency: 65KHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Internal Open-Loop Protection
- GATE Output Maximum Voltage Clamp: 13V
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)
- Internal Latch Circuit (OVP, OTP)
- Open-Loop Protection (OLP); Restart for MR, Latch for ML
- SENSE Short-Circuit Protection (SSCP)
- Built-in 8ms Soft-Start Function

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters

Description

The highly integrated FAN6754WA PWM controller provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions.

Under zero-load and very light-load conditions, FAN6754WA saves PWM pulses by entering "deep" Burst Mode. This Burst Mode function enables the power supply to meet international power conservation requirements.

FAN6754WA also integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. The built-in synchronized slope compensation helps achieve stable peak-current control. To keep constant output power limit over universal AC input range, the current limit is adjusted according to AC line voltage detected by the HV pin. The gate output is clamped at 13V to protect the external MOSFET from over-voltage damage.

Other protection functions include AC input brownout protection with hysteresis, sense pin short-circuit protection, and V_{DD} over-voltage protection. For over-temperature protection, an external NTC thermistor can be applied to sense the external switcher's temperature. When V_{DD} OVP or OTP are activated, an internal latch circuit is used to latch-off the controller. The latch mode is reset when the V_{DD} supply is removed.

FAN6754WA is available in an 8-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6754WAMRMY	-40 to +105°C	8-Pin, Small Outline Package (SOP)	Tape & Reel
FAN6754WAMLMY			

Application Diagram

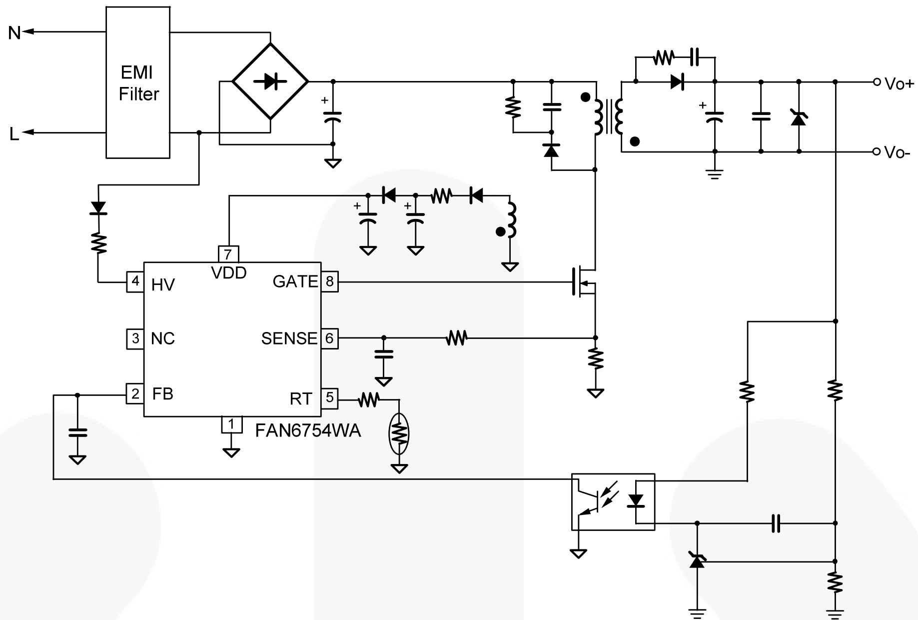


Figure 1. Typical Application

Internal Block Diagram

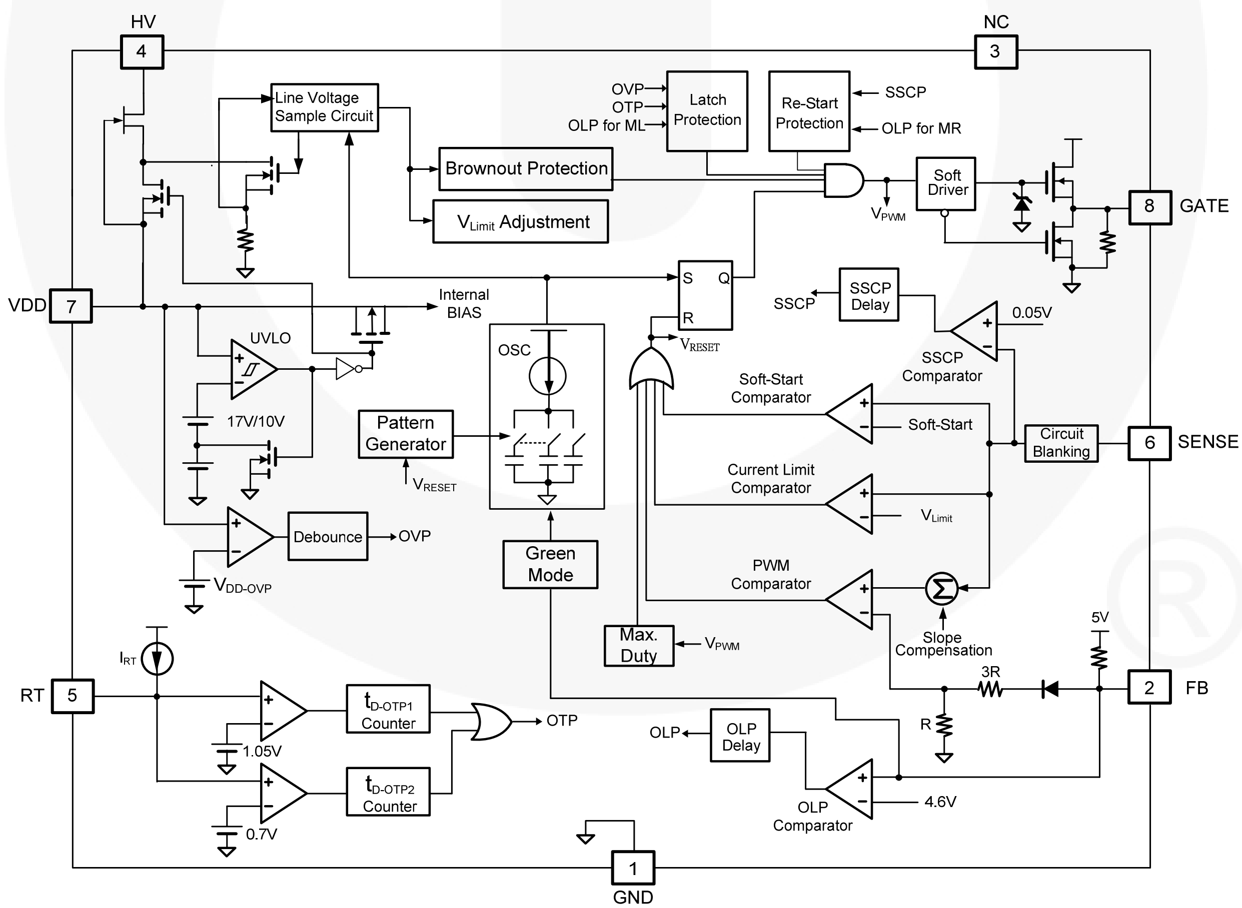
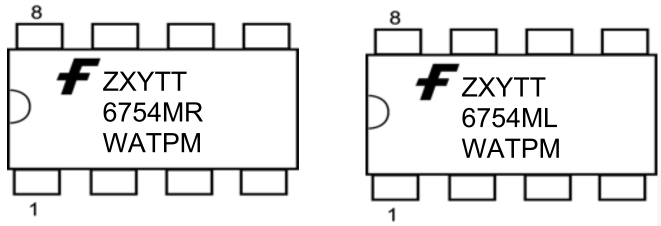


Figure 2. Functional Block Diagram

Marking Information



F - Fairchild Logo
Z - Plant Code
X - 1-Digit Year Code
Y - 1-Digit Week Code
TT - 2-Digit Die Run Code
T - Package Type (M=SOP)
P - Y: Package (Green)
M - Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

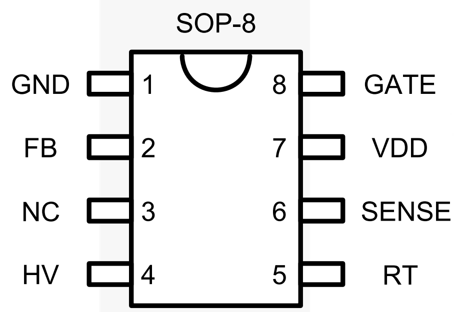


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. This pin is used for the ground potential of all the pins. A 0.1µF decoupling capacitor placed between VDD and GND is recommended.
2	FB	**Feedback**. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined by this pin and the current-sense signal from Pin 6. FAN6754WA performs open-loop protection (OLP); if the FB voltage is higher than a threshold voltage (around 4.6V) for more than 56ms, the controller latches off the PWM.
3	NC	**No Connection**
4	HV	**High-Voltage Startup**. This pin is connected to the line input via a 1N4007 and 200kΩ resistor to achieve brownout and high/low line compensation. Once the voltage on the HV pin is lower than the brownout voltage, PWM output turns off. High/low line compensation dominates the cycle-by-cycle current limiting to achieve constant output power limiting with universal input.
5	RT	**Over-Temperature Protection**. An external NTC thermistor is connected from this pin to GND. The impedance of the NTC decreases at high temperatures. Once the voltage on the RT pin drops below the threshold voltage, the controller latches off the PWM. If RT pin is not connected to NTC resistor for Over-Temperature Protection, a 100KΩ series one resistor is recommended to ground to prevent from noise interference. This pin is limited by an internal clamping circuit.
6	SENSE	**Current Sense**. This pin is used to sense the MOSFET current for the current-mode PWM and current limiting.
7	VDD	**Supply Voltage**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external bulk capacitor of typically 47µF. The threshold voltages for turn-on and turn-off are 17V and 10V, respectively. The operating current is lower than 2mA.
8	GATE	**Gate Drive Output**. The totem-pole output driver for the power MOSFET. It is internally clamped below 13V.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage[1,2]			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{SENSE}	SENSE Pin Input Voltage		-0.3	7.0	V
V_{RT}	RT Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			500	V
P_D	Power Dissipation ($T_A < 50°C$)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			150	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin	Human Body Model; JESD22-A114		5000	V
		Charged Device Model; JESD22-C101		2000	

Notes:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD with HV pin: CDM=1250V and HBM=500V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{HV}	HV Startup Resistor	150	200	250	kΩ

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				24	V
$V_{DD\text{-}ON}$	Start Threshold Voltage		16	17	18	V
$V_{DD\text{-}OFF}$	Minimum Operating Voltage		9	10	11	V
$V_{DD\text{-}OLP}$	$I_{DD\text{-}OLP}$ Off Voltage		5.5	6.5	7.5	V
$V_{DD\text{-}LH}$	Threshold Voltage on VDD Pin for Latch-Off Release Voltage		3.5	4.0	4.5	V
$V_{DD\text{-}AC}$	Threshold Voltage on VDD Pin for Disable AC Recovery to Avoid Startup Failed		$V_{DD\text{-}OFF}$ +2.8	$V_{DD\text{-}OFF}$ +3.3	$V_{DD\text{-}OFF}$ +3.8	V
$I_{DD\text{-}ST}$	Startup Current	$V_{DD\text{-}ON}$ – 0.16V			30	µA
$I_{DD\text{-}OP1}$	Operating Supply Current, PWM Operation	V_{DD}=20V, FB=3V Gate Open		1.5	2.0	mA
$I_{DD\text{-}OP2}$	Operating Supply Current, Gate Stop	V_{DD}=20V, FB=3V		1.0	1.5	mA
I_{LH}	Operating Current at PWM-Off Phase Under Latch-Off Conduction	V_{DD}=5V	30	60	90	µA
$I_{DD\text{-}OLP}$	Internal Sink Current Under Latch-Off Conduction	$V_{DD\text{-}OLP}$+0.1V	170	200	230	µA
$V_{DD\text{-}OVP}$	V_{DD} Over-Voltage Protection		24	25	26	V
$t_{D\text{-}VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		75	165	255	µs
HV Section						
I_{HV}	Supply Current from HV Pin	V_{AC}=90V(V_{DC}=120V), V_{DD}=0V	2.0	3.5	5.0	mA
$I_{HV\text{-}LC}$	Leakage Current after Startup	HV=700V, V_{DD}=$V_{DD\text{-}OFF}$+1V		1	20	µA
$V_{AC\text{-}OFF}$	Brownout Threshold	DC Source Series R=200kΩ to HV Pin *See Equation 1*	92	102	112	V
$V_{AC\text{-}ON}$	Brownin Threshold	DC Source Series R=200kΩ to HV Pin *See Equation 2*	104	114	124	V
ΔV_{AC}	$V_{AC\text{-}ON}$ - $V_{AC\text{-}OFF}$	DC Source Series R=200kΩ to HV Pin	6	12	18	V
$t_{S\text{-}CYCLE}$	Line Voltage Sample Cycle	FB > $V_{FB\text{-}N}$		220		µs
		FB < $V_{FB\text{-}G}$		650		
$t_{H\text{-}TIME}$	Line Voltage Hold Period			20		µs
$t_{D\text{-}AC\text{-}OFF}$	PWM Turn-off Debounce Time	FB > $V_{FB\text{-}N}$	65	75	85	ms
		FB < $V_{FB\text{-}G}$	180	235	290	ms

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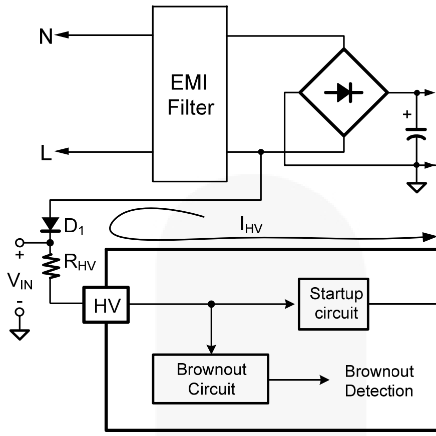

Figure 5. Brownout Circuit

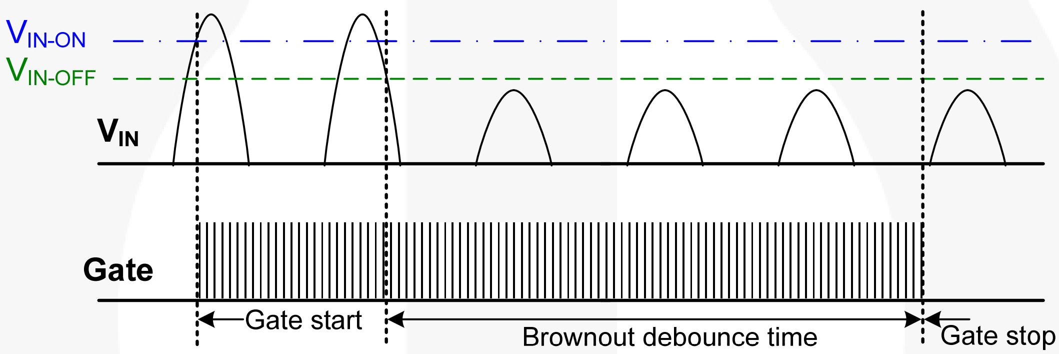

Figure 6. Brownout Behavior

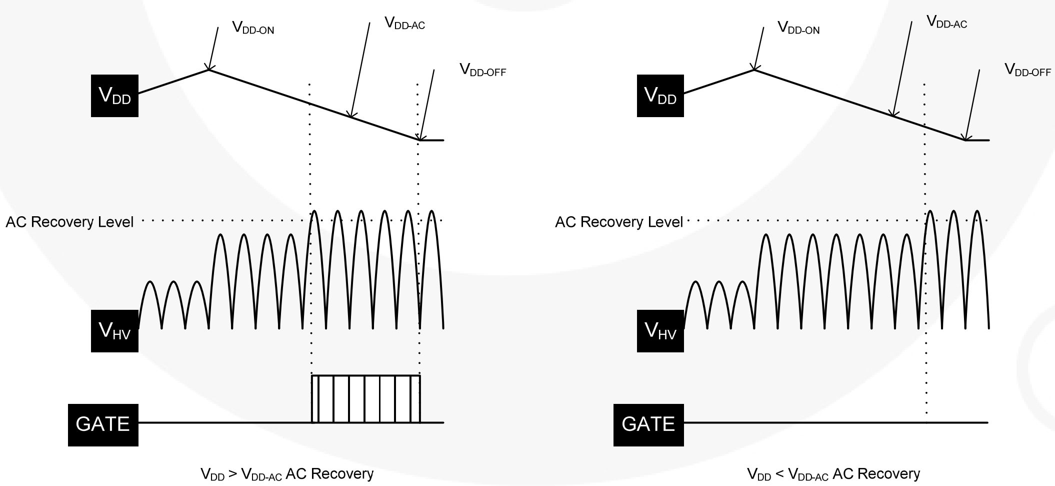

Figure 7. V_{DD-AC} and AC Recovery

Electrical Characteristics (Continued)

V_{DD}=15V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Oscillator Section						
f_{OSC}	Frequency in Normal Mode	Center Frequency	61	65	69	KHz
		Hopping Range	±3.7	±4.2	±4.7	
t_{HOP}	Hopping Period		12.0	13.5	15.0	ms
f_{OSC-G}	Green-Mode Frequency		19	22	25	KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-40 to +105°C			5	%
Feedback Input Section						
A_V	Input Voltage to Current-Sense Attenuation		1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Input Impedance		14	16	18	kΩ
$V_{FB-OPEN}$	Output High Voltage	FB Pin Open	4.8	5.0	5.2	V
V_{FB-OLP}	FB Open-Loop Trigger Level		4.3	4.6	4.9	V
t_{D-OLP}	Delay Time of FB Pin Open-Loop Protection		50	56	62	ms
V_{FB-N}	Green-Mode Entry FB Voltage	Pin, FB Voltage (FB=V_{FB-N})	2.6	2.8	3.0	V
		Hopping Range	±3.7	±4.2	±4.7	kHz
V_{FB-G}	Green-Mode Ending FB Voltage	Pin, FB Voltage (FB=V_{FB-G})	2.1	2.3	2.5	V
		Hopping Range	±1.27	±1.45	±1.62	kHz
$V_{FB-ZDCR}$	FB Threshold Voltage for Zero-Duty Recovery		1.9	2.1	2.3	V
V_{FB-ZDC}	FB Threshold Voltage for Zero-Duty		1.8	2.0	2.2	V

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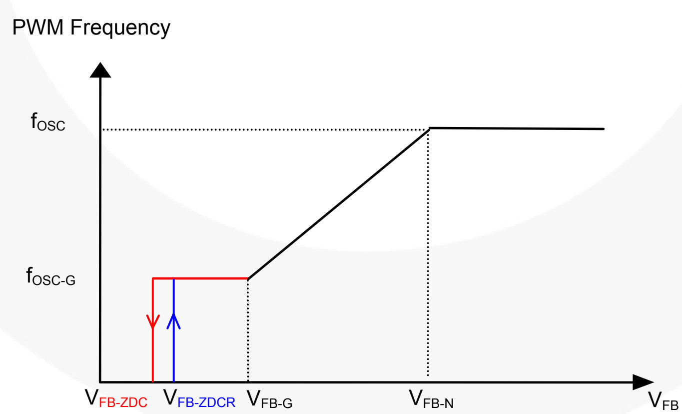

Figure 8. V_{FB} vs. PWM Frequency

Electrical Characteristics (Continued)

V_{DD}=15V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Current-Sense Section						
t_{PD}	Delay to Output			100	250	ns
t_{LEB}	Leading-Edge Blanking Time		230	280	330	ns
$V_{Limit-L}$	Current Limit at Low Line (V_{AC}=86V)	V_{DC}=122V, Series R=200kΩ to HV	0.43	0.46	0.49	V
$V_{Limit-H}$	Current Limit at High Line (V_{AC}=259V)	V_{DC}=366V, Series R=200kΩ to HV	0.36	0.39	0.42	V
V_{SSCP}	Threshold Voltage for SENSE Short-Circuit Protection		0.03	0.05	0.07	V
$t_{ON-SSCP}$	On Time for V_{SSCP} Checking		4.0	4.4	4.8	μs
t_{D-SSCP}	Delay for SENSE Short-Circuit Protection	V_{SENSE}<0.05V	60	120	180	μs
t_{SS}	Soft-Start Time	Startup Time	7	8	9	ms
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		86	89	92	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V, I_O=50mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12V, I_O=50mA	8			V
$I_{GATE-SINK}$	Gate Sink Current(4)	V_{DD}=15V	300			mA
$I_{GATE-SOURCE}$	Gate Source Current(4)	V_{DD}=15V, GATE=6V	250			mA
t_r	Gate Rising Time	V_{DD}=15V, C_L=1nF		100		ns
t_f	Gate Falling Time	V_{DD}=15V, C_L=1nF		50		ns
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V	9	13	17	V
RT Section						
I_{RT}	Output Current from RT Pin		92	100	108	μA
V_{RTTH1}	Over-Temperature Protection Threshold Voltage	0.7V < V_{RT} < 1.05V, after 12ms Latch Off	1.000	1.035	1.070	V
V_{RTTH2}		V_{RT} < 0.7V, After 100μs Latch Off	0.65	0.70	0.75	
t_{D-OTP1}	Over-Temperature Latch-Off Debounce	V_{RTTH2} < V_{RT} < V_{RTTH1} FB > V_{FB-N}	14	16	18	ms
		V_{RTTH2} < V_{RT} < V_{RTTH1} FB < V_{FB-G}	40	51	62	
t_{D-OTP2}		V_{RT}< V_{RTTH2}, FB > V_{FB-N}	110	185	260	μs
		V_{RT}< V_{RTTH2}, FB < V_{FB-G}	320	605	890	

Note:
4. Guaranteed by design.

Typical Performance Characteristics

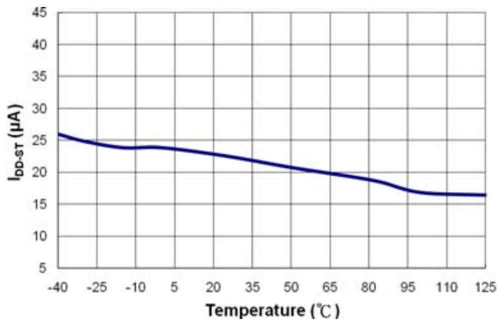

Figure 9. Startup Current (I_{DD-ST}) vs. Temperature

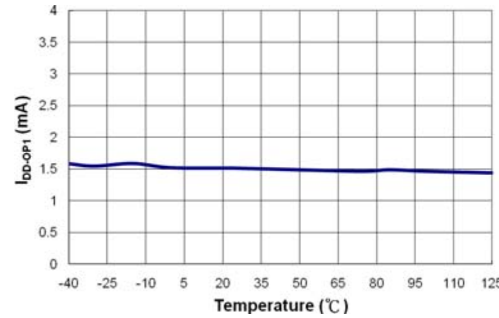

Figure 10. Operation Supply Current (I_{DD-OP1}) vs. Temperature

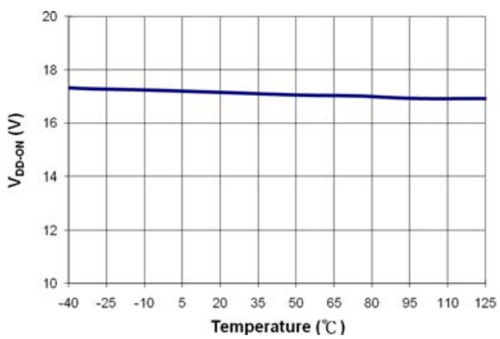

Figure 11. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

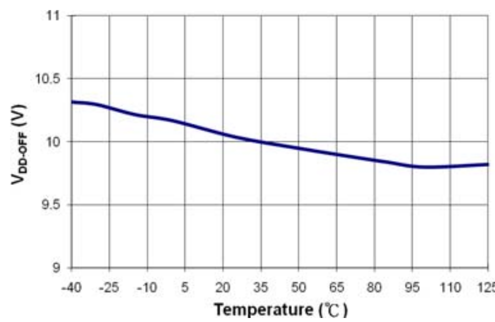

Figure 12. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

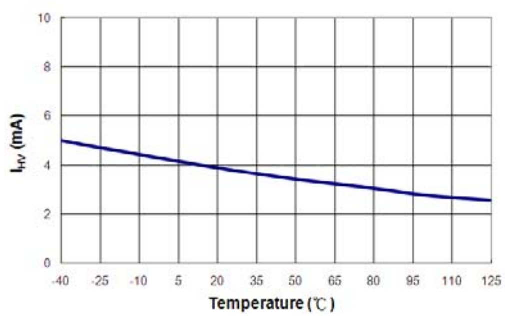

Figure 13. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

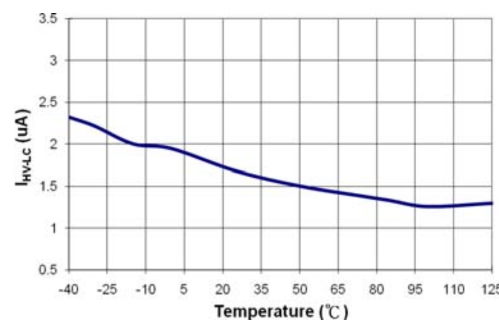

Figure 14. HV Pin Leakage Current After Startup (I_{HV-LC}) vs. Temperature

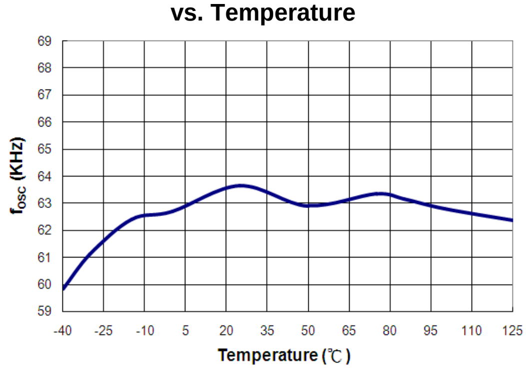

Figure 15. Frequency in Normal Mode (f_{OSC}) vs. Temperature

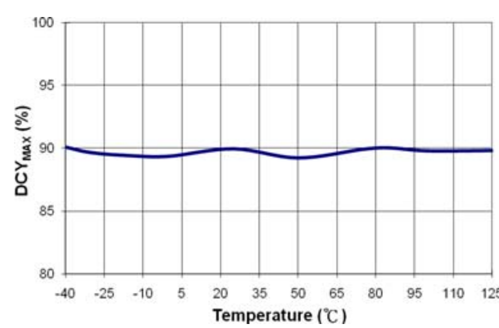

Figure 16. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Typical Performance Characteristics (Continued)

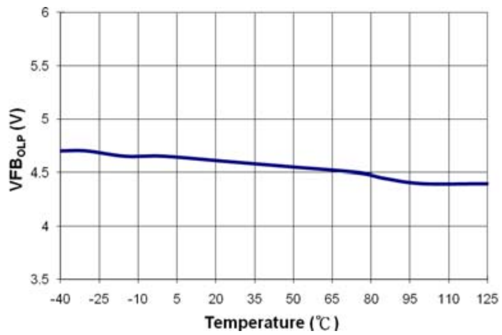

Figure 17. FB Open-Loop Trigger Level ($V_{FB\text{-}OLP}$) vs. Temperature

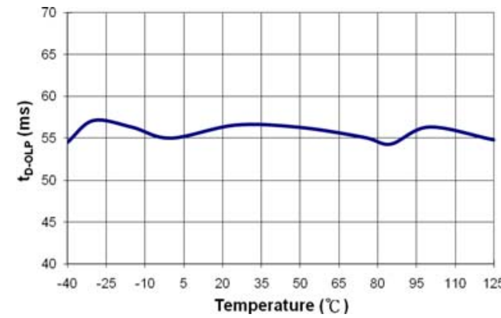

Figure 18. Delay Time of FB Pin Open-Loop Protection ($t_{D\text{-}OLP}$) vs. Temperature

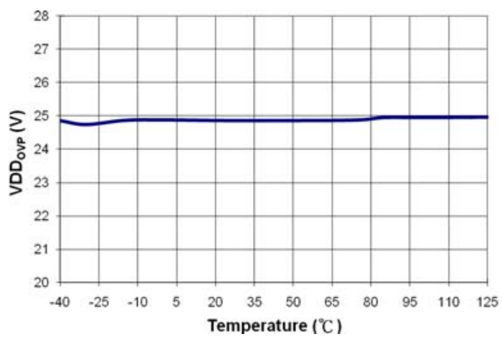

Figure 19. V_{DD} Over-Voltage Protection ($V_{DD\text{-}OVP}$) vs. Temperature

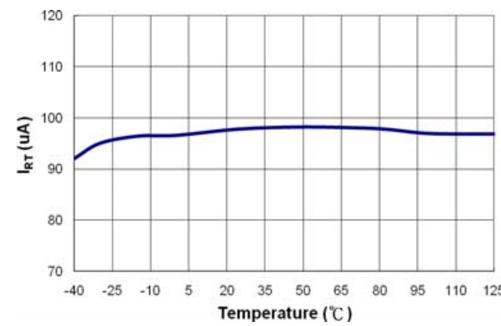

Figure 20. Output Current from RT Pin (I_{RT}) vs. Temperature

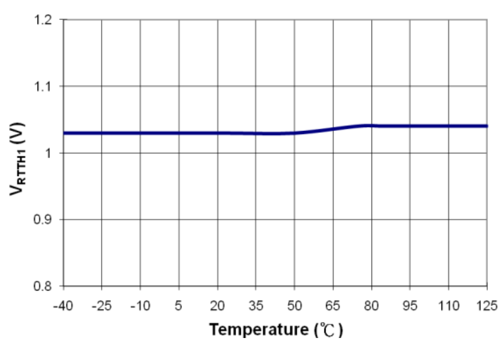

Figure 21. Over-Temperature Protection Threshold Voltage (V_{RTTH1}) vs. Temperature

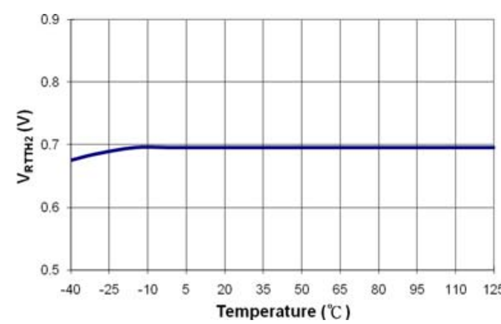

Figure 22. Over-Temperature Protection Threshold Voltage (V_{RTTH2}) vs. Temperature

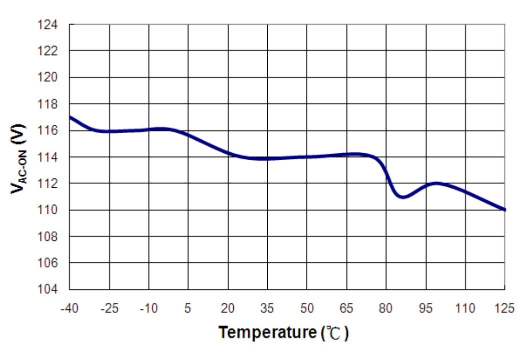

Figure 23. Brownin ($V_{AC\text{-}ON}$) vs. Temperature

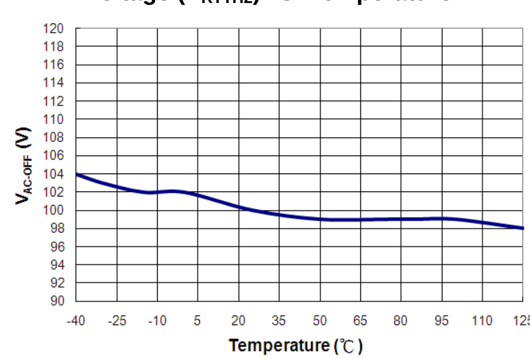

Figure 24. Brownout ($V_{AC\text{-}OFF}$) vs. Temperature

Functional Description

Startup Current

For startup, the HV pin is connected to the line input through an external diode and resistor; R_{HV}, (1N4007 / 200KΩ recommended). Peak startup current drawn from the HV pin is $(V_{AC} \times \sqrt{2}) / R_{HV}$ and charges the hold-up capacitor through the diode and resistor. When the V_{DD} capacitor level reaches $V_{DD\text{-}ON}$, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6754WA to keep the V_{DD} until the auxiliary winding of the main transformer provides the operating current.

Operating Current

Operating current is around 1.5mA. The low operating current enables better efficiency and reduces the requirement of V_{DD} hold-up capacitance.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to reduce the switching frequency in light-load and no-load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage ($V_{FB\text{-}N}$), the switching frequency is continuously decreased to the minimum green-mode frequency of around 22KHz.

Current Sensing / PWM Current Limiting

Peak-current-mode control is utilized to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current-sense signal and V_{FB}, the feedback voltage. When the voltage on the SENSE pin reaches around $V_{COMP} = (V_{FB}–0.6)/4$, the switch cycle is terminated immediately. V_{COMP} is internally clamped to a variable voltage around 0.46V for low-line output power limit.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 17V and 10V, respectively. During startup, the hold-up capacitor must be charged to 17V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} until the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10V during startup. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 13V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

Soft-Start

For many applications, it is necessary to minimize the inrush current at startup. The built-in 8ms soft-start circuit significantly reduces the startup current spike and output voltage overshoot.

Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and cycle-by-cycle current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. FAN6754WA inserts a synchronized, positive-going, ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage across sense resistor R_{SENSE} reaches the threshold voltage, around 0.46V for low-line condition, the output GATE drive is turned off after a small delay, t_{PD}. This delay introduces an additional current proportional to $t_{PD} \bullet V_{IN} / L_P$. Since the delay is nearly constant regardless of the input voltage V_{IN}, higher input voltage results in a larger additional current and the output power limit is higher than under low input line voltage. To compensate this variation for a wide AC input range, a power-limiter is controlled by the HV pin to solve the unequal power-limit problem. The power limiter is fed to the inverting input of the current limiting comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

Brownout and Constant Power Limited by the HV Pin

Unlike previous PWM controllers, FAN6754WA's HV pin can detect the AC line voltage brownout function and adjust the current limit. Using a fast diode and startup resistor to sample the AC line voltage, the peak value refreshes and is stored in a register at each sampling cycle. When internal update time is met, this peak value is used for brownout and current-limit level judgment. Equation 1 and 2 calculate the level of brown-in or brownout converted to RMS value. For power saving, FAN6754WA enlarges the sampling cycle to lower the power loss from HV sampling at light-load condition.

$$V_{AC\text{-}ON}(RMS) = \left(0.9V \times \frac{(R_{HV}+1.6)}{1.6}\right) / \sqrt{2} \quad (1)$$

$$V_{AC\text{-}OFF}(RMS) = \left(0.81V \times \frac{(R_{HV}+1.6)}{1.6}\right) / \sqrt{2} \quad (2)$$

where R_{HV} is in kΩ.

The HV pin can perform current limit to shrink the tolerance of Over-Current Protection (OCP) under full range of AC voltage, to linearly current limit curve, as shown in Figure 25. FAN6754WA also shrinks the V_{limit} level by half to lower the I^2R_{SENSE} loss to increase the heavy-load efficiency.

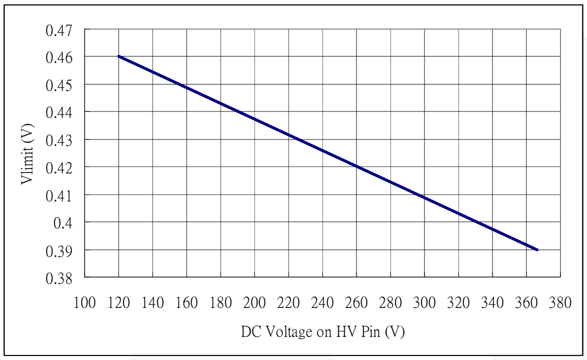

Figure 25. Linearly Current Limit Curve

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents damage due to abnormal conditions. If the V_{DD} voltage is over the over-voltage protection voltage (V_{DD-OVP}) and lasts for $t_{D-VDDOVP}$, the PWM pulses are disabled until V_{DD} drops below the UVLO, then starts again. Over-voltage conditions are usually caused by open feedback loops.

Sense-Pin Short-Circuit Protection

The FAN6754WA provides safety protection for Limited Power Source (LPS) tests. When the sense resistor is shorted by soldering during production, the pulse-by-pulse current limiting loses efficiency for the purpose of providing over-power protection for the unit. The unit may be damaged when the loading is larger than the maximum load. To protect against a short circuit across the current-sense resistor, the controller is designed to immediately shut down if a continuously low voltage (around 0.05V/120µs) on the SENSE pin is detected.

Thermal Protection

An NTC thermistor, R_{NTC}, in series with resistor R_A, can be connected from the RT pin to ground. A constant current, I_{RT}, is output from the RT pin. The voltage on the RT pin can be expressed as $V_{RT}=I_{RT} \bullet (R_{NTC} + R_{PTC})$, where I_{RT} is 100µA. At high ambient temperature, R_{NTC} is smaller, such that V_{RT} decreases. When V_{RT} is less than 1.035V (V_{RTTH1}), the PWM turns off after 16ms (t_{D-OTP1}). If V_{RT} is less than 0.7V (V_{RTTH2}), the PWM turns off after 185µs (t_{D-OTP2}). If the RT pin is not connected to NTC resistor for over-temperature protection, connecting a series one 100KΩ・ resistor to ground to prevent from noise interference is recommended. This pin is limited by an internal clamping circuit.

Limited Power Control

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned off, V_{DD} begins decreasing.

When V_{DD} goes below the turn-off threshold (10V) the controller is totally shut down and V_{DD} is continuously discharged to V_{DD-OLP} (6.5V) by I_{DD-OLP} to lower the average input power. This is called two-level UVLO. V_{DD} is cycled again. This protection feature continues as long as the overloading condition persists. This prevents the power supply from overheating due to overloading conditions.

Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6754WA, and increasing the power MOS gate resistance improve performance.

Physical Dimensions

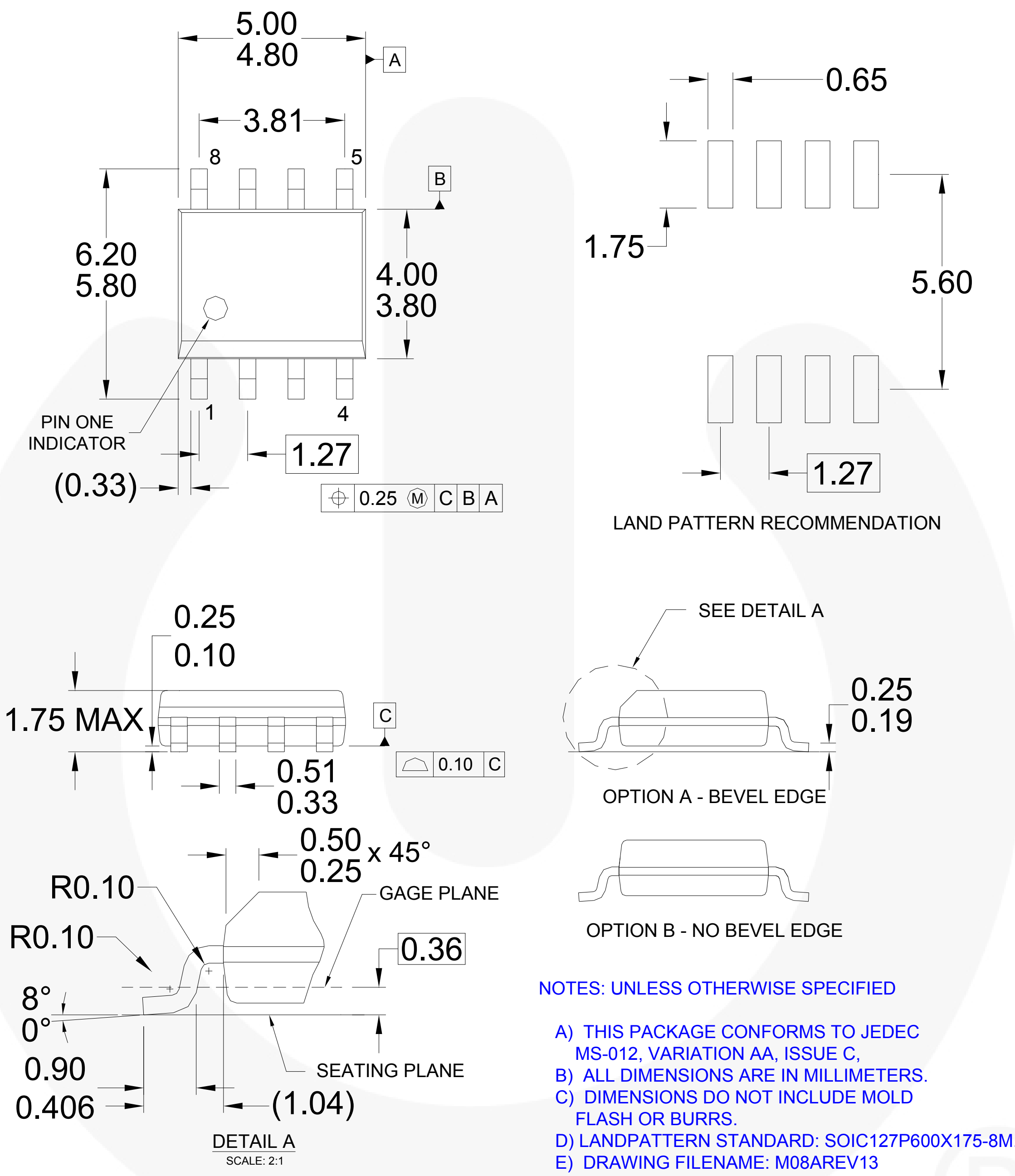

Figure 26. 8-Pin Small Outline Package (SOP) Package

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