

FAN7081_GF085 High Side Gate Driver

Features

- Automotive qualified to AEC Q100
- Floating channel designed for bootstrap operation up to +600V
- Tolerance to negative transient voltage on VS pin
- Common mode dV/dt noise cancelling circuit.
- Gate drive supply range from 10V to 20V
- Under-voltage lockout
- CMOS Schmit-triggered inputs with pull-up
- High side output out of phase with input (Inverted input)
- 8-Lead Small Outline Package (SO 8L NB)

Typical Applications

- Diesel and gasoline Injectors/Valves
- Common rail injection systems
- MOSFET-and IGBT high side driver applications
- Automotive motor and solenoid drivers

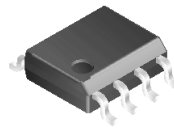


For Fairchild's definition of "green" Eco Status, please visit:
http://www.fairchildsemi.com/company/green/rohs_green.html

Description

The FAN7081_GF085 is a high-side gate drive IC designed for high voltage and high speed driving of MOSFET or IGBT, which operate up to 600V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to $V_S = -5V$ (typical) at $V_{BS} = 15V$. Logic input is compatible with standard CMOS outputs. The UVLO circuits prevent malfunction when VCC and VBS are lower than the specified threshold voltage. It is available in a space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250mA and 500mA respectively, which is suitable for magnetic- and piezo type injectors and general MOSFET/IGBT based high side driver applications.

SO 8L NB

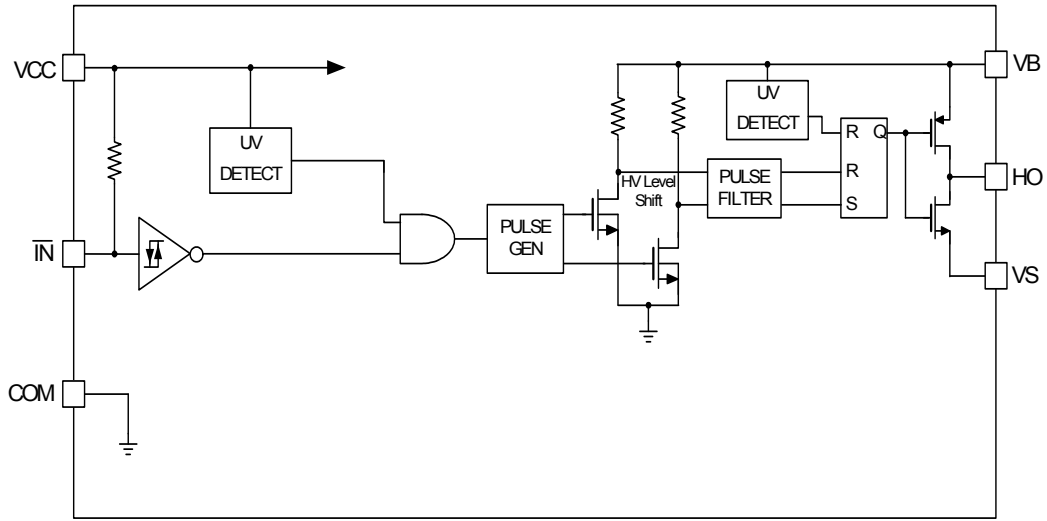


Ordering Information

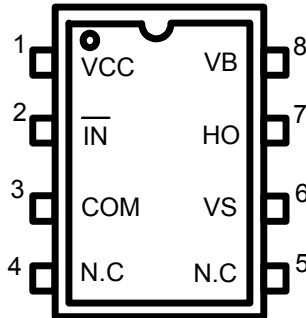
Device	Package	Operating Temp.
FAN7081M_GF085	SO 8L NB	-40 °C ~ 125 °C
FAN7081MX_GF085	SO 8L NB	-40 °C ~ 125 °C

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	VCC	P	Driver supply voltage
2	$\overline{\text{IN}}$	I	Logic input for high side gate drive output, out of phase with HO
3	COM	P	Ground
4	NC	-	NC
5	NC	-	NC
6	VS	P	High side floating offset for MOSFET Source connection
7	HO	A	High side drive output for MOSFET Gate connection
8	VB	P	Driver output stage supply

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Parameter	Symbol	Min.	Max.	Unit
High side floating supply offset voltage	VS	VB-25	VB+0.3	V
High side floating supply voltage	VB	-0.3	625	V
High side floating output voltage	VHO	VS-0.3	VB+0.3	V
Supply voltage	VCC	-0.3	25	V
Input voltage for $\overline{\text{IN}}$	VIN	-0.3	VCC+0.3	V
Power Dissipation ¹⁾	Pd		0.625	W
Thermal resistance, junction to ambient ¹⁾	Rthja		200	°C/W
Electrostatic discharge voltage (Human Body Model)	V _{ESD}	1K		V
Charge device model	V _{CDM}	500		V
Junction Temperature	T _J		150	°C
Storage Temperature	T _S	-55	150	°C

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural codition(StillAir)

JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operations the device should be used within the recommended conditions. $-40^{\circ}\text{C} \leq \text{Ta} \leq 125^{\circ}\text{C}$

Parameter	Symbol	Min.	Max.	Unit
High side floating supply voltage(DC) Transient:-10V@ 0.2 us	VB	VS + 10	VS + 20	V
High side floating supply offset voltage(DC)	VS	-4 (@VBS >= 10V) -5 (@VBS >= 11.5V)	600	V
High side floating supply offset voltage(Transient)	VS	-25 (~200ns) -20(200ns ~240ns) -7(240ns~400ns)	600	V
High side floating output voltage	VHO	VS	VB	V
Allowable offset voltage Slew Rate ¹⁾	dv/dt	-	50	V/ns
Supply voltage	VCC	10	20	V
Input voltage for $\overline{\text{IN}}$	VIN	0	Vcc	V
Switching Frequency ²⁾	Fs		200	KHz
Ambient Temperature	Ta	-40	125	°C

Note: 1) Guaranteed by design.

2) Duty = 0.5

Statics Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_S = 0\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vcc and VBS supply Characteristics						
VCC and VBS supply under voltage positive going threshold	VCCUV+ VBSUV+		-	8.7	9.8	V
VCC and VBS supply under voltage negative going threshold	VCCUV- VBSUV-		7.4	8.2	-	V
VCC and VBS supply under voltage hysteresis	VCCUVH VBSUVH	-	0.2	0.5	-	V
Under voltage lockout response time	tduvcc tduvbs	VCC: 10V-->7.3V or 7.3V-->10V VBS: 10V-->7.3V or 7.3V-->10V	0.5 0.5		20 20	us us
Offset supply leakage current	ILK	$V_B = V_S = 600\text{V}$	-	-	50	μA
Quiescent VBS supply current	IQBS	$V_{IN} = 0$	-	23	250	μA
Quiescent Vcc supply current	IQCC1	$V_{IN} = 0\text{V}$	-	42	120	μA
Quiescent Vcc supply current	IQCC2	$V_{IN} = 15\text{V}$	-	25	100	μA
Input Characteristics						
High logic level input voltage	V_{IH}		$0.63V_{CC}$	-	-	V
Low logic level input voltage	V_{IL}		-	-	$0.4V_{CC}$	V
Low logic level input bias current for IN	I_{IN+}	$V_{IN} = 0$	-	15	50	μA
High logic level input bias current for IN	I_{IN-}	$V_{IN} = 15\text{V}$	-	0	1	μA
Output characteristics						
High level output voltage, $V_{BIAS-VO}$	V_{OH}	$I_O = 0$	-	-	0.1	V
Low level output voltage, V_O	V_{OL}	$I_O = 0$	-	-	0.1	V
Peak output source current	I_{O1+}		250	-	-	mA
Peak output sink current	I_{O1-}		500	-	-	mA
Equivalent output resistance	ROP			40	60	Ω
	RON			20	30	Ω

Note: The input parameter are referenced to COM. The VO and IO parameters are referenced to COM.

Dynamic Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $V_{BS} = 15\text{V}$, $V_S = 0\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input-to-output turn-on propagation delay	t _{plh}	50% input level to 10% output level, V _S = 0V		130	300	ns
Input-to-output turn-off propagation delay	t _{phl}	50% input level to 90% output level V _S = 0V	-	140	300	ns
Output rising time	t _{r1}	10% to 90%, T _j =25°C, V _{BS} =15V	-	15	400	ns
	t _{r2}	10% to 90%		-	500	ns
Output falling time	t _{f1}	90% to 10%, T _j =25°C, V _{BS} =15V	-	10	150	ns
	t _{f2}	90% to 10%		-	500	ns

Application Information

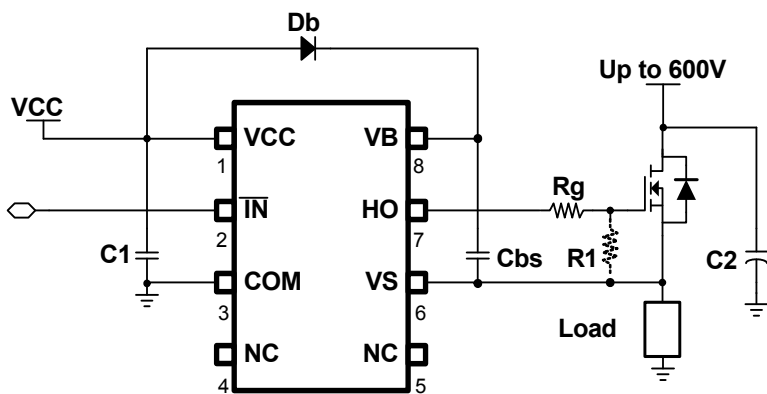
1. Relationship in input/output and supplies

Table.1 Truth table for Vcc, VBS, VIN, and VHO			
VCC	VBS	IN	HO
< VCCUVLO-	X	X	OFF
X	< VBSUVLO-	X	OFF
X	X	HIGH	OFF
> VCCUVLO+	> VBSUVLO+	LOW	ON

Notes:

X means independent from signal

Typical Application Circuit



Typical Waveforms

1. Input/Output Timing

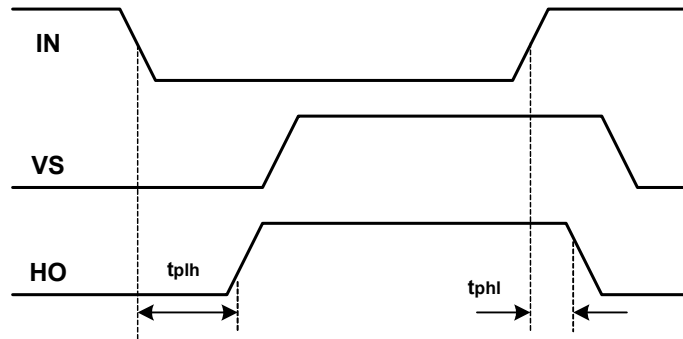


Figure 1. Input /output Timing Diagram

2. Output(HO) Switching Timing

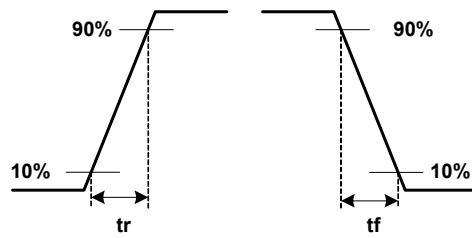


Figure 2. Switching Time Waveform Definitions

3. VB Drop Voltage Diagram

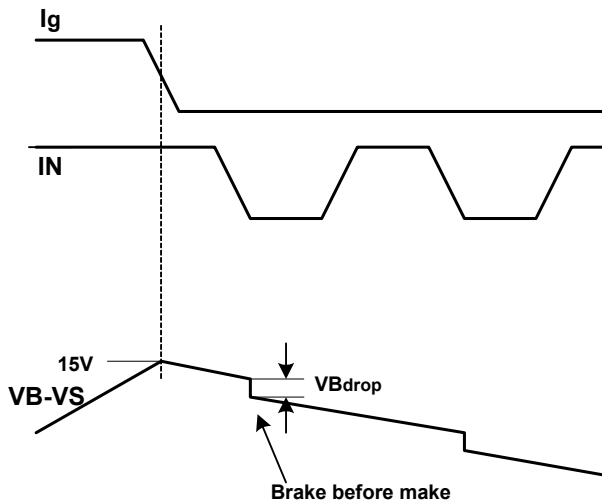


Figure 3a. VB Drop Voltage Diagram

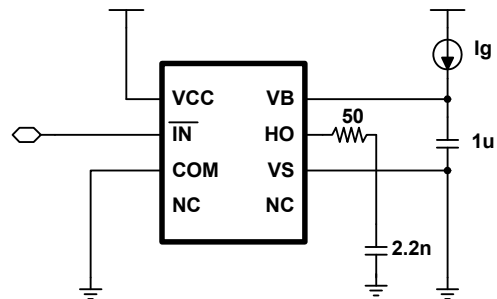


Figure3b. VB Drop Voltage Test Circuit

Performance Graphs

This performance graphs based on ambient temperature -40°C ~125°C

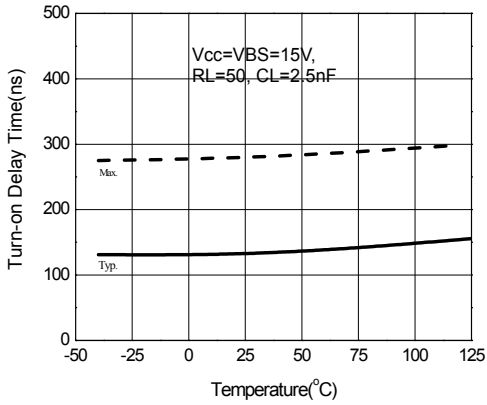


Figure 4a. Turn-On Delay Time vs Temperature

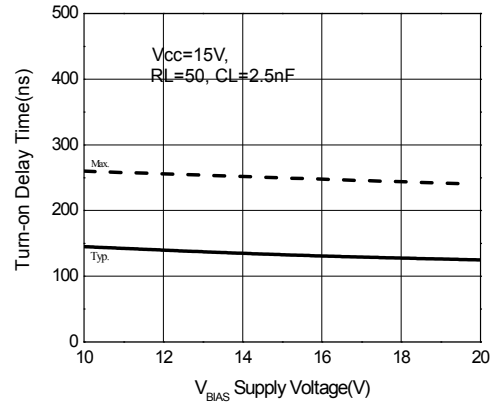


Figure 4b. Turn-On Delay Time vs VBS Supply Voltage

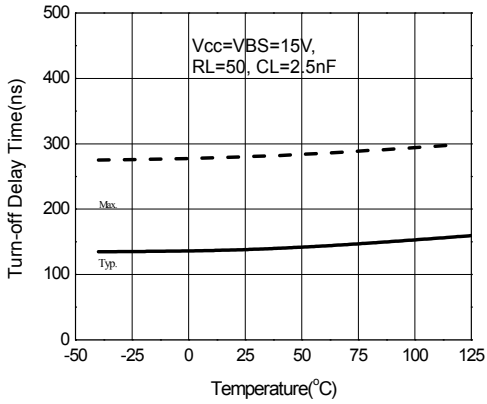


Figure 5a. Turn-Off Delay Time vs Temperature

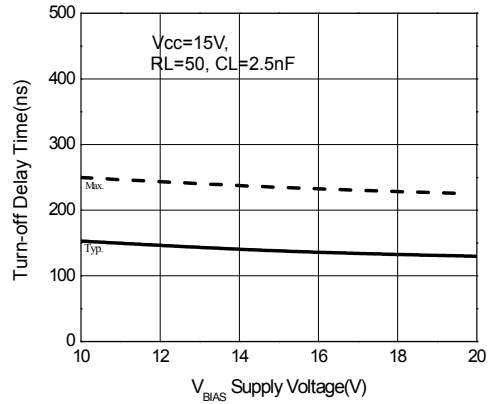


Figure 5b. Turn-Off Delay Time vs VBS Supply Voltage

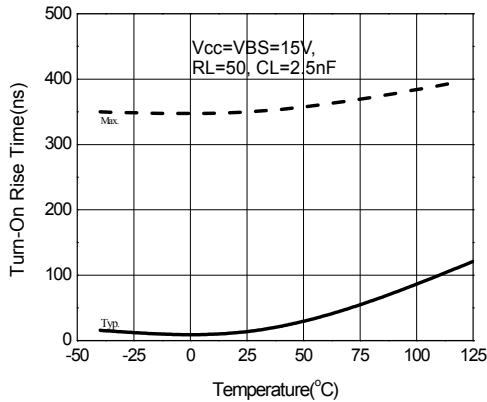


Figure 6a. Turn-On Rising Time vs Temperature

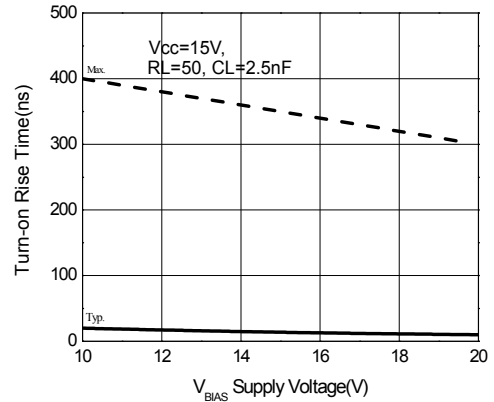


Figure 6b. Turn-ON Rising Time vs VBS Supply Voltage

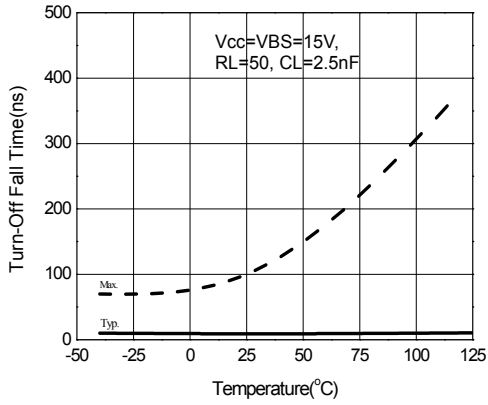


Figure 7a. Turn-Off Falling Time vs Temperature

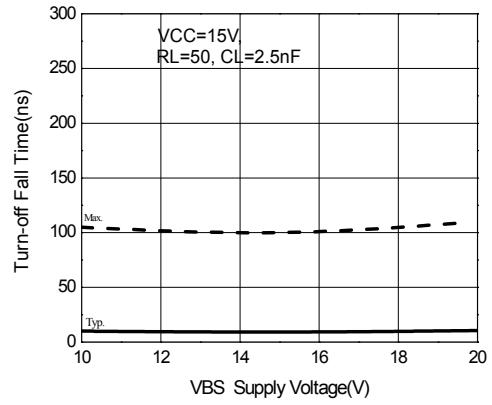


Figure 7b. Turn-Off Falling Time vs VBS Supply Voltage

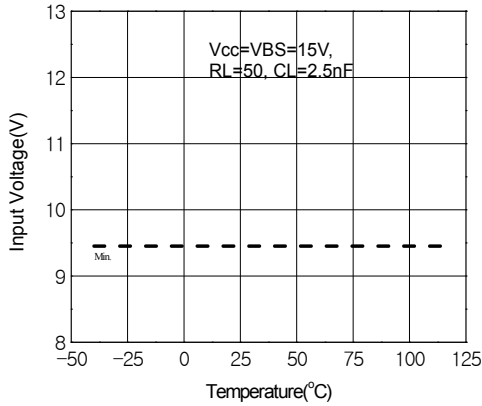


Figure 8a. Logic "1" IN Voltage vs Temperature

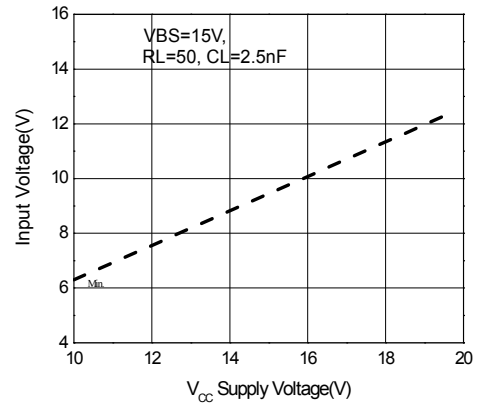


Figure 8b. Logic "1" IN Voltage vs VCC Supply Voltage

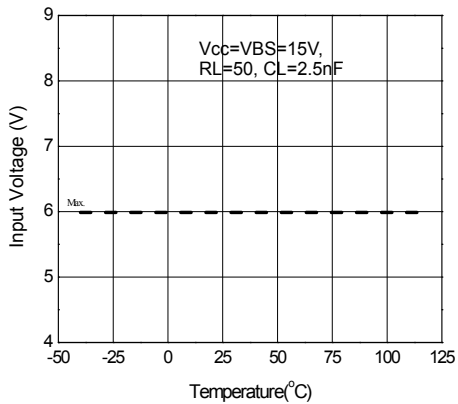


Figure 9a. Logic "0" IN Voltage vs Temperature

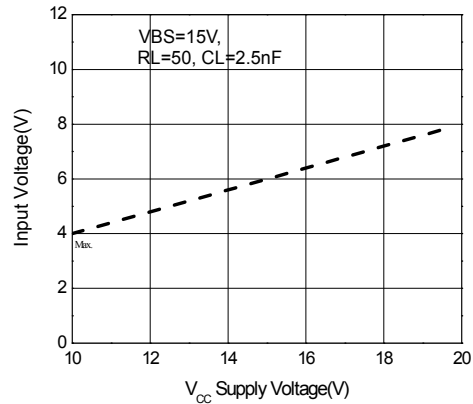


Figure 9b. Logic "0" IN Voltage vs VCC Supply Voltage

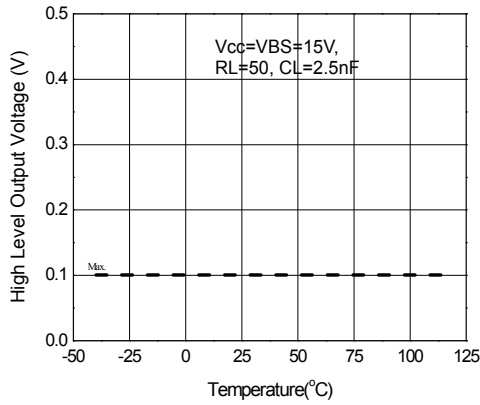


Figure 10a. High Level Output vs Temperature

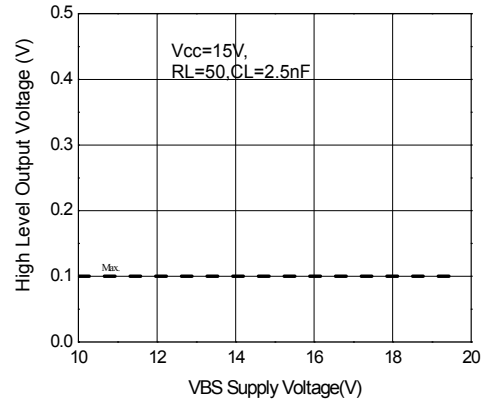


Figure 10b. High Level Output vs VBS Supply Voltage

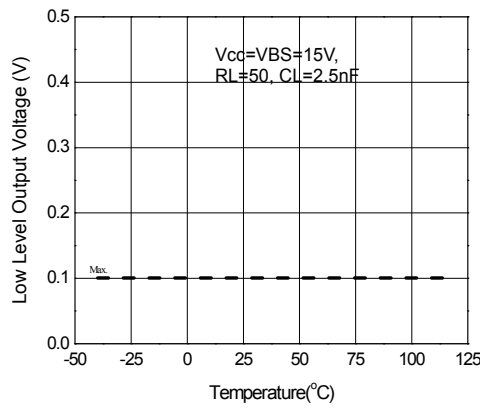


Figure 11a. Low Level Output vs Temperature

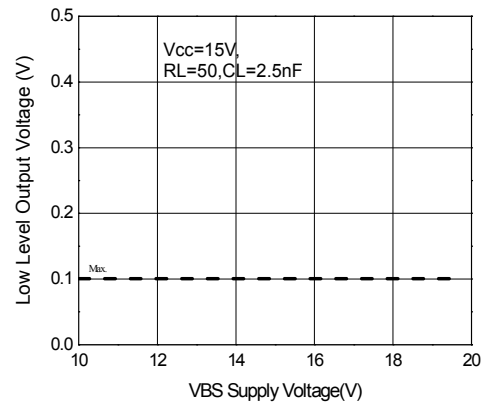


Figure 11b. Low Level Output vs VBS Supply Voltage

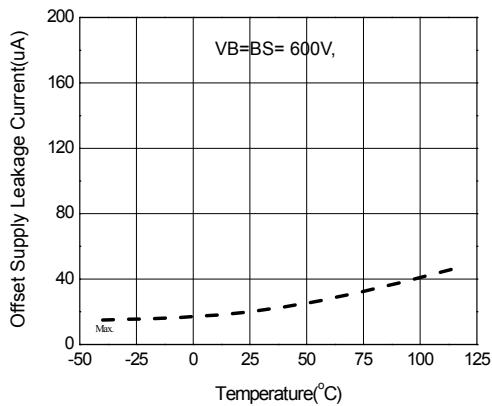


Figure 12a. Offset Supply Leakage Current vs Temperature

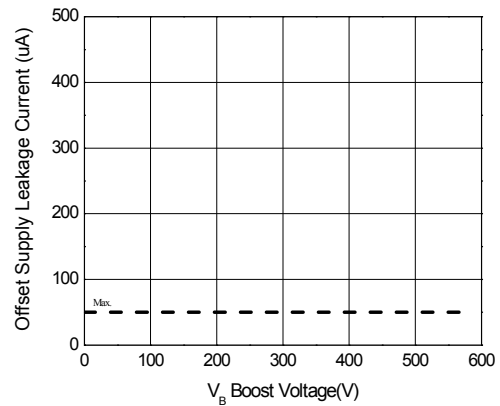


Figure 12b. Offset Supply Leakage Current vs VB Boost Voltage

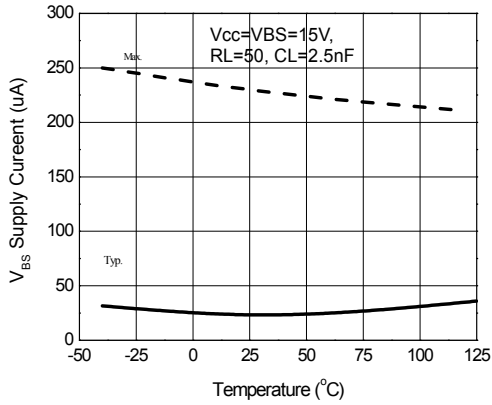


Figure 13a. VBS Supply Current vs Temperature

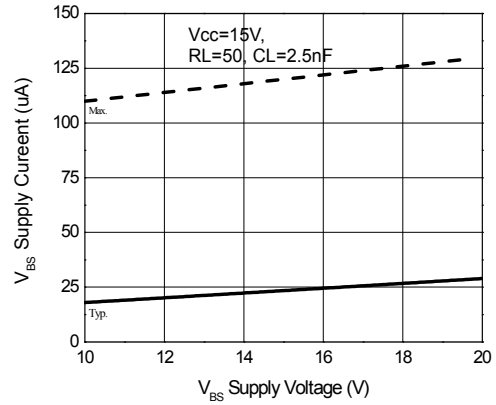


Figure 13b. VBS Supply Current vs VBS Supply Voltage

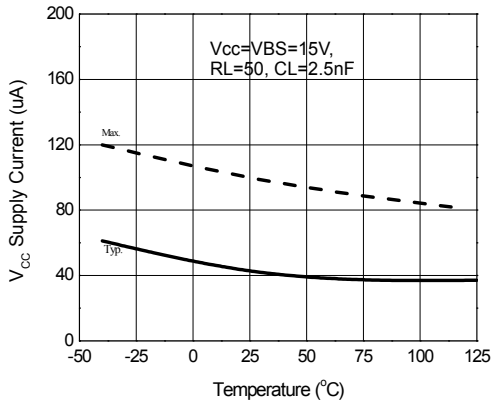


Figure 14a. VCC Supply Current vs Temperature

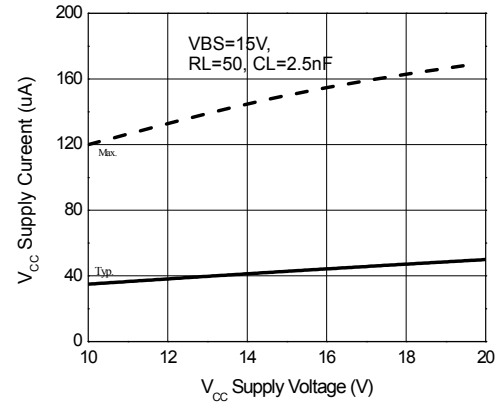


Figure 14b. VCC Supply Current vs VCC Supply Voltage

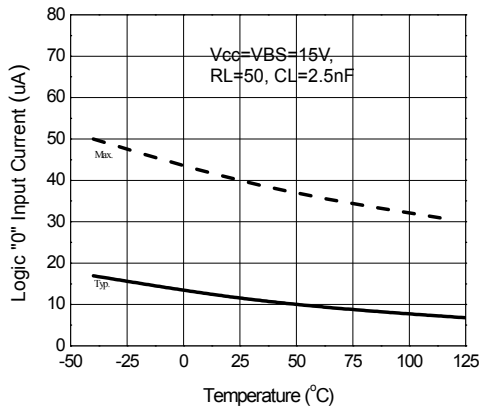


Figure 15a. Logic "0" IN Current vs Temperature

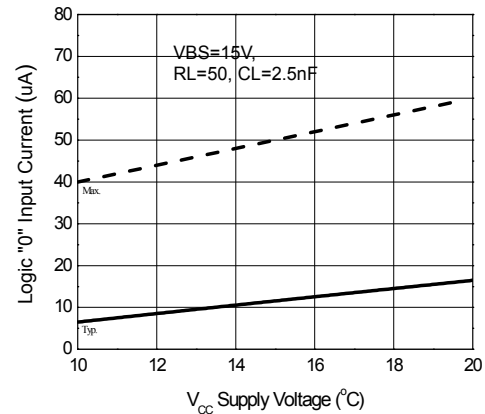


Figure 15b. Logic "0" IN Current vs VCC Supply Voltage

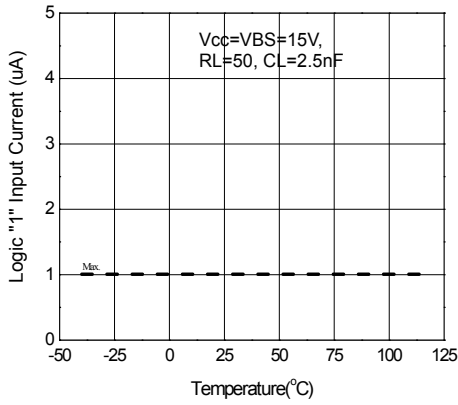


Figure 16a. Logic "1" IN Current vs Temperature

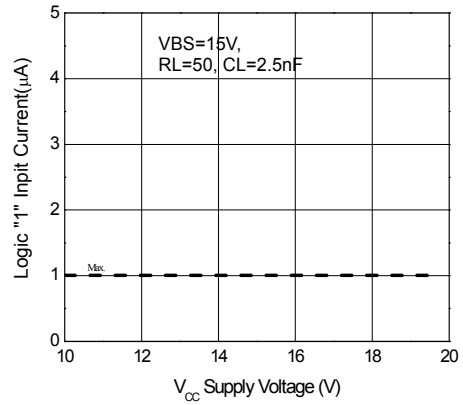


Figure 16b. Logic "1" IN Current vs VCC Supply Voltage

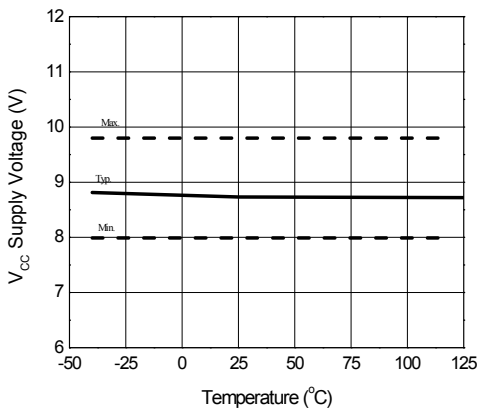


Figure 17a. VCC Under voltage Threshold(+) vs Temperature

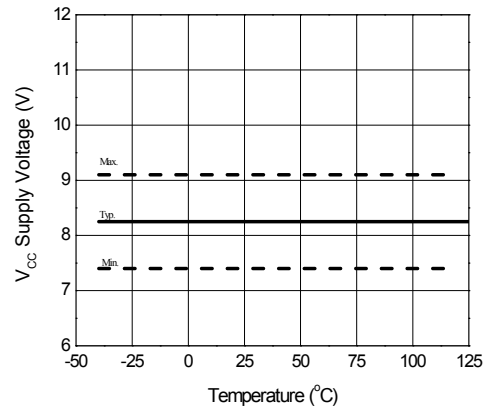


Figure 17b. VCC Under voltage Threshold(-) vs Temperature

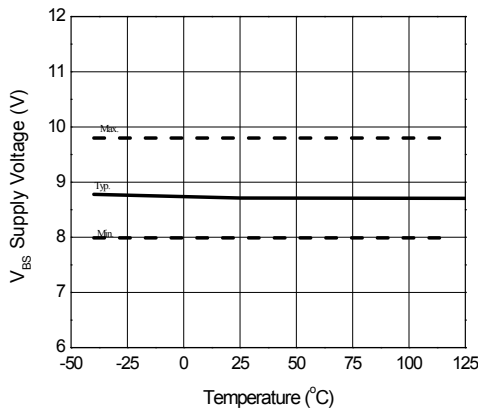


Figure 18a. VBS Under voltage Threshold(+) vs Temperature

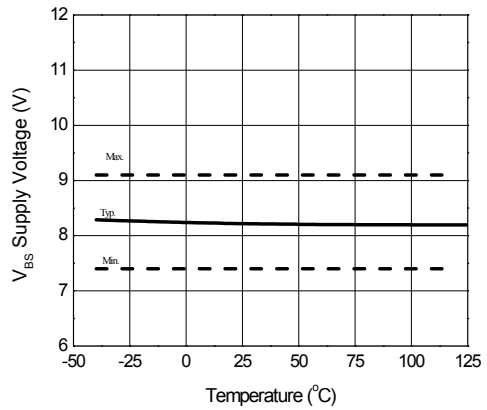


Figure 18b. VBS Under voltage Threshold(-) vs Temperature

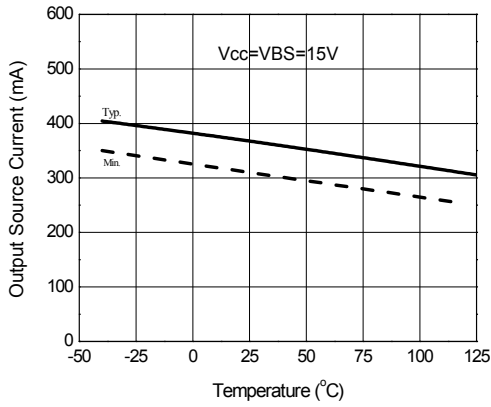


Figure 19a. Output Source Current vs Temperature

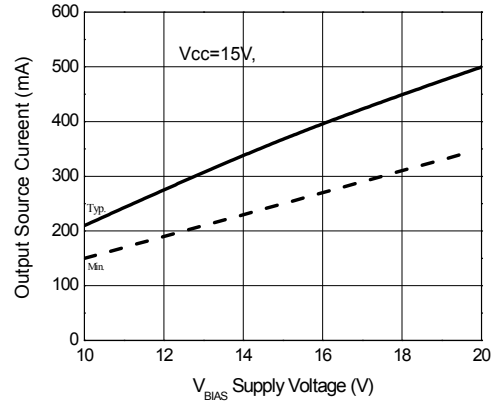


Figure 19b. Output Source Current vs VBS Supply Voltage

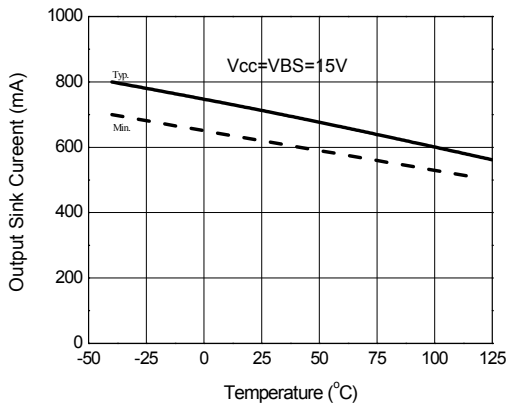


Figure 20a. Output Sink Current vs Temperature

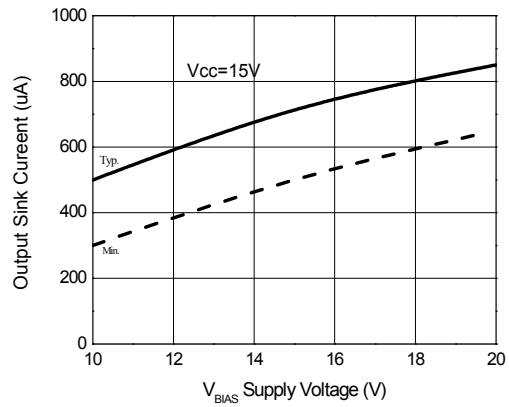


Figure 20b. Output Sink Current vs VBS Supply Voltage

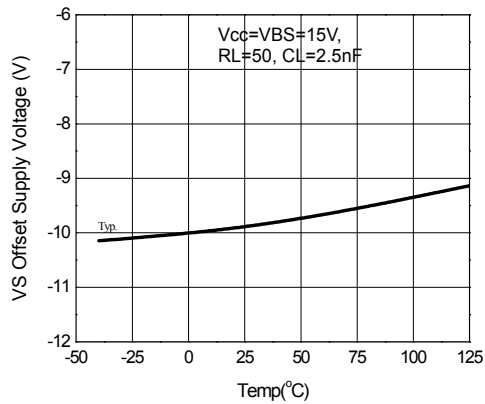


Figure 21a. Maximum VS Negative Voltage vs Temperature

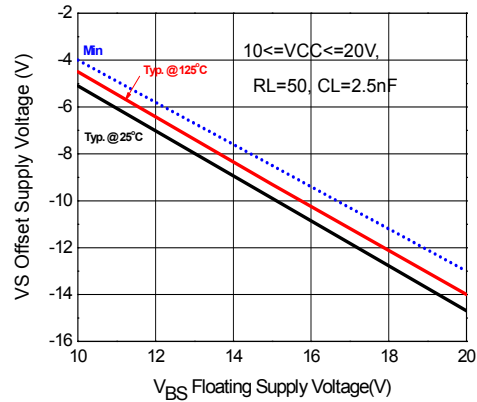
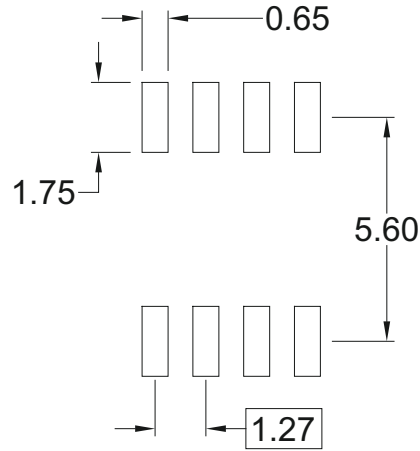
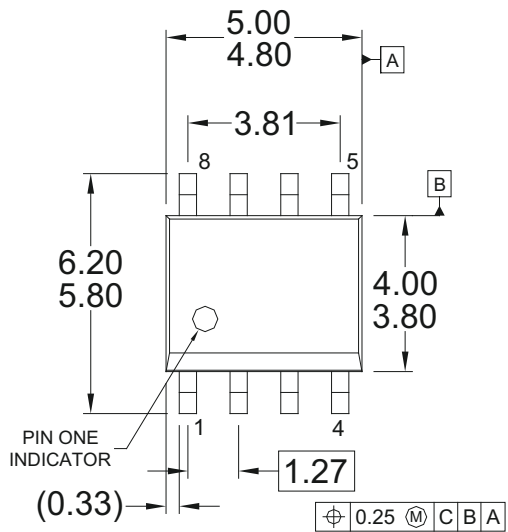
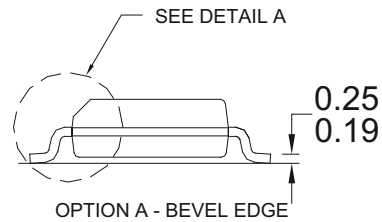
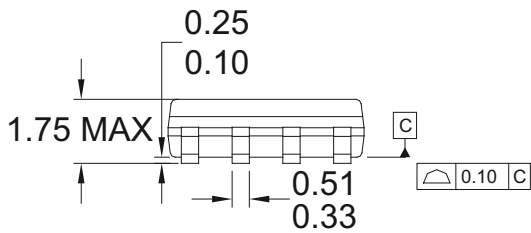


Figure 21b. Maximum VS Negative Voltage vs VBS Supply Voltage

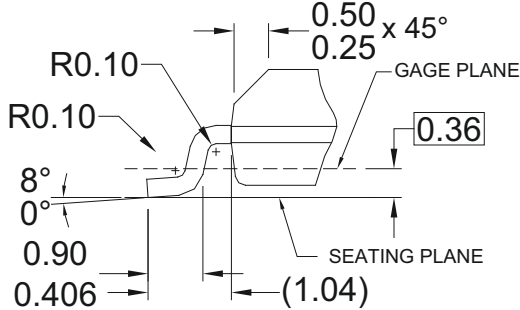
Package Dimensions



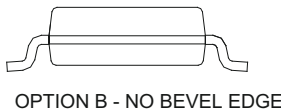
LAND PATTERN RECOMMENDATION



OPTION A - BEVEL EDGE



DETAIL A
SCALE: 2:1



OPTION B - NO BEVEL EDGE

NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
- E) DRAWING FILENAME: M08AREV13

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.








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<http://www.fairchildsemi.com/packaging/>



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Auto-SPM™	FPS™	PowerTrench®	
Build it Now™	F-PFS™	PowerXS™	
CorePLUS™	FRFET®	Programmable Active Droop™	
CorePOWER™	Global Power Resource SM	QFET®	
CROSSVOLT™	Green FPS™	QS™	
CTL™	Green FPS™ e-Series™	Quiet Series™	
Current Transfer Logic™	Gmax™	RapidConfigure™	
EcoSPARK®	GTO™	 ™	
EfficientMax™	IntelliMAX™	Saving our world, 1mW/W/kW at a time™	
EZSWITCH™*	ISOPLANAR™	SignalWise™	
 ™*	MegaBuck™	SmartMax™	
DEUXPEED™	MICROCOUPLER™	SMART START™	
 ™	MicroFET™	SPM®	
Fairchild®	MicroPak™	STEALTH™	
Fairchild Semiconductor®	MillerDrive™	SuperFET™	
FACT Quiet Series™	MotionMax™	SuperSOT™-3	
FACT®	Motion-SPM™	SuperSOT™-6	
FAST®	OPTOLOGIC®	SuperSOT™-8	
FAST®	OPTOPLANAR®	SupreMOS™	
FastvCore™	 ™	SyncFET™	
FETBench™	PDP SPM™	Sync-Lock™	

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As used herein:

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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