December 2009



# FAN73933 Half-Bridge Gate Drive IC

#### Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 2.5A/2.5A Sourcing/Sinking Current Driving Capability
- Extended Allowable Negative V<sub>S</sub> Swing to -9.8V for Signal Propagation at V<sub>BS</sub>=15V
- Output in Phase with Input Signal
- 3.3V and 5V Input Logic Compatible
- Matched Propagation Delay for Both Channels
- Built-in UVLO Functions for Both Channels
- Built-in Common-Mode dv/dt Noise Cancelling Circuit
- Programmable Dead-Time Control Function
- Internal 220ns Minimum Dead Time at R<sub>DT</sub>=0Ω

#### Applications

- High-Speed Power MOSFET and IGBT Gate Driver
- Induction Heating
- High-Power DC-DC Converter
- Synchronous Step-Down Converter
- Motor Drive Inverter

#### Description

The FAN73933 is a half-bridge, gate-drive IC with programmable dead-time control functions that can drive high-speed MOSFETs and IGBTs operating up to +600V. It has a buffered output stage with all NMOS transistors designed for high-pulse-current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to V<sub>S</sub>=-9.8V (typical) for V<sub>BS</sub>=15V.

The UVLO circuit prevents malfunction when  $V_{DD}$  and  $V_{BS}$  are lower than the specified threshold voltage.

The high-current and low-output voltage drop feature makes this device suitable for diverse half- and fullbridge inverters; motor drive inverters, switching mode power supplies, induction heating, and high-power DC-DC converter applications.



#### **Ordering Information**

Part Number	Package	Operating Temperature Range	Eco Status	Packing Method
FAN73933M	14-Lead, Small Outline Integrated Circuit (SOIC), Non-JEDEC, .150 Inch Narrow Body, 225SOP	-40°C to +125°C		Tube
FAN73933MX			RoHS	Tape & Reel

For Fairchild's definition of Eco Status, please visit: <u>http://www.fairchildsemi.com/company/green/rohs\_green.html</u>.



## **Pin Configuration**





## **Pin Definitions**

Pin #	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	V <sub>SS</sub>	Logic Ground
4	DT	Dead-Time Control with External Resistor (Referenced to V <sub>SS</sub> )
5	COM	Ground
6	LO	Low-Side Driver Return
7	V <sub>DD</sub>	Supply Voltage
8	NC	No Connection
9	NC	No Connection
10	NC	No Connection
11	Vs	High-Voltage Floating Supply Return
12	НО	High-Side Driver Output
13	V <sub>B</sub>	High-Side Floating Supply
14	NC	No Connection

### **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A=25^{\circ}C$  unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
VB	High-Side Floating Supply Voltage	-0.3	625.0	V
Vs	High-Side Floating Offset Voltage	V <sub>B</sub> -25.0	V <sub>B</sub> +0.3	V
V <sub>HO</sub>	High-Side Floating Output Voltage	V <sub>S</sub> -0.3	V <sub>B</sub> +0.3	V
V <sub>LO</sub>	Low-Side Output Voltage	-0.3	V <sub>DD</sub> +0.3	V
V <sub>DD</sub>	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
V <sub>IN</sub>	Logic Input Voltage (HIN and LIN)	-0.3	V <sub>DD</sub> +0.3	V
DT	Programmable Dead-Time Pin Voltage	-0.3	V <sub>DD</sub> +0.3	V
V <sub>SS</sub>	Logic Ground	V <sub>DD</sub> -25	V <sub>DD</sub> +0.3	V
dV <sub>S</sub> /dt	Allowable Offset Voltage Slew Rate		± 50	V/ns
PD	Power Dissipation <sup>(1, 2, 3)</sup>		1	W
$\theta_{JA}$	Thermal Resistance		110	°C/W
Т <sub>Ј</sub>	Junction Temperature		+150	°C
T <sub>STG</sub>	Storage Temperature	-55	+150	°C

Notes:

2

- 1 Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
  - Refer to the following standards: JESD51-2: Integral circuits thermal test method environmental conditions - natural convection, and JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
- 3 Do not exceed maximum P<sub>D</sub> under any circumstances.

#### **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>B</sub>	High-Side Floating Supply Voltage	V <sub>S</sub> +10	V <sub>S</sub> +20	V
V <sub>S</sub>	High-Side Floating Supply Offset Voltage	6-V <sub>DD</sub>	600	V
V <sub>HO</sub>	High-Side Output Voltage	V <sub>S</sub>	V <sub>B</sub>	V
V <sub>DD</sub>	Low-Side and Logic Fixed Supply Voltage	10	20	V
V <sub>LO</sub>	Low-Side Output Voltage	COM	V <sub>DD</sub>	V
V <sub>IN</sub>	Logic Input Voltage (HIN and LIN)	V <sub>SS</sub>	V <sub>DD</sub>	V
DT	Programmable Dead-Time Pin Voltage	V <sub>SS</sub>	V <sub>DD</sub>	V
V <sub>SS</sub>	Logic Ground	-5	+5	V
T <sub>A</sub>	Operating Ambient Temperature	-40	+125	°C

### **Electrical Characteristics**

 $V_{BIAS}(V_{DD}, V_{BS})=15.0V$ ,  $V_{SS}=COM=0V$ ,  $DT=V_{SS}$  and  $T_A = 25^{\circ}C$ , unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}/COM$  and are applicable to the respective input leads: HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Characteristics	Test Condition	Min.	Тур.	Max.	Unit
POWER S	SUPPLY SECTION					
I <sub>QDD</sub>	Quiescent V <sub>DD</sub> Supply Current	V <sub>IN</sub> =0V or 5V		0.9	1.5	mA
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	V <sub>IN</sub> =0V or 5V		50	100	μΑ
I <sub>PDD</sub>	Operating V <sub>DD</sub> Supply Current	f <sub>IN</sub> =20KHz, No Load		1.3	1.9	mA
I <sub>PBS</sub>	Operating V <sub>BS</sub> Supply Current	C <sub>L</sub> =1nF, f <sub>IN</sub> =20KHz, rms		450	800	μA
I <sub>LK</sub>	Offset Supply Leakage Current	V <sub>B</sub> =V <sub>S</sub> =600V			10	μA
BOOTST	RAPPED SUPPLY SECTION		-			
V <sub>DDUV+</sub> V <sub>BSUV+</sub>	V <sub>DD</sub> and V <sub>BS</sub> Supply Under-Voltage Positive-Going Threshold Voltage	V <sub>IN</sub> =0V, V <sub>DD</sub> =V <sub>BS</sub> =Sweep	8.0	9.0	10	V
V <sub>DDUV-</sub> V <sub>BSUV-</sub>	V <sub>DD</sub> and V <sub>BS</sub> Supply Under-Voltage Negative-Going Threshold Voltage	V <sub>IN</sub> =0V, V <sub>DD</sub> =V <sub>BS</sub> =Sweep	7.4	8.4	9.4	V
V <sub>DDUVH</sub> - V <sub>BSUVH</sub>	V <sub>DD</sub> and V <sub>BS</sub> Supply Under-Voltage Lockout Hysteresis Voltage	V <sub>IN</sub> =0V, V <sub>DD</sub> =V <sub>BS</sub> =Sweep		0.6		V
INPUT LC	OGIC SECTION					6
V <sub>IH</sub>	Logic "1" Input Voltage for HO & Logic "0" for LO		2.5			V
V <sub>IL</sub>	Logic "0" Input Voltage for HO & Logic "1" for LO				0.8	V
I <sub>IN+</sub>	Logic Input High Bias Current	V <sub>IN</sub> =5V		20	50	μA
I <sub>IN-</sub>	Logic Input Low Bias Current	V <sub>IN</sub> =0V			2	μA
R <sub>IN</sub>	Logic Input Pull-Down Resistance		100	250		KΩ
GATE DR	IVER OUTPUT SECTION					
V <sub>OH</sub>	High-Level Output Voltage (V <sub>BIAS</sub> - V <sub>O</sub> )	No Load			1.5	V
V <sub>OL</sub>	Low-Level Output Voltage	No Load			100	mV
I <sub>O+</sub>	Output High, Short-Circuit Pulsed Current <sup>(4)</sup>	V <sub>HO</sub> =0V, V <sub>IN</sub> =5V, PW ≤10µs	2.0	2.5		A
I <sub>O-</sub>	Output Low, Short-Circuit Pulsed Current <sup>(4)</sup>	V <sub>HO</sub> =15V,V <sub>IN</sub> =0V, PW ≤10µs	2.0	2.5		А
VS	Allowable Negative $V_S$ Pin Voltage for IN Signal Propagation to HO			-9.8	-7.0	V

Note:

4. These parameters guaranteed by design.

## **Dynamic Electrical Characteristics**

 $V_{BIAS}(V_{DD}, V_{BS})=15.0V, V_{SS}=COM=0V, C_L=1000pF, DT=V_{SS} and T_A=25^{\circ}C, unless otherwise specified.$ 

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
t <sub>ON</sub>	Turn-On Propagation Delay Time <sup>(5)</sup>	$V_{S}$ =0V, $R_{DT}$ =0 $\Omega$		160	230	ns
t <sub>OFF</sub>	Turn-Off Propagation Delay Time	V <sub>S</sub> =0V		160	230	ns
Mt <sub>ON</sub>	Delay Matching, HO & LO Turn-On			0	50	ns
Mt <sub>OFF</sub>	Delay Matching, HO & LO Turn-Off			0	50	ns
t <sub>R</sub>	Turn-On Rise Time	V <sub>S</sub> =0V		40	60	ns
t <sub>F</sub>	Turn-Off Fall Time	V <sub>S</sub> =0V		20	35	ns
DT	Dead Time: LO Turn-Off to HO Turn-On & HO Turn-Off to LO Turn-On	R <sub>DT</sub> =0Ω	170	220	270	ns
		R <sub>DT</sub> =300KΩ	400	500	600	ns
MDT	Dead-Time Matching= DT <sub>LO-HO</sub> - DT <sub>HO-LO</sub>	R <sub>DT</sub> =0Ω		0	50	ns
		R <sub>DT</sub> =300KΩ		0	100	ns

#### Note:

5 The turn-on propagation display does not include dead time.















### **Application Information**

#### Negative V<sub>S</sub> Transient

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations. The biggest difficulty with this circuit is the negative voltage present at the emitter of the high-side switching device when the high-side switch is turned off in half-bridge applications.

If the high-side switch, Q1, turns-off while the load current is flowing to an inductive load; a current commutation occurs from high-side switch, Q1, to the diode, D2, in parallel with the low-side switch of the same inverter leg. Then the negative voltage present at the emitter of the high-side switching device, just before the freewheeling diode, D2, starts clamping, causes load current to suddenly flow to the low-side freewheeling diode, D2, as shown in Figure 39.



Figure 39. Half-Bridge Application Circuits

This negative voltage can be trouble for the gate driver's output stage. There is the possibility to develop an overvoltage condition of the bootstrap capacitor, input signal missing, and latch-up problems because it directly affects the source  $V_S$  pin of the gate driver, as shown in Figure 40. This undershoot voltage is called "negative  $V_S$  transient.





Figure 41. and Figure 42. show the commutation of the load current between the high-side switch, Q1, and lowside freewheelling diode, D3, in same inverter leg. The parasitic inductances in the inverter circuit from the die wire bonding to the PCB tracks are jumped together in  $L_{C}$  and  $L_{F}$  for each IGBT. When the high-side switch, Q1, and low-side switch, Q4, are turned on; the VS1 node is below DC+ voltage by the voltage drops associated with the power switch and the parasitic inductances of the circuit due to load current is flows from Q1 and Q4, as shown in Figure 41. When the high-side switch, Q1, is turned off and Q4 remains turned on, the load current to flows the low-side freewheeling diode, D3, due to the inductive load connected to V<sub>S1</sub> as shown in Figure 42. The current flows from ground (which is connected to the COM pin of the gate driver) to the load and the negative voltage present at the emitter of the high-side switching device.

In this case, the COM pin of the gate driver is at a higher potential than the V<sub>S</sub> pin due to the voltage drops associated with freewheeling diode, D3, and parasitic elements,  $L_{C3}$  and  $L_{E3}$ .







The FAN73933 has a negative  $\rm V_{S}$  transient performance curve, as shown in Figure 43.



Figure 43. Negative V<sub>S</sub> Transient Chracteristic

Even though the FAN73933 has been shown able to handle these negative  $V_S$  tranient conditions, it is strongly recommended that the circuit designer limit the negative  $V_S$  transient as much as possible by careful PCB layout to minimize the value of parasitic elements and component use. The amplitude of negative  $V_S$  voltage is proportional to the parasitic inductances and the turn-off speed, di/dt, of the switching device.

## **General Guidelines**

#### **Printed Circuit Board Layout**

The layout recommended for minimized parasitic elements is as follows:

- Direct tracks between switches with no loops or deviation.
- Avoid interconnect links. These can add significant inductance.
- Reduce the effect of lead-inductance by lowering package height above the PCB.
- Consider co-locating both power switches to reduce track length.
- To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.
- To reduce the EM coupling and improve the power switch turn-on/off performance, the gate drive loops must be reduced as much as possible.

#### **Placement of Components**

The recommended selection of component is as follows:

- Place a bypass capacitor between the V<sub>DD</sub> and V<sub>SS</sub> pins. A ceramic 1µF capacitor is suitable for most applications. This component should be placed as close as possible to the pins to reduce parasitic elements.
- The bypass capacitor from V<sub>CC</sub> to COM supports both the low-side driver and bootstrap capacitor recharge. A value at least ten times higher than the bootstrap capacitor is recommended.
- The bootstrap resistor, R<sub>BOOT</sub>, must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that V<sub>B</sub> does not fall below COM (ground). Recommended use is typically 5 ~ 10Ω, which increases the V<sub>BS</sub> time constant. If the votage drop of the bootstrap resistor and diode is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra-fast recovery diode can be used.
- The bootstrap capacitor, C<sub>BOOT</sub>, uses a low-ESR capacitor, such as a ceramic capacitor.

It is stongly recommended that the placement of components is as follows:

- Place components tied to the floating voltage pins (V<sub>B</sub> and V<sub>S</sub>) near the respective high-voltage portions of the device and the FAN73933. NC (not connected) pins in this package maximize the distance between the high-voltage and low-voltage pins (see Figure 3.).
- Place and route for bypass capacitors and gate resistors as close as possible to gate drive IC.
- Locate the bootstrap diode, D<sub>BOOT</sub>, as close as possible to bootstrap capacitor, C<sub>BOOT</sub>.
- The bootstrap diode must use a lower forward voltage drop and minimal switching time as soon as possible for fast recovery or ultra-fast diode.





The datasheet is for reference information only.