

FCU900N60Z

600V N-Channel MOSFET

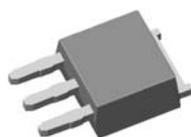
Features

- 675V @ $T_J = 150^\circ\text{C}$
- Max. $R_{DS(on)} = 900\text{m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 13\text{nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss-eff} = 49\text{pF}$)
- 100% Avalanche Tested
- ESD Improved Capacity

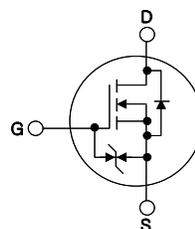
Description

SuperFET®II is, Fairchild's proprietary, new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET®II is very suitable for various AC/DC power conversion in switching mode operation for system miniaturization and higher efficiency.



I-PAK



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	Rating	Units
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	-DC	± 20
		-AC ($f > 1\text{Hz}$)	± 30
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	4.5
		-Continuous ($T_C = 100^\circ\text{C}$)	2.8
I_{DM}	Drain Current - Pulsed (Note 1)	13.5	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	47.5	mJ
I_{AR}	Avalanche Current (Note 1)	1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.52	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
	MOSFET dv/dt	100	
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	52	W
		- Derate above 25°C	0.42
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	100	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCU900N60Z	FCU900N60Z	I-PAK	-	-	75

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	625	-	-	V
		$I_D = 1\text{mA}, V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}$	675	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{mA}, \text{Referenced to } 25^\circ\text{C}$	-	0.72	-	V/ $^\circ\text{C}$
BV _{DS}	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 4.5\text{A}$	-	700	-	V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 600\text{V}, T_C = 125^\circ\text{C}$	-	-	10	μA
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 2.3\text{A}$	-	0.82	0.90	Ω
g _{FS}	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 2.3\text{A}$ (Note 4)	-	4.6	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	534	710	pF
C _{oss}	Output Capacitance		-	399	530	pF
C _{rss}	Reverse Transfer Capacitance		-	19.7	30	pF
C _{oss}	Output Capacitance	$V_{DS} = 380\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$	-	11.1	-	pF
C _{oss eff.}	Effective Output Capacitance	$V_{DS} = 0\text{V to } 480\text{V}, V_{GS} = 0\text{V}$	-	48.6	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	$V_{DS} = 380\text{V}, I_D = 2.3\text{A}$ $V_{GS} = 10\text{V}$	-	13.1	17	nC
Q _{gs}	Gate to Source Gate Charge		-	2.2	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	4.5	-
ESR	Equivalent Series Resistance	Drain open	-	2.4	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	$V_{DD} = 380\text{V}, I_D = 2.3\text{A}$ $V_{GS} = 10\text{V}, R_G = 4.7\Omega$	-	10.9	32	ns
t _r	Turn-On Rise Time		-	5.3	21	ns
t _{d(off)}	Turn-Off Delay Time		-	33.6	77	ns
t _f	Turn-Off Fall Time		(Note 4)	-	11.9	34

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current	-	-	4.5	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	13.5	A	
V _{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 2.3\text{A}$	-	-	1.2	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 2.3\text{A}$	-	156	-	ns
Q _{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	1.3	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 1.0\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 2.3\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

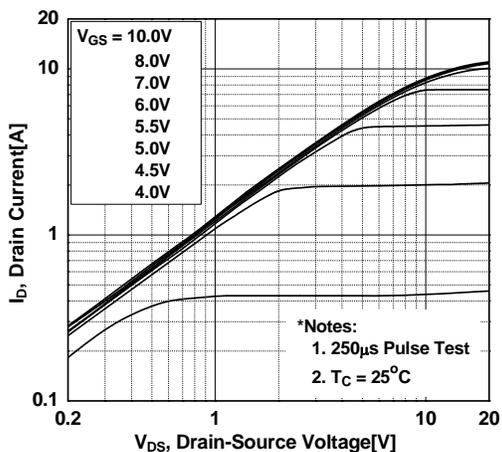


Figure 2. Transfer Characteristics

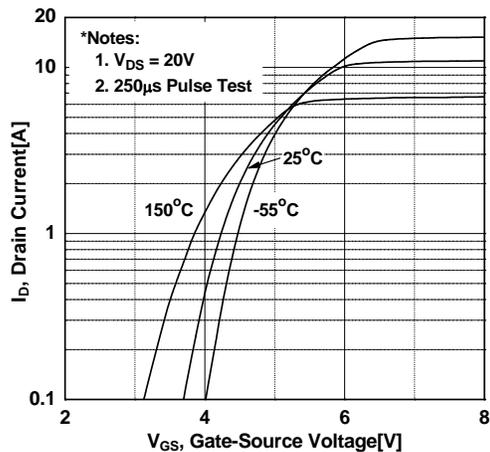


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

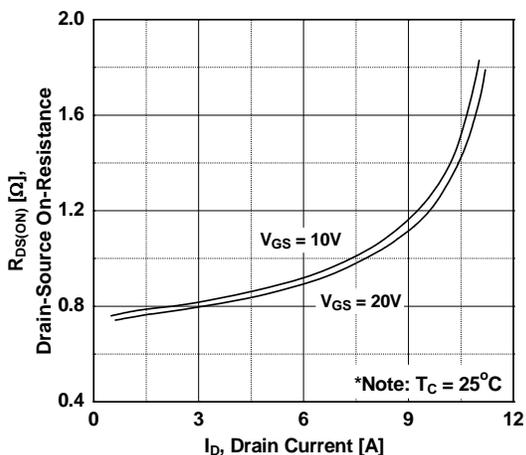


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

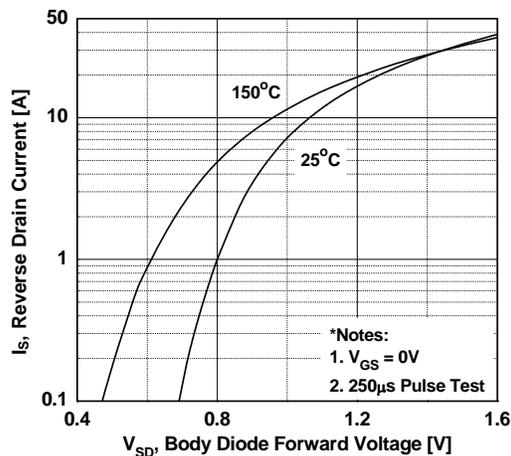


Figure 5. Capacitance Characteristics

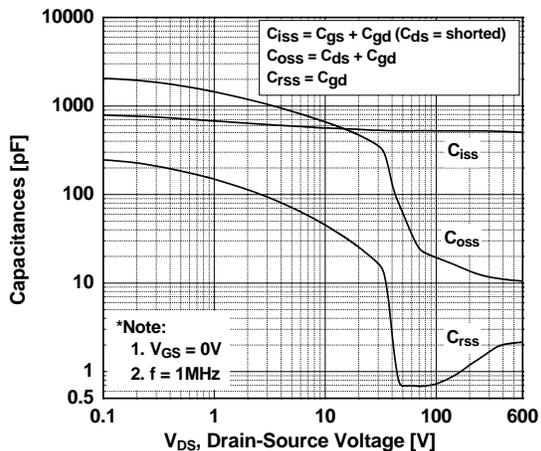
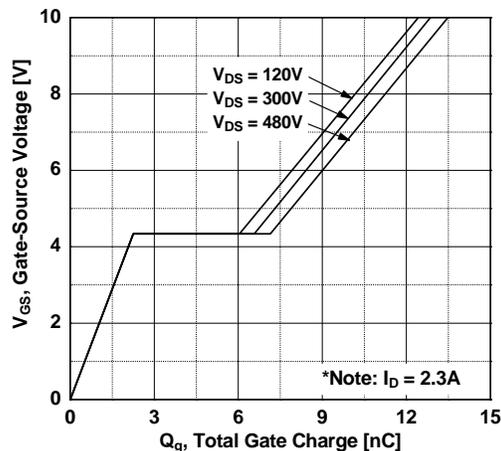


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

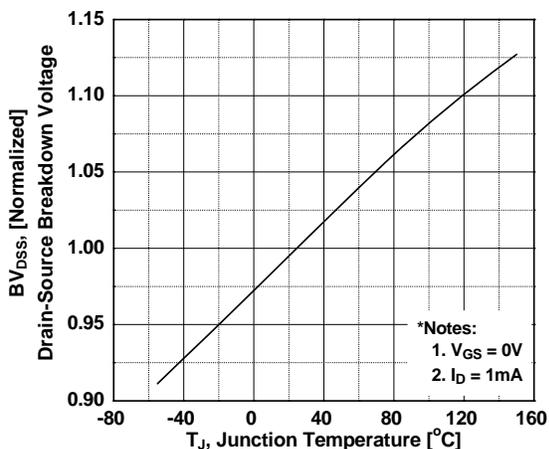


Figure 8. On-Resistance Variation vs. Temperature

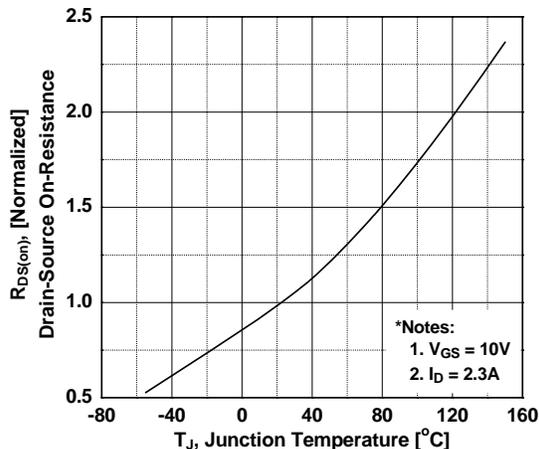


Figure 9. Maximum Safe Operating Area vs. Case Temperature

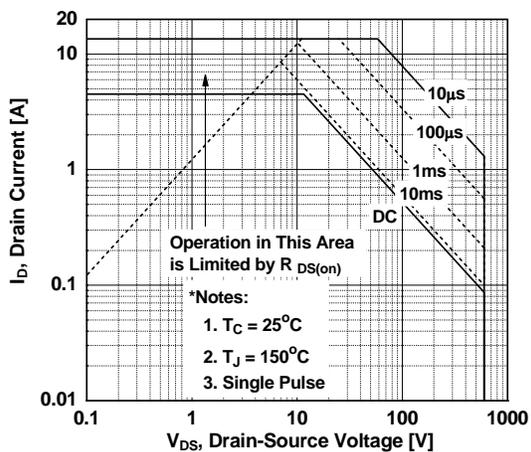


Figure 10. Maximum Drain Current

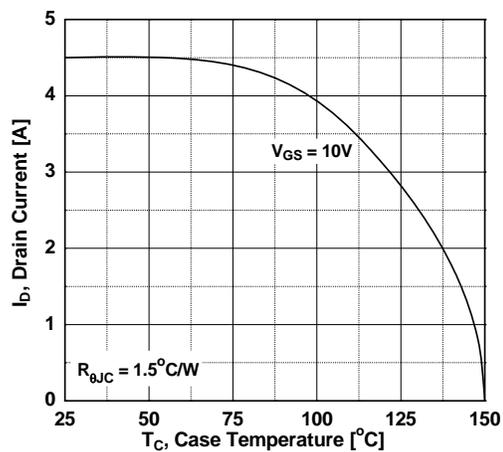
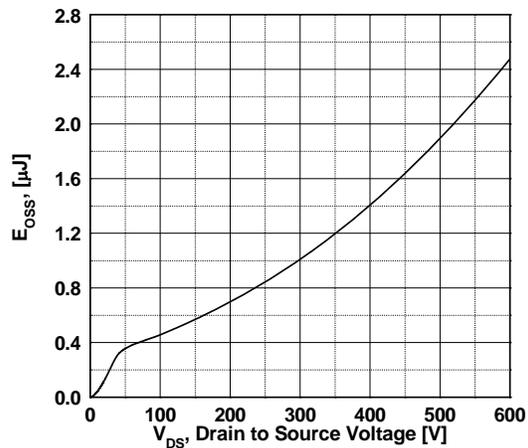
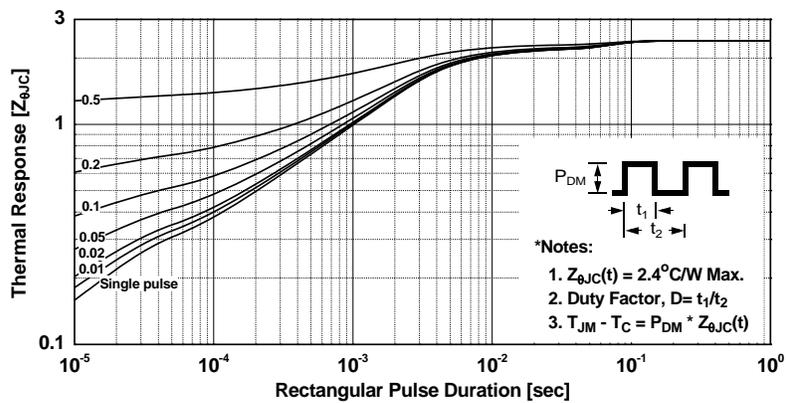


Figure 11. E_oss vs. Drain to Source Voltage

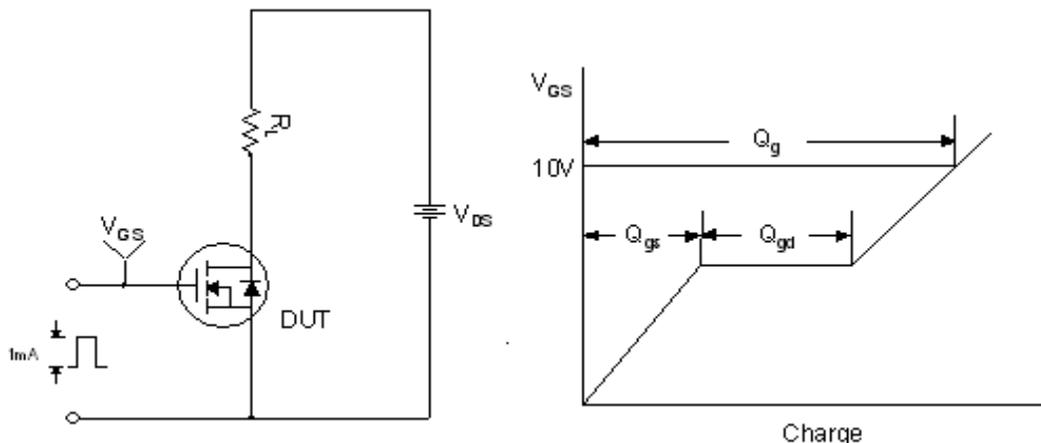


Typical Performance Characteristics (Continued)

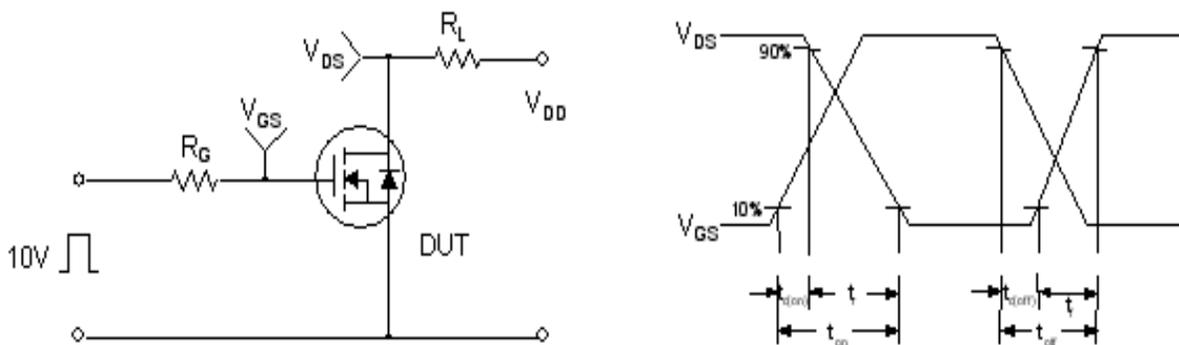
Figure 12. Transient Thermal Response Curve



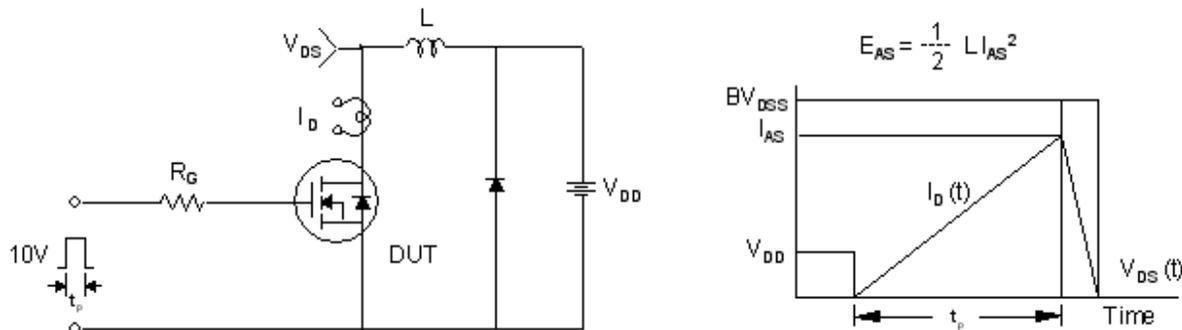
Gate Charge Test Circuit & Waveform



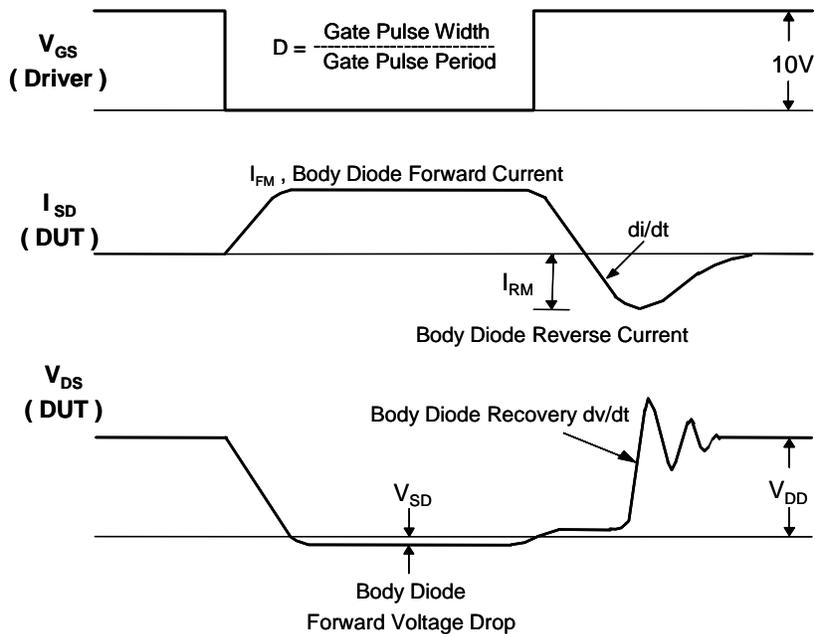
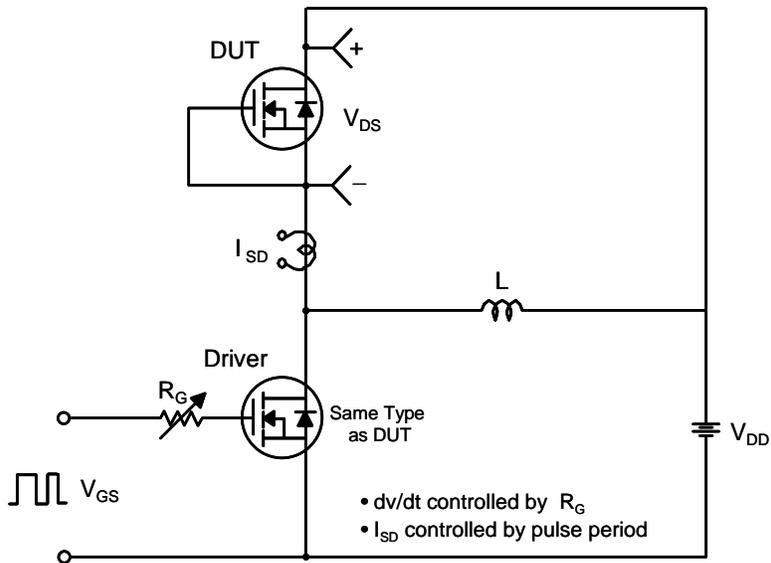
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

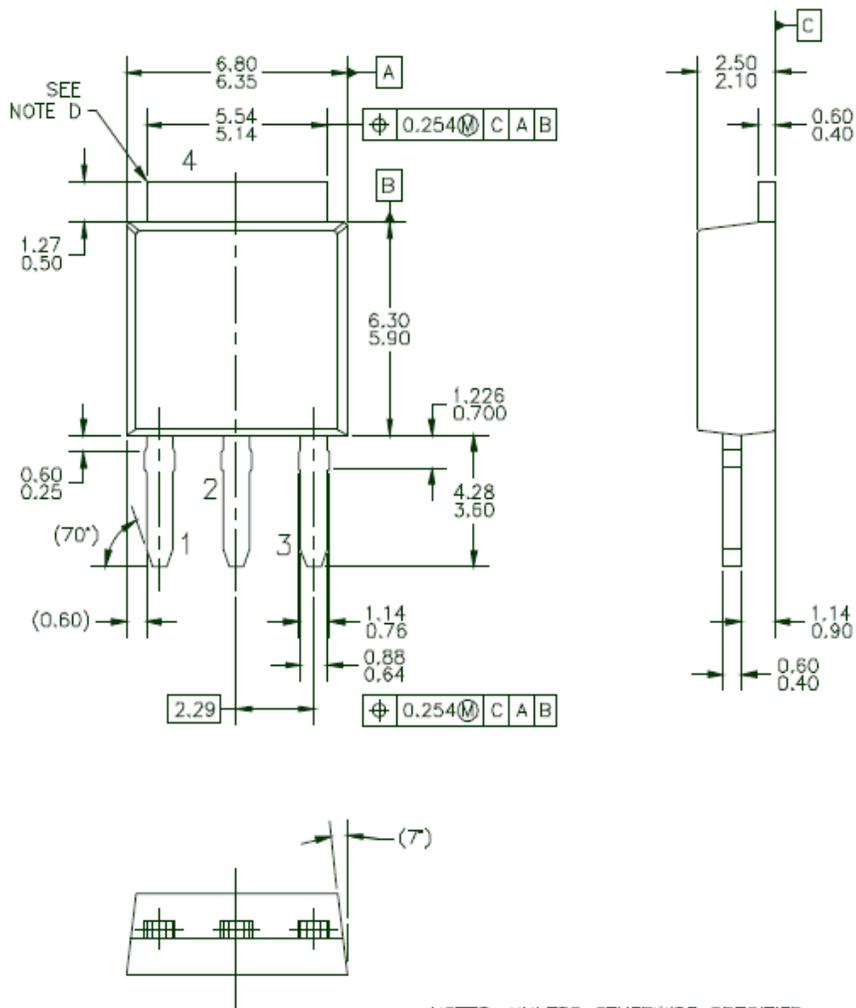


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

I-PAK (Short Lead)



- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) PACKAGE BODY REFERENCE: JEDEC, TO-251, ISSUE D, VARIATION AA, DATED JUNE 2002.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) DRAWING FILE NAME: T0251B03_3

Dimensions in Millimeters



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