



ON Semiconductor®

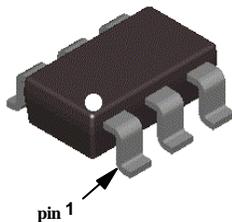
## FDC6324L Integrated Load Switch

### General Description

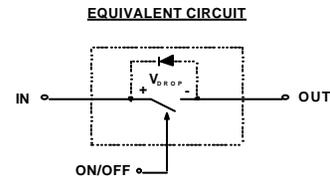
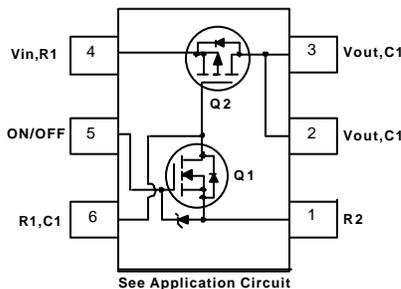
These Integrated Load Switches are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage high side load switch application where low conduction loss and ease of driving are needed.

### Features

- $V_{DROP}=0.2V$  @  $V_{IN}=12V$ ,  $I_L=1A$ ,  $V_{ON/OFF}=1.5$  to  $8V$   
 $V_{DROP}=0.3V$  @  $V_{IN}=5V$ ,  $I_L=1A$ ,  $V_{ON/OFF}=1.5$  to  $8V$ .
- High density cell design for extremely low on-resistance.
- $V_{ON/OFF}$  Zener protection for ESD ruggedness. >6KV Human Body Model.
- SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.



SuperSOT™-6



### Absolute Operating Range $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDC6324L	Units
$V_{IN}$	Input Voltage Range	3 - 20	V
$V_{ON/OFF}$	ON/OFF Voltage Range	1.5 - 8	V
$I_L$	Load Current @ $V_{DROP}=0.5V$ - Continuous (Note 1)	1.5	A
	- Pulsed (Note 1 & 3)	2.5	
$P_D$	Maximum Power Dissipation (Note 2a)	0.7	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf/1500Ohm)	6	kV

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2a)	180	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	60	$^\circ\text{C/W}$

### Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
I <sub>FL</sub>	Forward Leakage Current	V <sub>IN</sub> = 20 V, V <sub>ON/OFF</sub> = 0 V			1	μA
I <sub>RL</sub>	Reverse Leakage Current	V <sub>IN</sub> = -20 V, V <sub>ON/OFF</sub> = 0 V			-1	μA
<b>ON CHARACTERISTICS</b> (Note 3)						
V <sub>IN</sub>	Input Voltage		3		20	V
V <sub>ON/OFF</sub>	On/Off Voltage		1.5		8	V
V <sub>DROP</sub>	Conduction Voltage Drop @ 1A	V <sub>IN</sub> = 10 V, V <sub>ON/OFF</sub> = 3.3V		0.135	0.2	V
		V <sub>IN</sub> = 5 V, V <sub>ON/OFF</sub> = 3.3 V		0.215	0.3	
I <sub>L</sub>	Load Current	V <sub>DROP</sub> = 0.2 V, V <sub>IN</sub> = 10 V, V <sub>ON/OFF</sub> = 3.3 V	1			A
		V <sub>DROP</sub> = 0.3 V, V <sub>IN</sub> = 5 V, V <sub>ON/OFF</sub> = 3.3 V	1			

Notes:

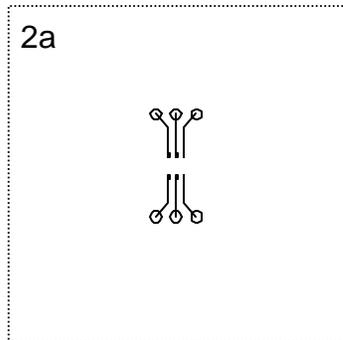
1. V<sub>IN</sub> = 20V, V<sub>ON/OFF</sub> = 8V, V<sub>DROP</sub> = 0.5V, T<sub>A</sub> = 25°C

2. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J}(t)} = \frac{T_J - T_A}{R_{\theta J} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical R<sub>θJA</sub> for single device operation using the board layouts shown below on FR-4 PCB in still air environment

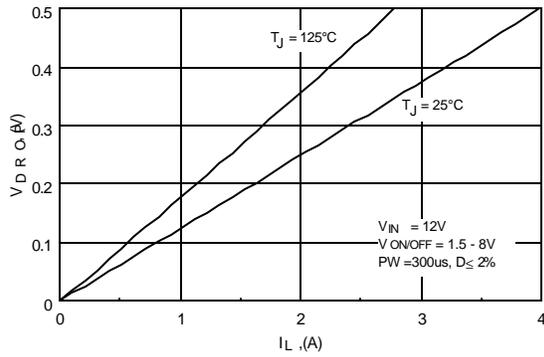
a. 180°C/W when mounted on a 2oz minimum copper pad.



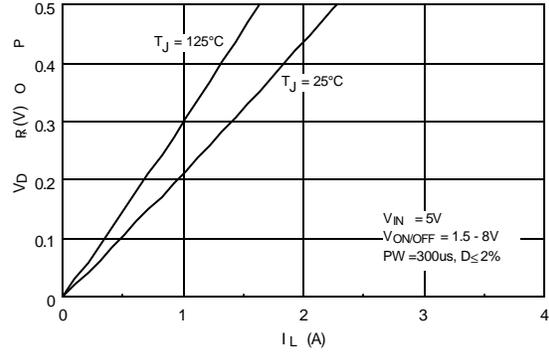
Scale 1 : 1 on letter size paper

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

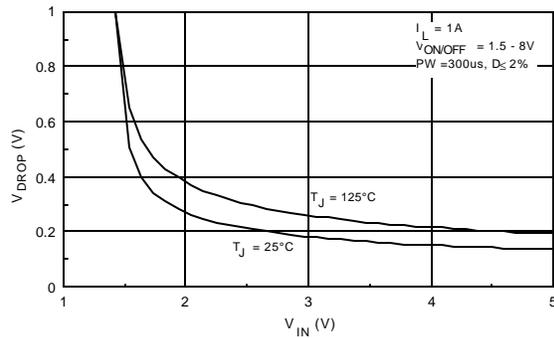
**Typical Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)



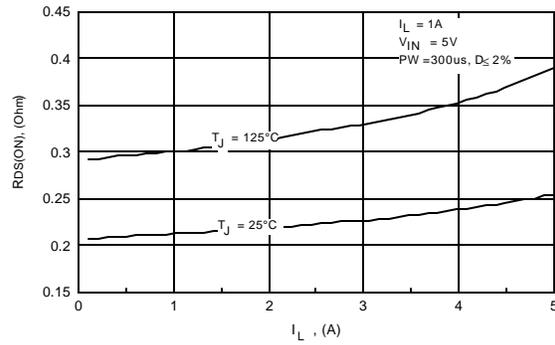
**Figure 1.**  $V_{DROD}$  Versus  $I_L$  at  $V_{IN}=12V$ .



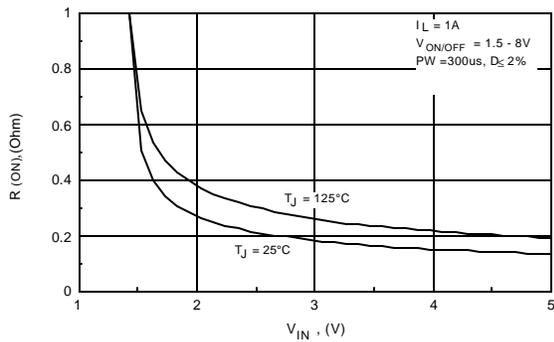
**Figure 2.**  $V_{DROD}$  Versus  $I_L$  at  $V_{IN}=5.0V$ .



**Figure 3.**  $V_{DROD}$  Versus  $V_{IN}$  at  $I_L=1A$ .

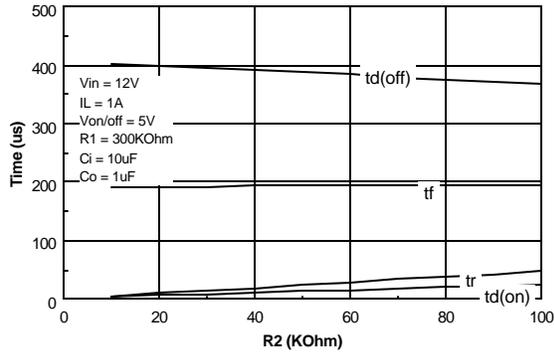


**Figure 4.**  $R_{DS(ON)}$  Versus  $I_L$  at  $V_{IN}=5.0V$ .

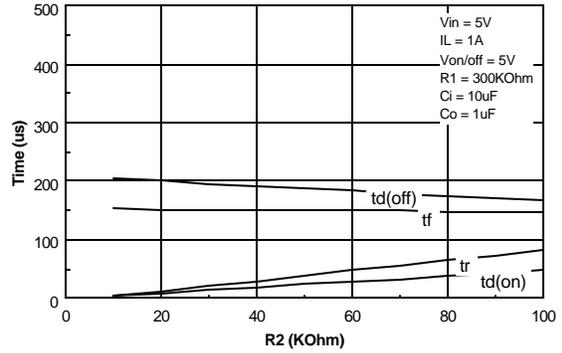


**Figure 5.** On Resistance Variation with Input Voltage.

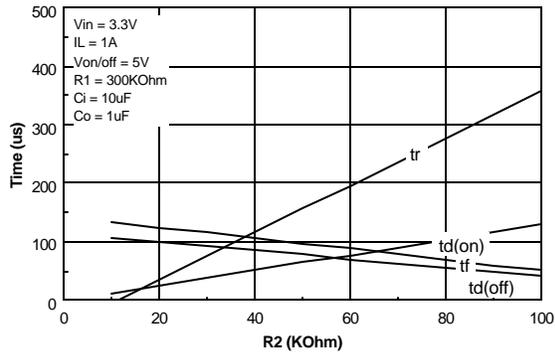
**Typical Electrical Characteristics** ( $T_A = 25\text{ }^\circ\text{C}$  unless otherwise noted)



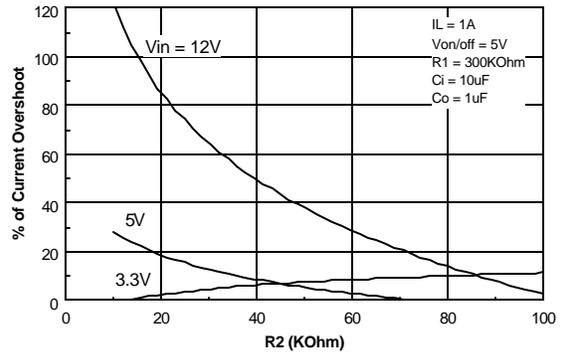
**Figure 6. Switching Variation with R2 at Vin = 12V and R1 = 300KOhm.**



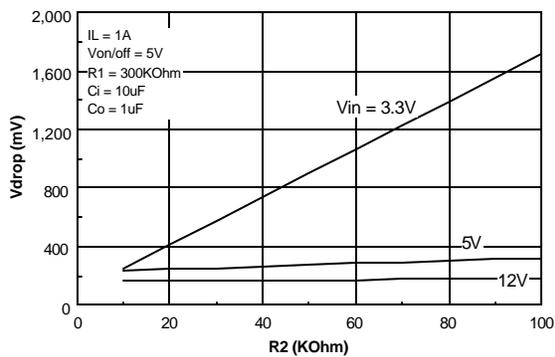
**Figure 7. Switching Variation with R2 at Vin = 5V and R1 = 300KOhm.**



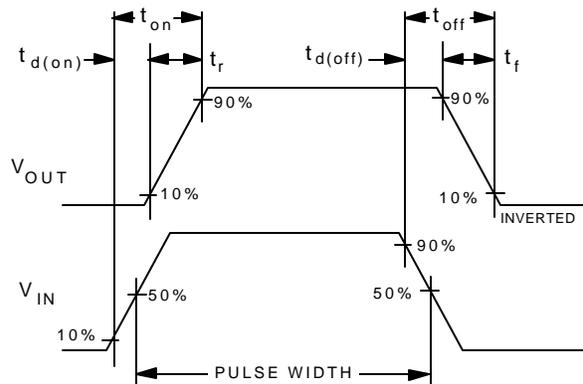
**Figure 8. Switching Variation with R2 at Vin = 3.3V and R1 = 300KOhm.**



**Figure 9. % of Current Overshoot Variation with Vin and R2.**

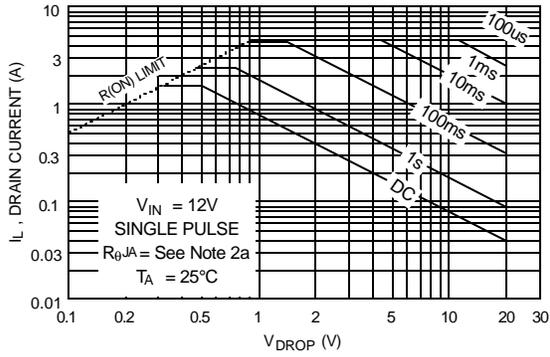


**Figure 10. Vdrop Variation with Vin and R2.**

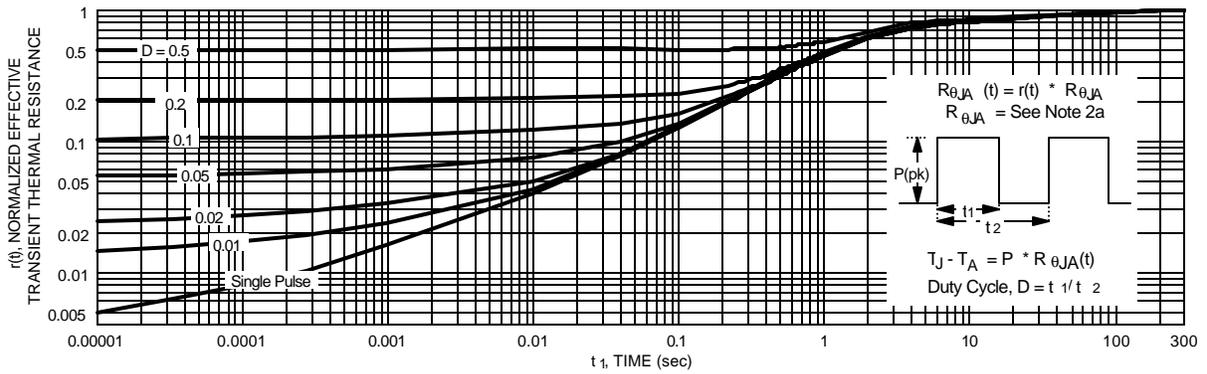


**Figure 11. Switching Waveforms.**

**Typical Electrical Characteristics** ( $T_A = 25\text{ }^\circ\text{C}$  unless otherwise noted )



**Figure 12. Safe Operating Area.**

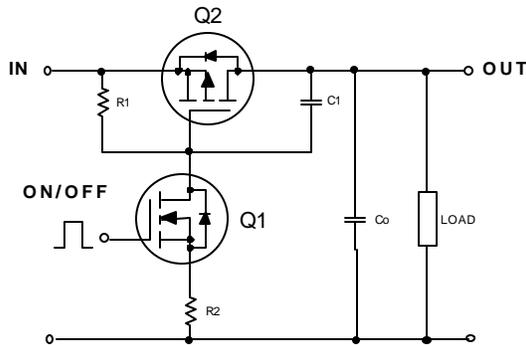


**Figure 13. Transient Thermal Response Curve.**

Note: Thermal characterization performed on the conditions described in Note 2a. Transient thermal response will change depends on the circuit board

## FDC6324L Load Switch Application

### APPLICATION CIRCUIT



### General Description

This device is particularly suited for computer peripheral switching applications where 20V input and 1A output current capability are needed. This load switch integrates a small N-Channel Power MOSFET (Q1) which drives a large P-Channel Power MOSFET (Q2) in one tiny SuperSOT™-6 package.

A load switch is usually configured for high side switching so that the load can be isolated from the active power source. A P-Channel Power MOSFET, because it does not require its drive voltage above the input voltage, is usually more cost effective than using an N-Channel device in this particular application. A large P-Channel Power MOSFET minimizes voltage drop. By using a small N-Channel device the driving stage is simplified.

### Component Values

R1	Typical 10k - 1MΩ	
R2	Typical 0 - 10kΩ	(optional)
C1	Typical 1000pF	(optional)

### Design Notes

- R1 is needed to turn off Q2.
- R2 can be used to soft start the switch in the case the output capacitance Co is small.
- $R2 \leq$  should be at least 10 times smaller than R1 to guarantee Q1 turns on.
- By using R1 and R2 a certain amount of current is lost from the input. This bias current loss is given by the equation
 
$$I_{BIAS\_LOSS} = \frac{V_{in}}{R1 + R2}$$
 when the switch is ON.  $I_{BIAS\_LOSS}$  can be minimized by large R1.
- R2 and  $C_{RSS}$  of Q2 make ramp for slow turn on. If excessive overshoot current occurs due to fast turn on, additional capacitance C1 can be added externally to slow down the turn on.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative