FDMF5075

20 A Smart Power Stage (SPS) Modules with Integrated Current and Temperature Monitors

The FDMF5075 is ON Semiconductor's next generation of Smart Power Stage (SPS) solutions with fully optimized, ultra−compact, integrated MOSFETs plus driver for high−current, high frequency, and synchronous buck DC−DC converters.

With an integrated approach, the SPS switching power stage is optimized for driver and MOSFET dynamic performance, minimized system inductance, and power MOSFET $R_{DS(ON)}$.

The integration of Power MOSFETs with a driver IC also enables advanced high accuracy module thermal and current monitoring. The FDMF5075 provides an output signal (IMON), which reports the real−time module current. IMON is a very accurate, 5 μA/A signal representing the real time Power MOSFET drain currents. The IMON signal can be used to replace output filter inductor DCR current sense or resistor sense methods.

The FDMF5075 also includes very accurate module thermal monitor (TMON). TMON is a voltage sourced PTAT signal that is calibrated to provide a 0.8 V output at 25°C with an 8 mV / °C slope.

Features

- Up to 20 A of Current Handling Capability
- High−Performance, Universal Footprint, Copper−Clip 4 mm x 5 mm PQFN Package
- ON Semiconductor's PowerTrench® MOSFETs for Clean Voltage Waveforms and Reduced Ringing
- 30 V/ 25 V Breakdown Voltage MOSFETs for Higher Long Term Reliability
- Optimized FET Pair for Highest Efficiency at 10% ~ 15% Duty Cycle
- Optimized for Switching Frequencies up to 1 MHz
- Integrated Current Monitor Compliant with Intel's VR13 Accuracy Requirements
- Integrated Temperature Monitor (TMON)
- Catastrophic Fault Detection
  - Thermal Flag (OTP) for Over−Temperature Condition
  - Over−Current Protection FAULT (OCP)
  - High−Side Short Detect FAULT
  - Under−Voltage Lockout (UVLO) on VCC
- ON Semiconductor Green Packaging and RoHS Compliance

Applications

- Multiphase and Single Phase DC−DC Voltage Regulators in Servers, Storage Systems, Computing, Graphics Cards and Enterprise Switches among others

ON Semiconductor®

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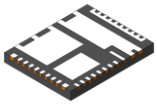
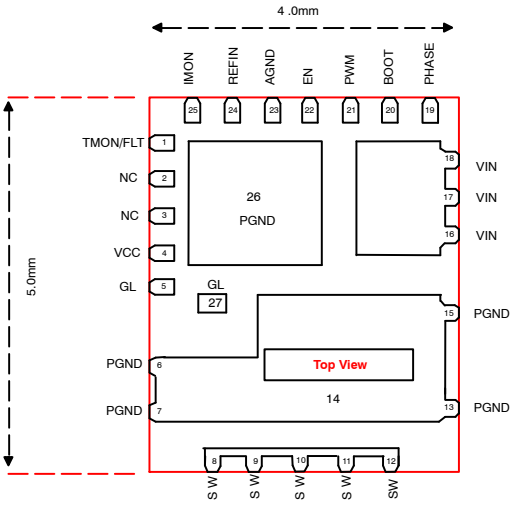


PQFN24 4 x 5, 0.5P
CASE 483BV

MARKING DIAGRAM

5075	= Specific Device Code
A2	= Version Code
A	= Assembly Plant Code
KK	= Lot Code
Y	= Year
W	= Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 19 of this data sheet.

TYPICAL APPLICATION

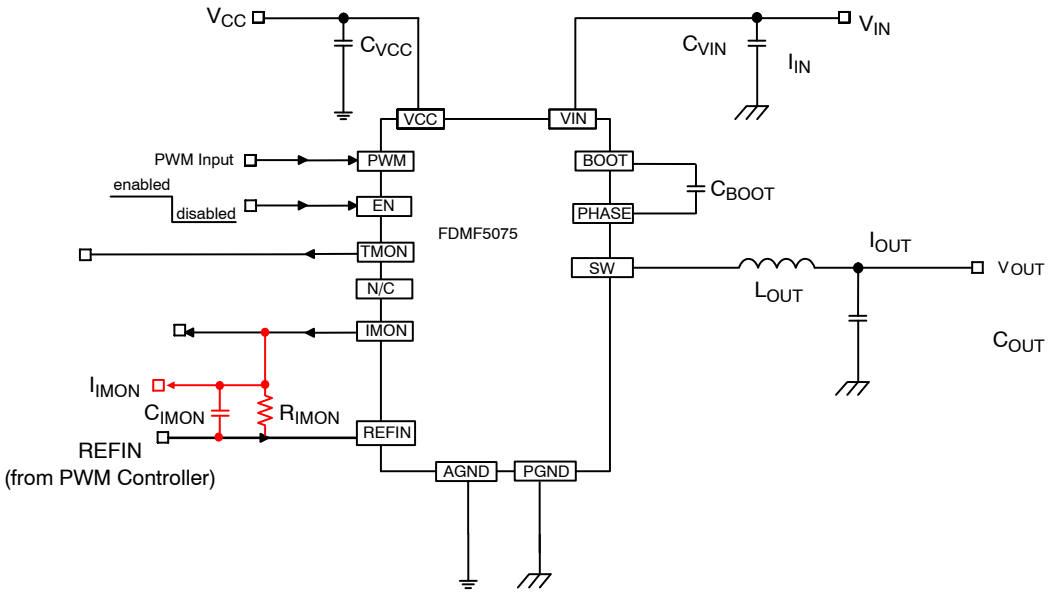


Figure 1. Typical Application Diagram

BLOCK DIAGRAM

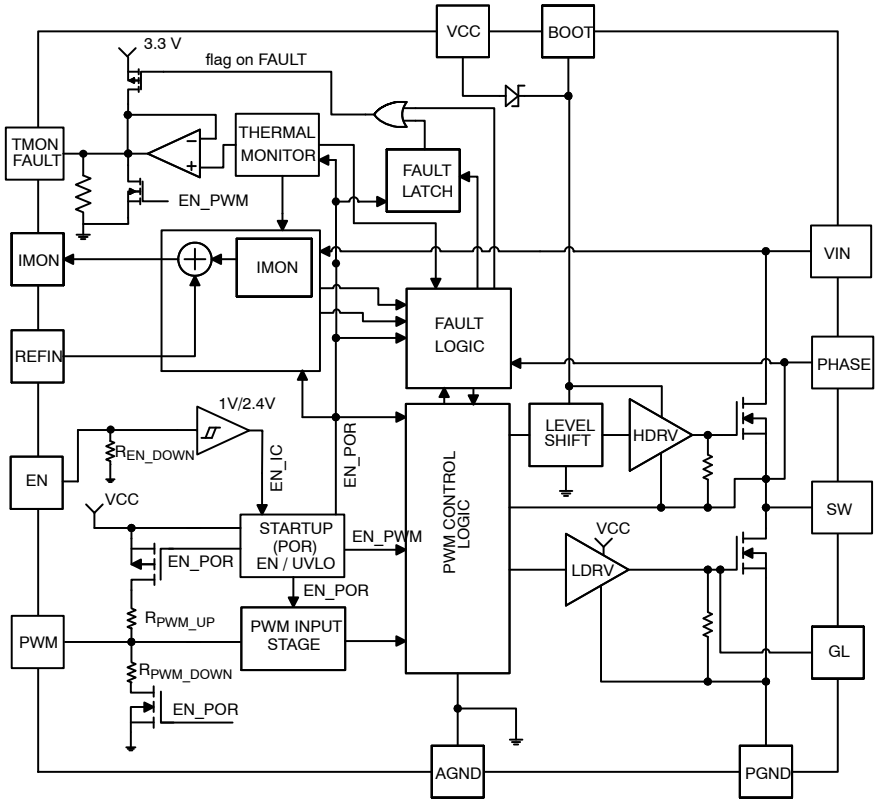


Figure 2. Functional Block Diagram

PIN CONNECTIONS

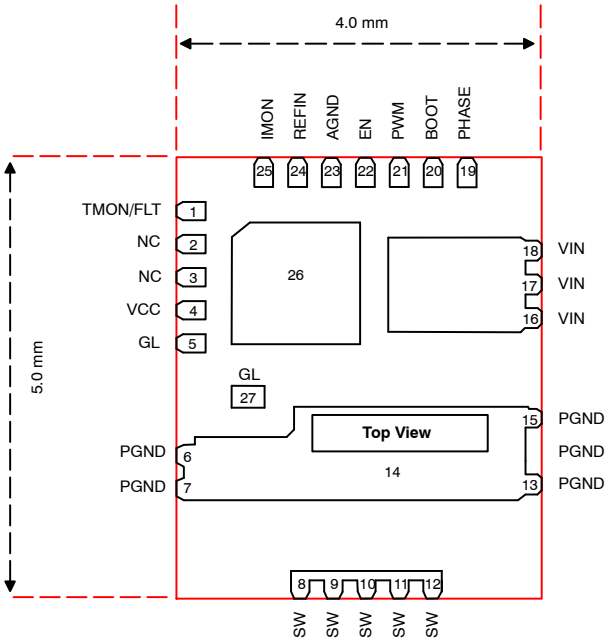


Figure 3. Pin Connections – (Top View)

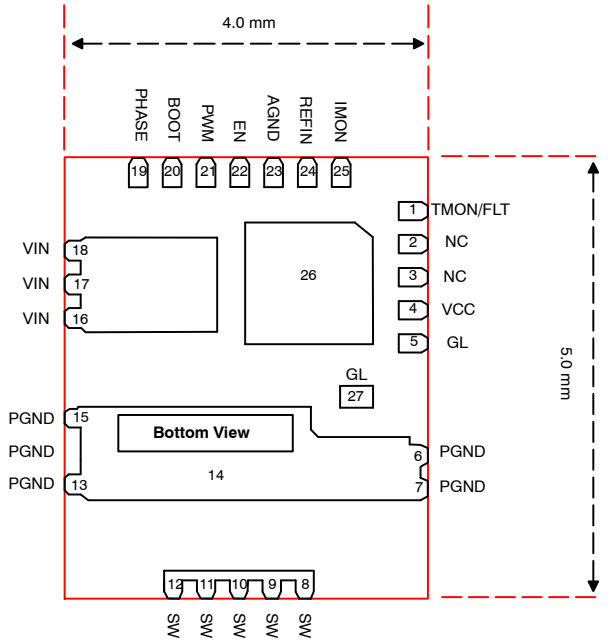


Figure 4. Pin Connections – (Bottom View)

Table 1. PIN FUNCTION DESCRIPTION

#	Name	Function
1	Tmon/Fault	Temperature and FAULT Reporting Pin. Pin sources a (PTAT) voltage of 0.6 V at 0°C with an 8 mV/°C slope when no module FAULT is present. In the event of a module FAULT, this pin pulls HIGH to an internal driver IC rail = 3.0 V typ. This pin will be pulled low under UVLO condition
2, 3	NC	No Connection
4	VCC	Power Supply input for LS gate drivers, Boot Diode and all analog control functions
5, 27	GL	Low Side Gate Monitor
8–12	SW	Switching node junction between high and low side MOSFETs
6, 7, 13–15, 26	PGND	Power ground connection for Power Stage high current path
16 – 18	VIN	Input Voltage to Power Stage
19	PHASE	Return for high side gate driver
20	BOOT	Supply for high side MOSFET gate driver. A capacitor from *BOOT* to *PHASE* supplies the charge to turn on the n−channel high side MOSFET. During the freewheeling interval (LS MOSFET on), the high side capacitor is recharged by an internal diode or PMOS connected to *VCC*
21	PWM	PWM input to gate driver IC
22	EN	EN = LOW disables most blocks inside IC (<500 uA Icc). EN=HIGH enables all blocks in-side IC and requires 30 μs power up time
23	AGND	Signal ground. All signals are referenced to this pin
24	REFIN	Referenced voltage used for IMON feature. DC input voltage supplied by external source (not generated on SPS driver IC)
25	IMON	Current monitor output (output is referenced to REFIN) – 5 mV/A

Table 2. ABSOLUTE MAXIMUM RATINGS ($T_A = T_J = 25°C$)

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage	Referenced to AGND	−0.3	6.0	V
V_{EN}	Module Enable	Referenced to AGND	−0.3	6.0	V
V_{PWM}	PWM Signal Input	Referenced to AGND	−0.3	VCC +0.3	V
V_{GL}	Low Gate Manufacturing Test Pin	Referenced to AGND	−0.3	6.0	V
V_{IMON}	Current Monitor Output	Referenced to AGND	−0.3	6.0	V
V_{REFIN}	Current Monitor Output Reference	Referenced to AGND	−0.3	6.0	V
$V_{TMON/FAULT}$	Thermal Monitor Output	Referenced to AGND	−0.3	6.0	V
$I_{TMON/FAULT}$	TMON/ FAULT Source Current			5.0	mA
V_{IN}	Power Input	Referenced to PGND, AGND	−0.3	25.0	V
V_{PHASE}	PHASE	Referenced to PGND, AGND (DC Only)	−0.3	25.0	V
		Referenced to PGND, AC < 2 ns	−12.0	25.0	V
V_{SW}	Switch Node Input	Referenced to PGND, AGND (DC Only)	−0.3	25.0	V
		Referenced to PGND, AC duration < 2 ns	−7.0	25.0	V
V_{BOOT}	Bootstrap Supply	Referenced to AGND (DC Only)	−0.3	30.0	V
		Referenced to AGND, AC duration < 2 ns	−9	30.0	V
$V_{BOOT-PHASE}$	Boot to PHASE Voltage		−0.3	7.0	V
$I_{O(peak)}$	Output Current			20	A
θ_{J-A}	Junction−to−Ambient Thermal Resistance			13	°C/W
θ_{J-PCB}	Junction−to−PCB Thermal Resistance (ON Semiconductor SPS Evaluation Board)			1.7	°C/W
T_A	Ambient Temperature Range		−40	+125	°C
T_J	Maximum Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range		−55	+150	°C
ESD	Electrostatic Discharge Protection		2000		V
			1000		V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Control Circuit Supply Voltage	4.5	5.0	5.5	V
V_{IN}	Output Stage Supply Voltage	4.5	12.0	16.0 (Note 1)	V
V_{REFIN}	REFIN Pin Supply Voltage	0.55	1.2	2.0	V
T_J	Operation Junction Temperature	−40		+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Operating at high V_{IN} can create excessive AC voltage overshoots on the SW−to−GND and BOOT−to−GND nodes during MOSFET switching transient. For reliable SPS operation, SW−to−GND and BOOT−to−GND must remain at or below the Absolute Maximum Ratings shown in the table above.

Table 4. ELECTRICAL CHARACTERISTICS

(Typical value is under V_{CC} = 5 V and $T_A = T_J$ = +25°C unless otherwise noted. Minimum and maximum values are under V_{CC} = 5 V ±10% and $T_J = T_A$ = 0°C to +125°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BASIC OPERATION						
I_{QQ_ENH}	Quiescent Current	$I_{QQ} = I_{VCC}$, PWM = LOW or HIGH (non−switching), EN = High	4.2	5.3	7	mA
I_{QQ_ENL}		$I_{QQ} = I_{VCC}$, PWM = LOW or HIGH (non−switching), EN = Low		510	720	μA
V_{UVLO}	UVLO Threshold	VCC Rising	3.8	4.1	4.2	V
V_{UVLO_HYST}	UVLO Hysteresis			0.17		V
EN INPUT						
V_{IH_EN}	High−Level Input Voltage		2.7			V
V_{IL_EN}	Low−Level Input Voltage				0.6	V
R_{PLD_EN}	Pull−Down Resistance			130		kΩ
t_{PD_ENH}	Propagation Delay for EN 0→1	PWM = GND, Delay Between EN from LOW to HIGH to GL from LOW to HIGH − Slow EN Setting	16	26	32	μs
t_{PD_ENL}	Propagation Delay for EN 1→0	PWM = GND, Delay Between EN from HIGH to LOW to GL from HIGH to LOW − Fast EN setting		43	109	ns
PWM INPUT						
R_{UP_PWM}	Pull−Up Impedance			21		kΩ
R_{DN_PWM}	Pull−Down Impedance			10		kΩ
V_{IH_PWM}	PWM High Level Voltage		2.35	2.45	2.55	V
V_{TRI_HI}	Tri−State Upper Threshold		2.1	2.2	2.3	V
V_{TRI_LO}	Tri−State Lower Threshold		0.9	1	1.1	V
V_{IL_PWM}	PWM Low Level Voltage		0.65	0.75	0.85	V
V_{HiZ_PWM}	Tri−State Open Voltage		1.4	1.5	1.85	V
PWM PROPAGATION DELAYS AND DEAD TIMES (T_A = 25°C, V_{CC} = 5 V, F_{SW} = 0.5 MHz, I_{OUT} = 20 A)						
t_{PD_PHGLL}	PWM HIGH Propagation Delay	PWM Going HIGH to GL going LOW, V_{IH_PWM} to 90% GL		17	20	ns
t_{PD_PLGHL}	PWM LOW Propagation Delay	PWM Going LOW to SW going LOW, V_{IL_PWM} to 90% SW		26	30	ns
t_{PD_TSGHH}	Exiting Tri−State Propagation Delay	PWM (from Tri−State) going HIGH to SW going HIGH, V_{IH_PWM} to 10% SW		27	30	ns
t_{PD_TSGLH}	Exiting Tri−State Propagation Delay	PWM (from Tri−State) going LOW to GL going HIGH, V_{IL_PWM} to 10% GL		20	30	ns
t_{D_DEADON}	LS Off to HS on Adaptive Time	GL ≤ 0.5 V to SW > 1.2 V. PWM Transition 0→1	6	13	26	ns
$t_{D\_DEADOFF}$	HS Off to LS on Adaptive Dead Time	SW ≤ 1.2 V to GL ≥ 0.5 V, PWM Transition 1→0	6	13	26	ns
$t_{D\_HOLD-OFF1}$	PWM High to Tri−State Hold Off Time	PWM Going Tri−State to SW going LOW	20	43	50	ns
$t_{D\_HOLD-OFF2}$	PWM Low to Tri−State Hold Off Time	PWM Going Tri−State to GL going LOW	20	36	50	ns
MINIMUM PWM HIGH / LOW TIME						
$t_{ON\_MIN\_HS}$	HS Minimal Turn On Time	SW gate rising 10% to falling 10%		37		ns
$t_{ON\_MIN\_LS}$	LS Minimal Turn On Time	LS gate rising 10% to falling 10%		33		ns

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Typical value is under V_{CC} = 5 V and $T_A = T_J$ = +25°C unless otherwise noted. Minimum and maximum values are under V_{CC} = 5 V ±10% and $T_J = T_A$ = 0°C to +125°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MINIMUM PWM HIGH / LOW TIME						
$t_{OFF\_MIN\_HS}$	HS Minimal Turn Off Time	SW gate falling 10% to rising 10%		31		ns
$t_{OFF\_MIN\_LS}$	LS Minimal Turn Off Time	LS gate falling 10% to rising 10%		51		ns
HIGH−SIDE DRIVER (HDRV, VCC = 5 V)						
t_{R_GH}	Rise Time	SW = 10% to 90%, C_{LOAD} = 1.3 nF		1.82		ns
t_{F_GH}	Fall Time	SW = 90% to 10%, C_{LOAD} = 1.3 nF		2.52		ns
LOW−SIDE DRIVER (LDRV, VCC = 5V)						
R_{SOURCE_GL}	Output Impedance, Sourcing	Source Current = 100 mA	1.22	1.56	2.1	Ω
I_{SOURCE_GL}	Output Sourcing Peak current	GL = 4.5 V		1.5		A
R_{SINK_GL}	Output Impedance, Sinking	Sink Current = 100 mA	0.467	0.575	0.775	Ω
I_{SINK_GL}	Output Sinking Peak Current	GL = 0 V		4		A
t_{R_GL}	Rise Time	GL = 10% to 90%, C_{LOAD} = 7.0 nF		12.14		ns
t_{F_GL}	Fall Time	GL = 90% to 10%, C_{LOAD} = 7.0 nF		6.14		ns
THERMAL MONITOR VOLTAGE						
V_{TMON_25C}	Thermal Monitor Voltage	$T_A = T_J$ = 25°C	0.776	0.8	0.824	V
V_{TMON_150C}		$T_A = T_J$ = 150°C	1.764	1.8	1.836	V
V_{TMON_SLOPE}	Thermal Monitor Voltage Slope	Guaranteed by design	7.8	8	8.2	mV/°C
I_{SOURCE_TMON}	TMON Source Current	V_{CC} = 5 V, 25°C		900		μA
I_{SINK_TMON}	TMON Sink Current	V_{CC} = 5 V, 25°C		40		μA
IMON BLOCK QUIESCENT CURRENT AND TIMES						
t_{blank_Hsoff}	HS Off to LS On Blanking Stop Time	IMON Blanking Time for PWM Transition 1→0		90		ns
T_{blank_Hson}	HS On to LS Off Blanking Stop Time	IMON Blanking Time for PWM Transition 0→1		70		ns
BW_{IMON}	IMON Amplifier Gain BW	L = 150 nH, V_{IN} = 12 V, V_{OUT} = 1.0 V, f_{SW} = 800 kHz		5		MHz
t_{delay}	IMON Propagation Delay Time	L = 150 nH, V_{IN} = 12 V, V_{OUT} = 1.0 V, f_{SW} = 800 kHz, IMON Peak to IL Peak		60	75	ns
IMON AND REFIN OPERATING RANGE						
V_{IMON}	Voltage at IMON Pin		0.5		2.5	V
V_{REFIN}	Voltage between REFIN to GND		0.6		2	V

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Typical value is under V_{CC} = 5 V and $T_A = T_J$ = +25°C unless otherwise noted. Minimum and maximum values are under V_{CC} = 5 V ±10% and $T_J = T_A$ = 0°C to +125°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IMON ACCURACY ($T_A = T_J$ = 25°C to 65°C, V_{CC} = 5 V, V_{IN} = 12 V)						
I_{MON_SLOPE}		I_{OUT} = −10 A to 30 A	4.75	5.00	5.25	μA/A
V_{IMON_5A}	R_{IMON} = 1 kΩ − resistor placed from IMON to REFIN and used to measure IMON−REFIN differential voltage Current Monitor Voltage ($V_{IMON-REFIN}$) V_{REFIN} = 1.2 V	I_{OUT} = 5 A, Voltage is Referenced to REFIN Pin	23	25	27	mV
V_{IMON_10A}		I_{OUT} = 10 A, Voltage is Referenced to REFIN Pin	47.5	50	52.5	mV
V_{IMON_20A}		I_{OUT} = 20 A, Voltage is Referenced to REFIN Pin	95	100	105	mV
FAULT REPORT						
V_{FAULT}	Fault Report Voltage		3			V
T_{D_FAULT}	Fault Report Delay Time			100		ns
OVER−TEMPERATURE PROTECTION (OTP) FAULT						
OTP	Over−Temperature Protection Accuracy	Driver IC Temperature	136	140	143	°C
OTP_hysteresis	OTP Hysteresis	Driver IC Temperature		15		°C
HS CYCLE−BY−CYCLE I−LIMIT						
$t_{D\_Ilimit-COMP}$	I−limit Comparator Input−Output Propagation Delay	Input Signal = 380 mV, dv / dt = 0.2 mV / nsec		60		ns
t_{BLANK_Ilimit}	I−limit Blanking Time	De−glitch Filter (Blanking) Time for I−Limit Comparator Trip		33		ns
I_{LIM}	FDMF5075 Over−Current Protection Accuracy	$T_A = T_J$ = 25° to 125°C	29			A
I_{LIM_HYS}	OCP Hysteresis			15		A
NEGATIVE OVER−CURRENT (NOCP) FAULT						
I_{NOCP_LOW}	NOCP Trip LOW Level		−30	−25	−20	A
HS−SHORT DETECT FAULT						
V_{HS_SHORT}	HS_short Comparator Reference Voltage			0.2		V
$t_{BLANK\_HS-short}$	HS Short Detect Blanking Time	Blanking Time Needed for Noise			50	ns
BOOT DIODE						
V_F	Forward−Voltage Drop	I_F = 10 mA		0.35		V
V_R	Breakdown Voltage	I_R = 1 mA	30			V

TYPICAL PERFORMANCE CHARACTERISTICS

Test conditions: V_{IN} = 12 V, V_{CC} = 5 V, V_{OUT} = 1.0 V, L_{OUT} = 150 nH, T_A = +25°C and natural convection cooling unless otherwise noted.

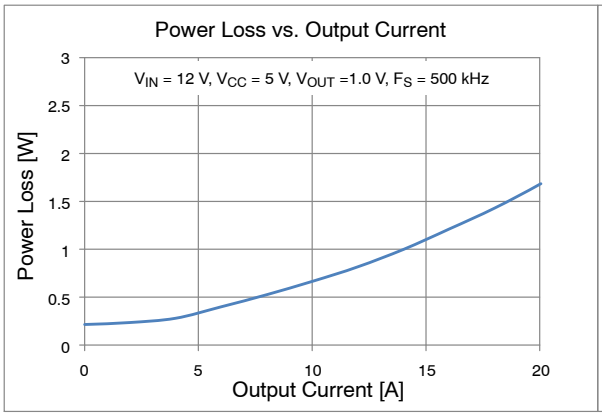


Figure 5. Power Loss vs. Output Current

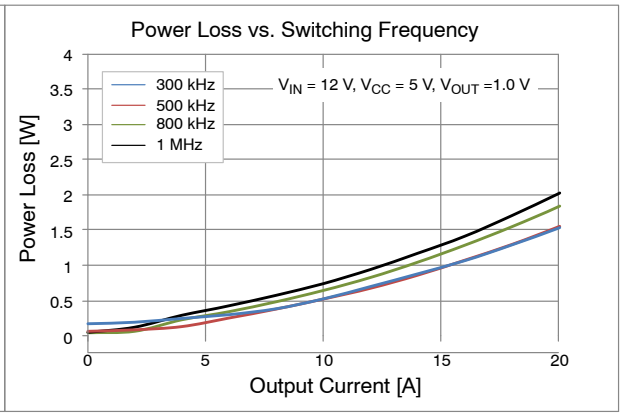


Figure 6. Power Loss vs. Switching Frequency

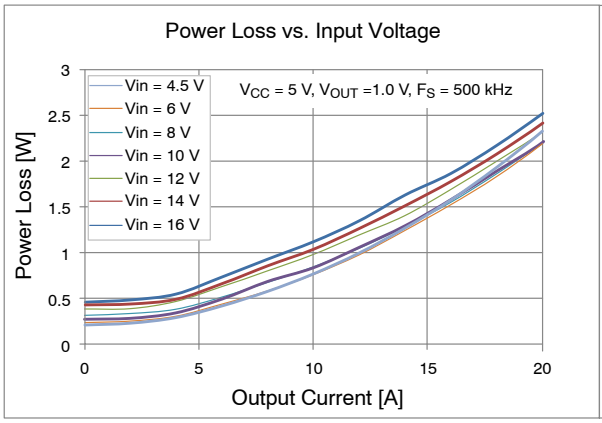


Figure 7. Power Loss vs. Input Voltage

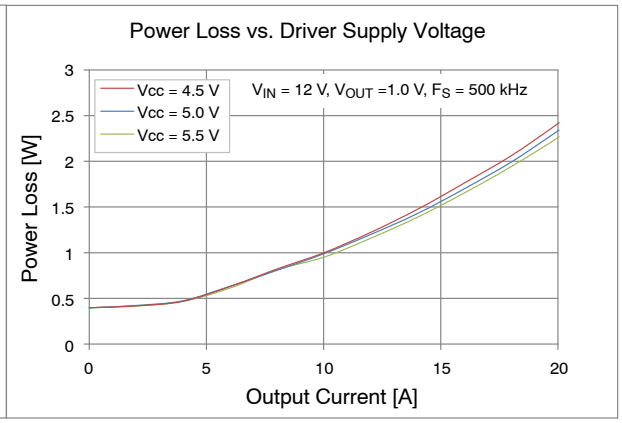


Figure 8. Power Loss vs. Driver Supply Voltage

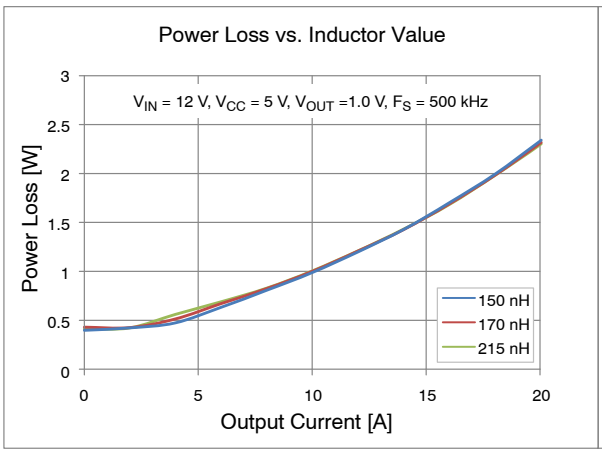


Figure 9. Power Loss vs. Output Inductor

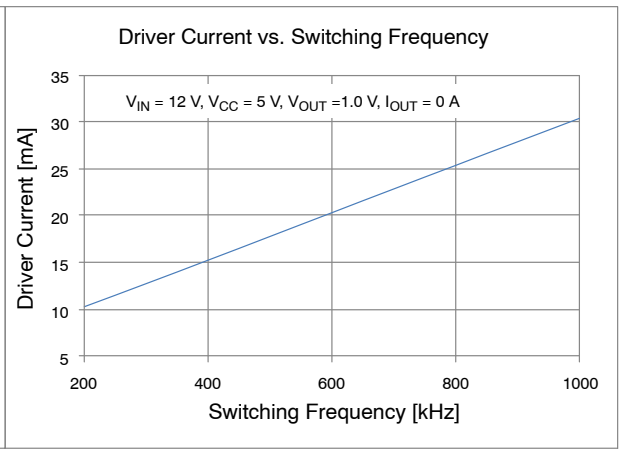


Figure 10. Driver Supply Current vs. Switching Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Test conditions: V_{IN} = 12 V, V_{CC} = 5 V, V_{OUT} = 1.0 V, L_{OUT} = 150 nH, T_A = +25°C and natural convection cooling unless otherwise noted.

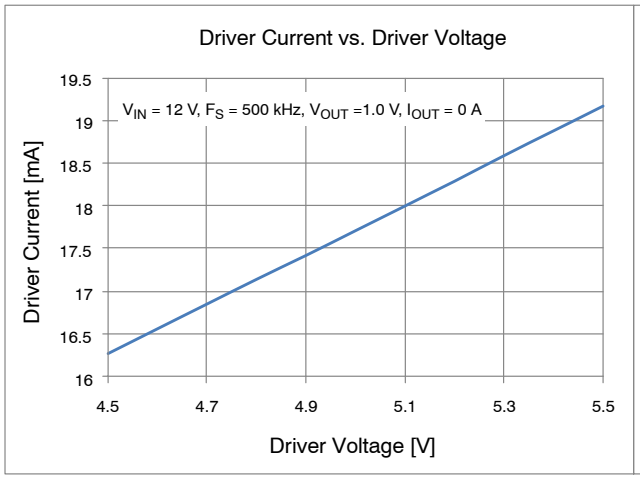


Figure 11. Driver Current vs. Driver Voltage

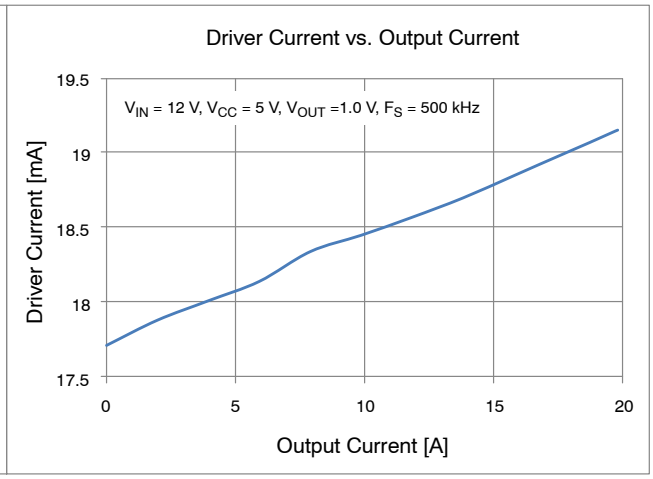


Figure 12. Driver Current vs. Output Current

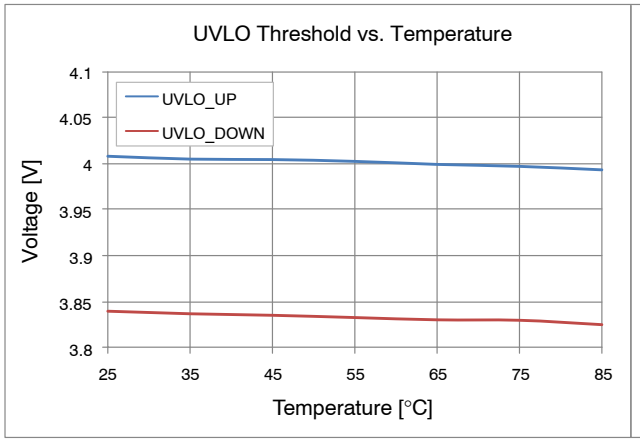


Figure 13. UVLO Threshold vs. Temperature

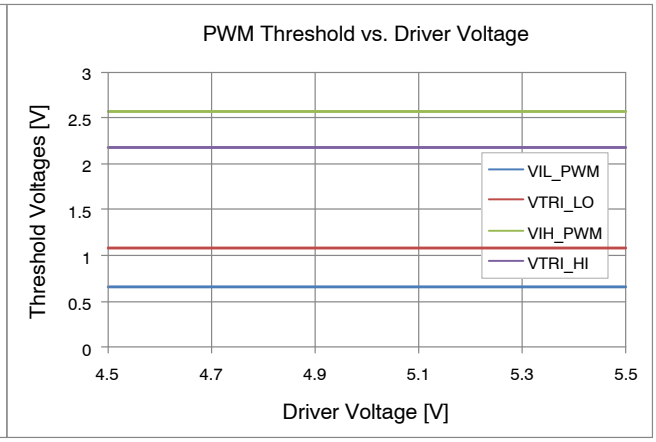


Figure 14. PWM Threshold vs. Driver Voltage

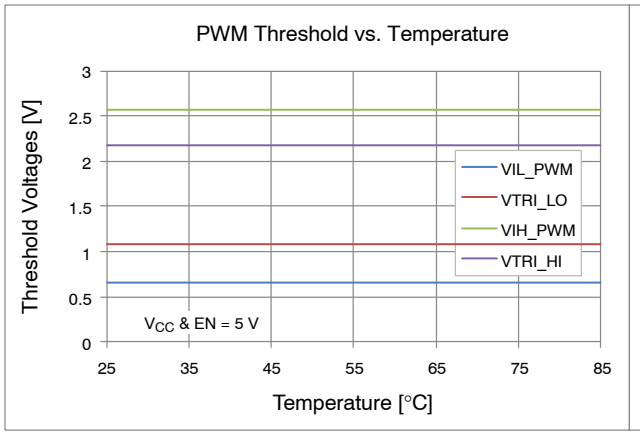


Figure 15. PWM threshold vs. Temperature

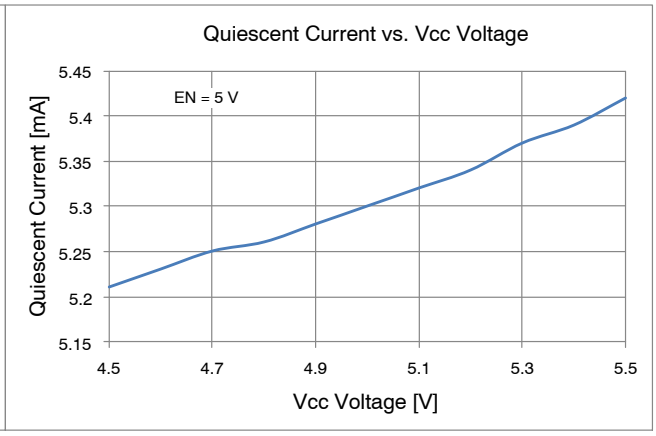


Figure 16. Quiescent Current vs. VCC Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Test conditions: V_{IN} = 12 V, V_{CC} = 5 V, V_{OUT} = 1.0 V, L_{OUT} = 150 nH, T_A = +25°C and natural convection cooling unless otherwise noted.

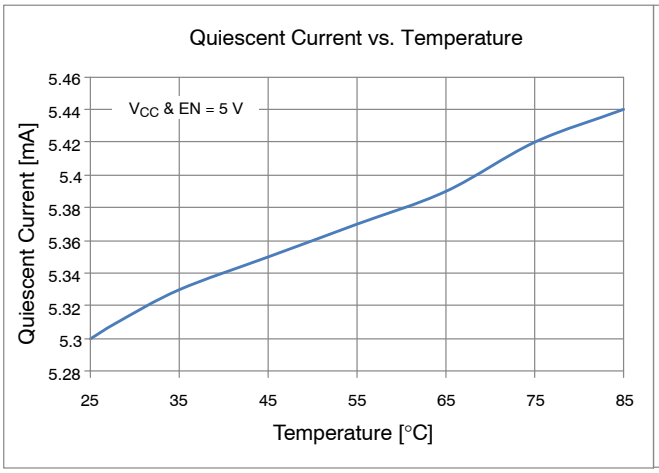


Figure 17. Quiescent Current vs. Temperature

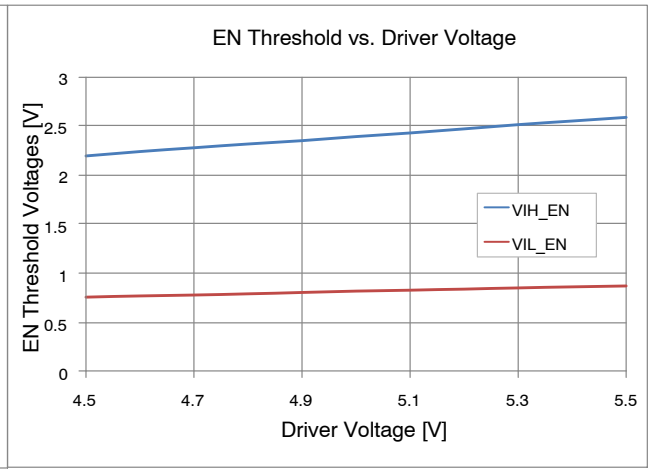


Figure 18. EN Threshold vs. Driver Voltage

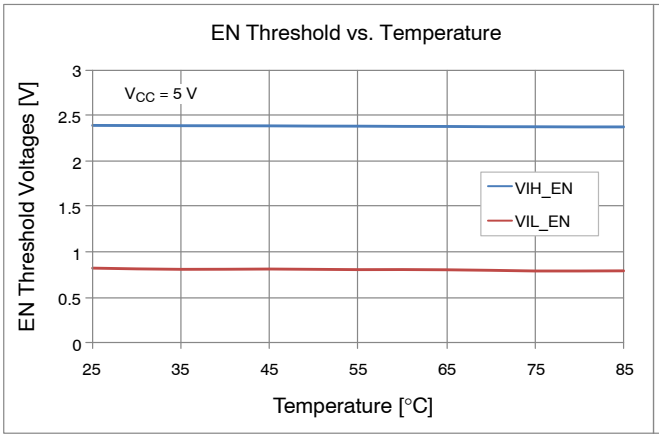


Figure 19. EN Threshold vs. Temperature

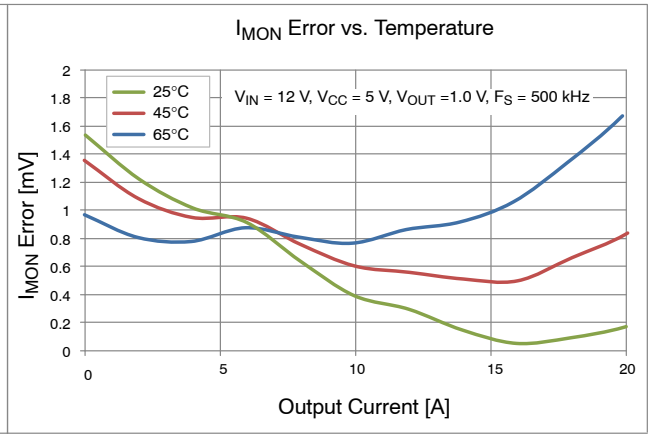


Figure 20. IMON Accuracy vs. Temperature

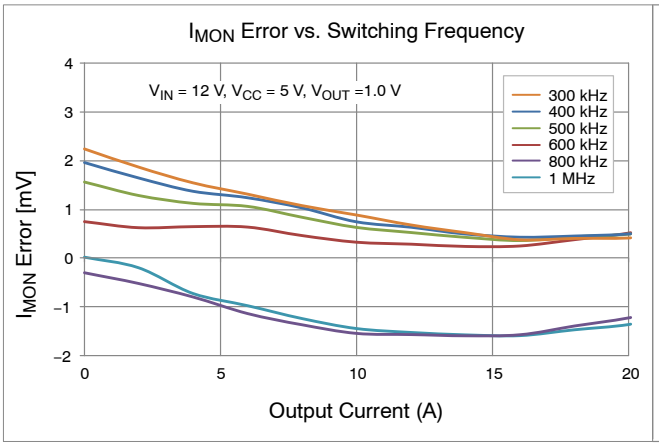


Figure 21. IMON Accuracy vs. Frequency

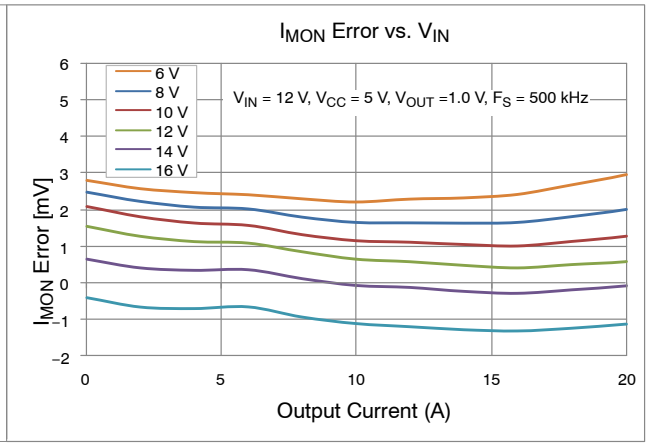


Figure 22. IMON Accuracy vs. VIN

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Test conditions: V_{IN} = 12 V, V_{CC} = 5 V, V_{OUT} = 1.0 V, L_{OUT} = 150 nH, T_A = +25°C and natural convection cooling unless otherwise noted.

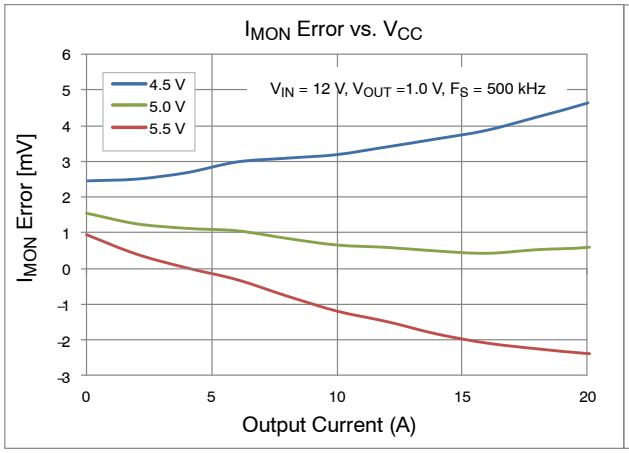


Figure 23. IMON Accuracy vs. V_{CC}

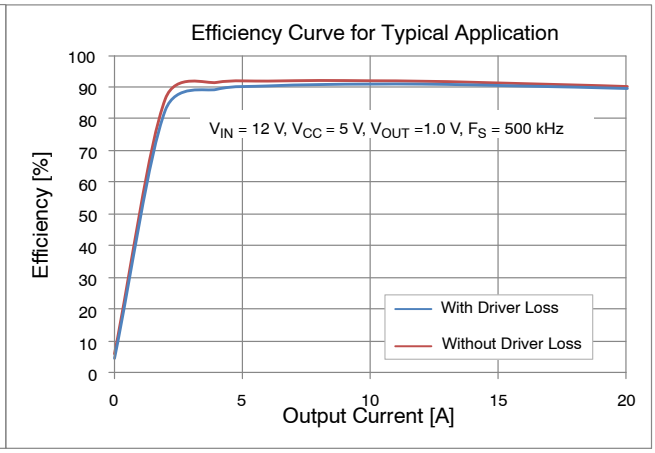


Figure 24. Efficiency Curve for Typical Application

FUNCTIONAL DESCRIPTION

The SPS FDMF5075 is a driver plus MOSFET module optimized for the synchronous buck converter topology. A PWM input signal is required to properly drive the high−side and the low−side MOSFETs. The part is capable of driving speed up to 1 MHz.

EN and UVLO

The SPS FDMF5075 is enabled by both EN pin input signal and V_{CC} UVLO. Table 5 summarizes the enable and disable logics. With EN low and V_{CC} UVLO, SPS is fully shut down. If V_{CC} is ready but EN is low, SPS goes to sleep mode with very low quiescent current, where only critical circuitry such as the bandgap and general housekeeping circuitry are alive. The part should also read fuses/program itself during this state.

Table 5. UVLO AND DRIVER STATE

VCC UVLO	EN	Driver State
0	X	Full driver shutdown (GL = 0), requires 40 μs for start−up
1	0	Partial driver shutdown (GL = 0), requires 30 μs for startup
1	1	Enabled (GL follow PWM)
X	Open/0	Disabled (GL = 0)

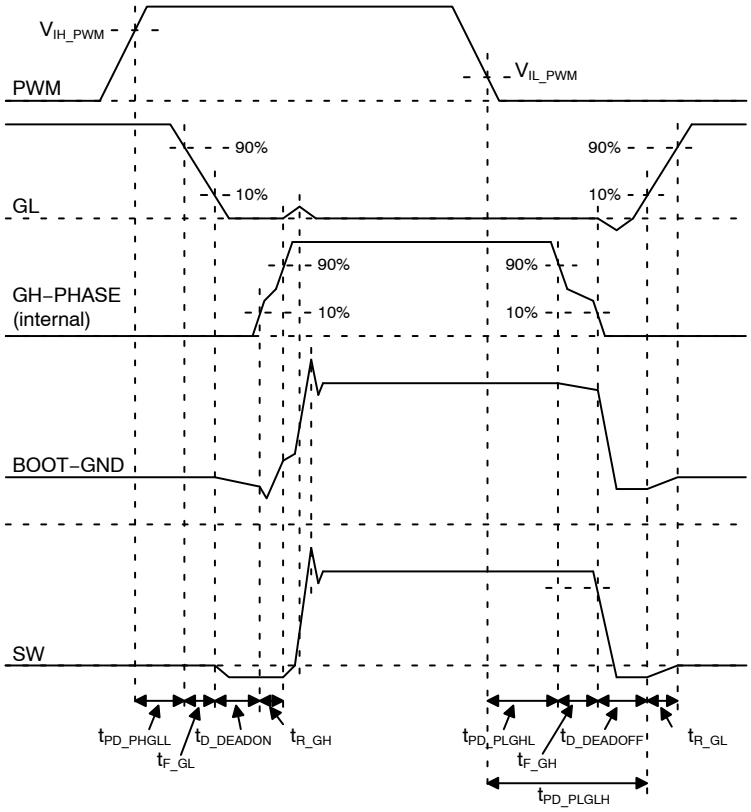
FDMF5075 needs 40 μs time to go from fully shutdown mode to power ready mode. The time is 30 μs to go from partial shutdown mode to power ready mode. Before power is ready, TMON pin is strongly pulled low with a 50 Ω resistor. As a result, TMON pin can also be used as a power ready indicator.

Tri−State PWM Input

The FDMF5075 incorporates a tri−state 3.3 V PWM input gate drive design. The tri−state gate drive has both logic HIGH and LOW levels, along with a tri−state shutdown window. When the PWM input signal enters and remains within the tri−state window for a defined hold−off time ($t_{D\_HOLD-OFF}$), both GL and GH are pulled LOW. This feature enables the gate drive to shut down both high−side and low−side MOSFETs to support features such as phase shedding, a common feature on multi−phase voltage regulators.

Table 6. ENABLE / PWM / TRI−STATE / OFF#LOGIC

Enable	PWM	GL
0	X	0
1	Tri−State	0
1	0	1
1	1	0



Notes: t_{PD_PHGLL} = PWM HIGH TO GL LOW, V_{IH_PWM} TO 90% GL
t_{F_GL} = 90% GL to 10% GL
t_{D_DEADON} = LS off to HS On Dead Time, 10% GL to 10% GH or BOOT = GND dip start point
t_{R_GH} = 10% gh to 90% GH or BOOT = GND dip start point to GL bounce start point
t_{PD_LPLGHL} = PWM LOW to GH LOW, V_{IL_PWM} to 90% GH or BOOT−GND decrease start point, $t_{PD\_PLGLH} - t_{D\_DEADOFF} - t_{F\_GH}$
t_{F_GH} = 90% GH to 10% GH, BOOT−GND decrease start point to 90% SW or GL dip start point
$t_{D\_DEADOFF}$ = HS Off to LS On Dead Time, 90% SW or GL dip start point to 10% GL
t_{R_GL} = 10% GL to 90% GL
t_{PD_PLGLH} = PWM LOW to GL HIGH, V_{IL_PWM} to 10% GL

Figure 25. PWM Timing Diagram

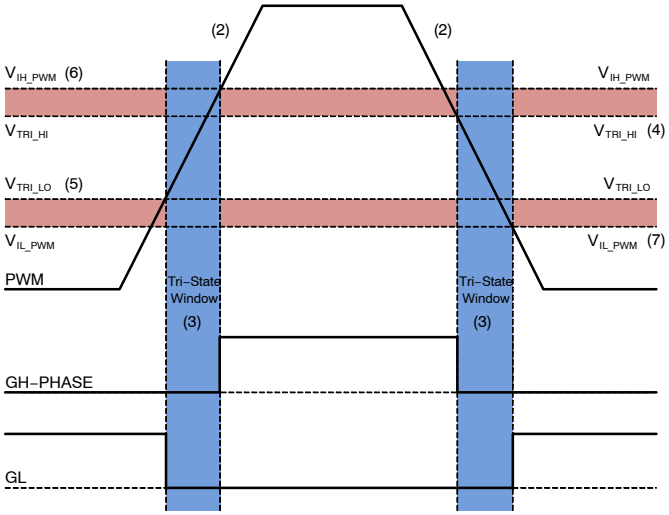


Figure 26. PWM Threshold Definition

NOTES:
2. The timing diagram in Figure 26 assumes very slow ramp on PWM.
3. Slow ramp of PWM implies the PWM signal remains within the Tri−state window for a time >>> $t_{D\_HOLD-OFF}$.
4. V_{TRI_HI} = PWM trip level to enter Tri−state on PWM falling edge.
5. V_{TRI_LO} = PWM trip level to enter Tri−state on PWM rising edge.
6. V_{IH_PWM} = PWM trip level to exit Tri−state on PWM rising edge and enter the PWM HIGH logic state.
7. V_{IL_PWM} = PWM trip level to exit Tri−state on PWM falling edge and enter the PWM LOW logic state.

Power Sequence

FDMF5075 requires four (4) input signals to conduct normal switching operation: V_{IN}, V_{CC}, PWM, and EN. All combinations of power sequences are available. The below example of a power sequence is for a reference application design:

- From no input signals
  - V_{CC} On: Typical 5 V_{DC}
  - EN HIGH: Typical 5 V_{DC}
  - V_{IN} On: Typical 12 V_{DC}
  - PWM Signaling: 3.3 V HIGH / 0 V LOW

The VIN pins are tied to the system main DC power rail.

The EN pin can be tied to the V_{CC} rail with an external pull−up resistor and it will maintain HIGH once the V_{CC} rail turns on. Or the EN pin can be directly tied to the PWM controller for other purposes.

High−Side Driver

The high−side driver (HDRV) is designed to drive a floating N−channel MOSFET (Q1). The bias voltage for the high−side driver is developed by a bootstrap supply circuit, consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, the SW node is held at PGND, allowing C_{BOOT} to charge to VCC through the internal bootstrap diode. When the PWM input goes HIGH, HDRV begins to charge the gate of the high−side MOSFET (internal GH pin). During this transition, the charge is removed from the C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, SW rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to SW. C_{BOOT} is then recharged to VCC when the SW falls to PGND. HDRV output is in phase with the PWM input. The high−side gate is held LOW when the driver is disabled or the PWM signal is held within the 3−state window for longer than the 3−state hold−off time, $t_{D\_HOLD-OFF}$.

Low−Side Driver

The low−side driver (LDRV) is designed to drive the gate−source of a ground referenced low $R_{DS(ON)}$ N−channel MOSFET (Q2). The bias for LDRV is internally connected between VCC and PGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled, LDRV is held LOW.

Dead−Times

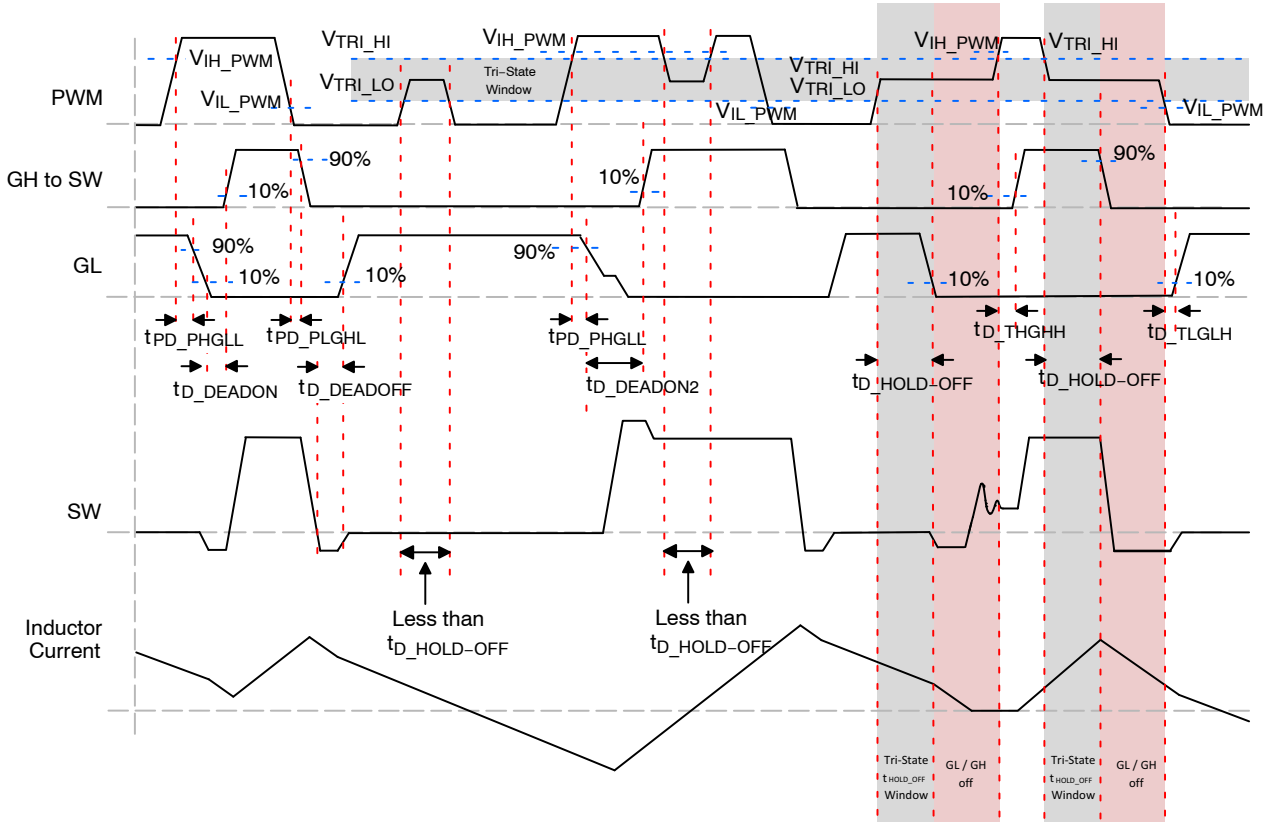
The driver IC design ensures minimum MOSFET dead times, while eliminating potential shoot−through (cross−conduction) currents. To ensure optimal module efficiency, body diode conduction times must be reduced to the low nano−second range during CCM and DCM operation. Delay circuitry is added to prevent gate overlap during both the low−side MOSFET off to high−side MOSFET on transition and the high−side MOSFET off to low−side MOSFET on transition.

Exiting Tri−State Condition

When exiting a valid Tri−state condition, the gate driver of the FDMF5075 follows the PWM input command. If the PWM input goes from Tri−state to LOW, the low−side MOSFET is turned on. If the PWM input goes from Tri−state to HIGH, the high−side MOSFET is turned on. This is illustrated in Figure 27.

Boot Capacitor Refresh

FDMF5075 monitors the low Boot−SW voltage. If EN and VCC are ready, but the voltage across the boot capacitor voltage is lower than 3.1 V, FDMF5075 ignores the PWM input signal and starts the boot refresh circuit. The boot refresh circuit turns on the low side MOSFET with a 100 ns ~ 200 ns narrow pulse in every 7 ~ 14 μs until Boot−SW voltage is above 3.8 V.



Notes:

t_{PD_xxx} = propagation delay from external signal (PWM, SMOD#, etc.) to IC generated signal.
Example (t_{PD_PHGLL} − PWM going HIGH to LS V_{GS}(GL) going LOW).
t_{D_xxx} = delay from IC generated signal to IC generated signal. Example (t_{D_DEADON} − LS V_{GS} LOW to HS V_{GS} HIGH

PWM

t_{PD_PHGLL} = PWM rise to LS V_{GS} fall, V_{IH_PWM} to 90% LS V_{GS}
t_{PD_PLGHL} = PWM fall to HS V_{GS} fall, V_{IL_PWM} to 90% HS V_{GS}
t_{PD_PHGHH} = PWM rise to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS} (SMOD# held LOW)

Exiting Tri−State

t_{PD_TSGHH} = PWM Tri−stte to HIGH to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS}
t_{PD_TSGLH} = PWM Tri−state to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

Dead Times

t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS−comp trip value to 10% HS V_{GS}
$t_{D\_DEADOFF}$ = VSWH fall to LS V_{GS} rise, SW−comp trip value to 10% LS V_{GS}

Figure 27. PWM HIGH / LOW / Tri−State Timing Diagram

Current Monitor (IMON)

The SPS current monitor accurately senses high−side and low−side MOSFET currents. The currents are summed together to replicate the output filter inductor current. The signal is reported from the SPS module in the form of a 5 μA/A current signal ($I_{IMON-REFIN}$). The IMON signal will be referenced to an externally supplied signal (REFIN) and differentially sensed by an external analog / digital PWM controller.

The motivation for the IMON feature is to replace the industry standard output filter DCR sensing, or output current sense using an external precision resistor. Both techniques are lossy and lead to reduced system efficiency. Inductor DCR sensing is also notoriously inaccurate for low value DCR inductors. Figure 28 shows a comparison between conventional inductor DCR sensing and the unique IMON feature.

The accuracy on IMON signal is ± 5 % from 10 A to 30 A output current. For the SPS module, parameters that can affect IMON accuracy are tightly controlled and trimmed at the MOSFET/IC production stage. The user can easily incorporate the IMON feature and accuracy replacing the traditional current sensing methods in multi−phase VR applications.

The REFIN voltage is an externally supplied DC voltage. The DC voltage can be supplied from any DC rail capable of supplying 100 μA, such as a PWM controller or other power rail in system.

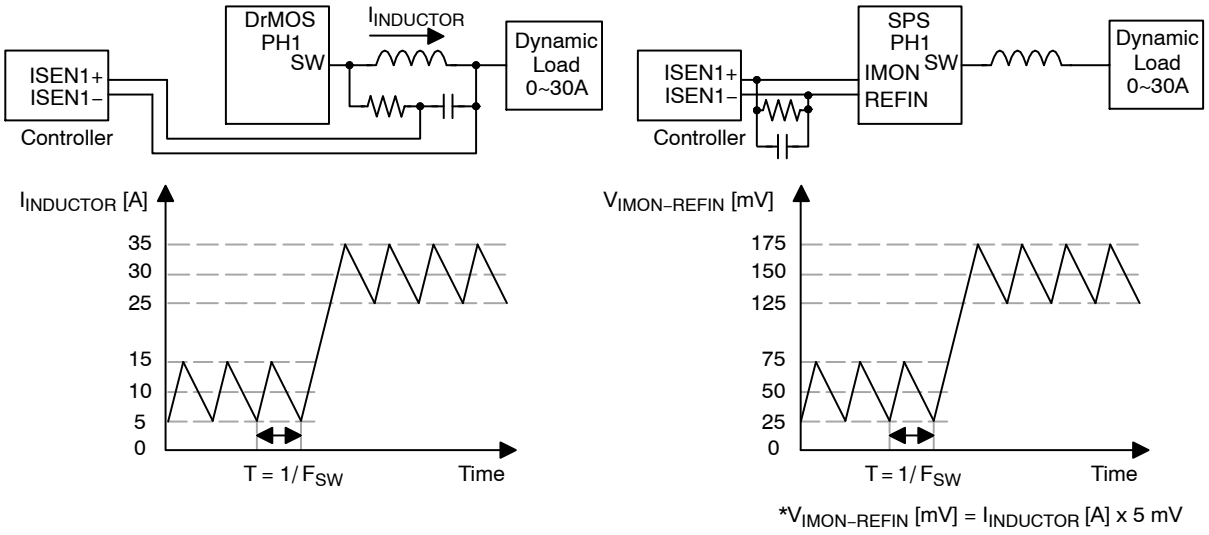


Figure 28. DrMOS with Inductor DCR Sensing vs. SPS with IMON

Temperature Monitor / Fault Flag (TMON / FAULT)

The TMON/FAULT pin on FDMF5075 is a thermal monitor output in normal operation. Before power is ready, TMON pin is strongly pulled low with a 50 Ω resistor. As a result, it can be used as a power ready indicator. Also, this pin is used as a module FAULT flag pin if there is OCP, OTP, or high side FET shorted.

The TMON pin output is a Proportional to Absolute Temperature (PTAT) voltage sourced signal referenced to AGND when no module FAULT is present. It will typically output 0.6 V at 0°C and 1.8 V at 150°C with 8 mV / °C typ. slope.

TMON pins from multiple FDMF5075 modules (used in multi−phase topologies) can be tied together to share a common thermal bus. Operating with this configuration will force the thermal bus signal to report the highest voltage output TMON signal to the controller (highest temperature). The TMON output has low output impedance when sourcing current and high output impedance when sinking current.

The TMON signal reported from the module pin is a buffered version of an internal TMON signal. Configuring the SPS module to share a common thermal bus will still permit each module to safely monitor its own temperature since the internal TMON signal is unaffected by the common thermal bus configuration.

The TMON voltage has a slope defined as following equation.

The TMON pin pulls to an internal 3.0 V typical rail capable of sourcing 5 mA current during any of the FAULT conditions listed below.

$$\frac{V_{TMON}[V]}{T_J[°C]} = \frac{1.75\ V - 0.6\ V}{140°C - 0°C} = 8[mV/°C] \qquad \text{(eq. 1)}$$

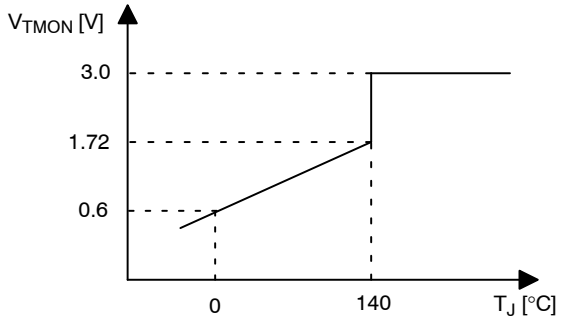


Figure 29. SPS T_J vs. V_{TMON}

Over−Temperature Protection (OTP)

An over temperature event is considered catastrophic in nature. OTP raises fault flag HIGH once TMON exceeds 140°C temperature. Driver still responds to PWM commands (NO tri−state shutdown). Once TMON falls below 125°C, fault flag is cleared internally by driver IC.

Over−Current Protection (OCP)

The FDMF5075 has cycle−by−cycle over−current protection. If current exceeds the OCP threshold, HS FET is gated off regardless of PWM command. HS FET cannot be gated on again until the current is less than the OCP threshold with a hysteresis.

Fault flag will be pulled HIGH after 10 consecutive cycle−by−cycle OCPs are detected. Fault flag will clear once OCP is NOT detected. Module never shuts down (nor does it disable HDRV/LDRV outputs – i.e., enter internal tri−state) and always responds to PWM commands (but driver will still truncate HS on time when PWM = HIGH and ILIM is detected).

High−Side MOSFET Short Fault

A high−side MOSFET short fault feature is added to the FDMF5075. If a high−side MOSFET short fault is detected, the driver will pull the TMON / FAULT pin HIGH and continue to respond to PWM commands. Fault flag will clear once HS short is NOT detected or 5 V_{CC} power re−cycle, EN toggle.

Negative−OCP

The FDMF5075 can detect large negative inductor current and protect the low side MOSFET. Once this negative current threshold is detected, the SPS module blanks the LS on−time pulse for 200 ns. If PWM remains low, the LS FET will turn back on again at the end of the 200 ns. If the PWM goes high during the 200 ns period, the HS FET will turn on normally.

APPLICATION INFORMATION

Decoupling Capacitor for VCC

For the supply input (VCC pin), local decoupling capacitor is required to supply the peak driving current and to reduce noise during switching operation. Use at least 0.68 ~ 2.2 μF / 0402 ~ 0603 / X5R ~ X7R multi−layer ceramic capacitor for the power rail. Keep this capacitor close to the VCC pin and AGND copper planes. If it needs to be located on the bottom side of board, put through−hole vias on each pad of the decoupling capacitor to connect the capacitor pad on bottom with VCC pin on top.

The supply voltage range on VCC is 4.5 V ~ 5.5 V, typically 5 V for normal applications.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}). A bootstrap capacitor of 0.1 ~ 0.22 μF / 0402 ~ 0603 / X5R ~ X7R is usually appropriate for most switching applications. A series bootstrap resistor may be needed for specific applications to lower high−side MOSFET switching speed. The boot resistor is required when the SPS is switching above 15 V V_{IN}; when it is effective at controlling V_{SW} overshoot. R_{BOOT} value from zero to 6 Ω is typically recommended to reduce excessive voltage spike and ringing on the SW node. A higher R_{BOOT} value can cause lower efficiency due to high switching loss of high−side MOSFET.

Do not add a capacitor or resistor between the BOOT pin and GND.

IMON (Output) / REFIN (Input)

An externally generated DC voltage from either a controller or other power rail is required to supply REFIN voltage for IMON−REFIN signal. The REFIN voltage must be set to be within the compliant range from 0.6 ~ 2.0 V DC. It is recommended to add a PCB place holder for a small size 1 nF ~ 1 μF capacitor close to the REFIN pin and AGND to reduce switching noise injection.

It is also recommended to add a small 10 ~ 47 pF capacitor in parallel with the IMON resistor from IMON to REFIN. This capacitor can help reduce switching noise coupling onto the IMON signal. The place of the IMON resistor and cap should be close to the controller, not the SPS to improve the sensing accuracy.

TMON (Output)/ FAULT (Output)

A 0.1 nF to 1 nF capacitor, C_{TMON}, can be placed from TMON to AGND and used to minimize switching noise injection onto TMON pin.

An RC low−pass filter with ~ 1 kΩ and ~ 1 nF can be placed on TMON/ FAULT pin to AGND to reduce switching noise injection into TMON/ FAULT pin.

PCB LAYOUT GUIDELINE

All of the high−current paths; such as VIN, SW, VOUT, and GND coppers; should be short and wide for low parasitic inductance and resistance. This helps achieve a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Input ceramic bypass capacitors must be close to the VIN and PGND pins. This reduces the high−current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

An output inductor should be located close to the FDMF5075 to minimize the power loss due to the SW copper trace. Care should also be taken so the inductor dissipation does not heat the SPS.

PowerTrench® MOSFETs are used in the output stage and are effective at minimizing ringing due to fast switching. In most cases, no RC snubber on SW node is required. If a snubber is used, it should be placed close to the SW and PGND pins. The resistor and capacitor of the snubber must be sized properly to not generate excessive heating due to high power dissipation.

Decoupling capacitor on VCC and BOOT capacitor should be placed as close as possible to the VCC ~ AGND and BOOT ~ PHASE pin pairs to ensure clean and stable power supply. Their routing traces should be wide and short to minimize parasitic PCB resistance and inductance.

The board layout should include a placeholder for small−value series boot resistor on BOOT ~ PHASE. The boot−loop size, including series R_{BOOT} and C_{BOOT}, should be as small as possible.

A boot resistor may be required when the SPS is operating above 15 V V_{IN} and it is effective to control the high−side MOSFET turn−on slew rate and SW voltage overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative V_{SW} ringing. Inserting a boot resistance lowers the SPS module efficiency. Efficiency versus switching noise must be considered. R_{BOOT} values from 0.5 Ω to 6.0 Ω are typically effective in reducing V_{SW} overshoot.

The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is not recommended since this adds extra parasitic inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SW} ringing.

PGND pad and pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noisy and transient offset voltage level between PGND and AGND. This could lead to faulty operation of gate driver and MOSFETs.

Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add any additional capacitors between BOOT to PGND. This may lead to excess current flow through the BOOT diode, causing high power dissipation.

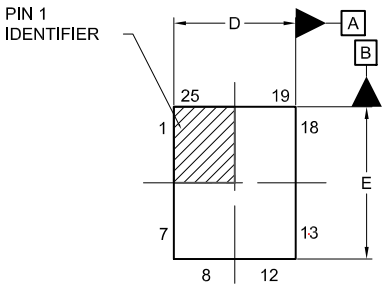
Put multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to evenly distribute current flow and heat conduction. Do not put too many vias on the SW copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one SW node copper on the top layer and put no vias on the SW copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high−frequency components; such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective SPS module pins as possible on the top layer of the PCB. If this is not feasible, they can be placed on the board bottom side and their pins connected from bottom to top through a network of low−inductance vias.

Table 7. ORDERING INFORMATION

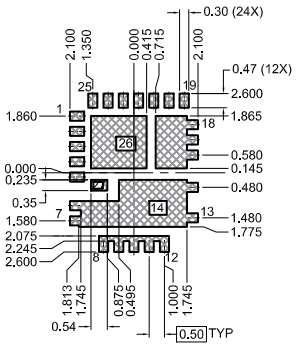
Device	Output Configuration	Marking	Package	Shipping
FDMF5075	High−Side and Low−Side	5075	PQFN	Tape and Reel

PACKAGE DIMENSIONS

PQFN25 4x5, 0.5P
CASE 483BV
ISSUE A

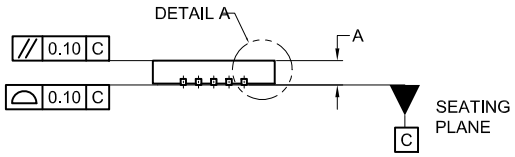


TOP VIEW

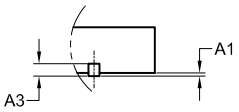


RECOMMENDED
MOUNTING FOOTPRINT

NOTES: UNLESS OTHERWISE SPECIFIED
1) THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-220.
2) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DO NOT EXCEED 0.10 MM
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) DRAWING CONFORMS TO ASME Y14.5M-2009.

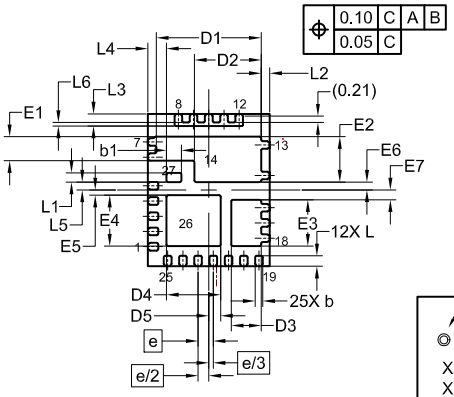


SIDE VIEW

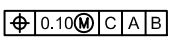


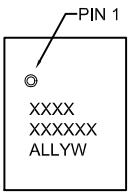
DETAIL A

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
b1	0.44	0.49	0.54
D	3.90	4.00	4.10
D1	3.34	3.44	3.54
D2	2.09	2.19	2.29
D3	0.88	0.98	1.08
D4	1.68	1.78	1.88
D5	0.34	0.39	0.44
E	4.90	5.00	5.10
E1	0.69	0.79	0.89
E2	1.39	1.49	1.59
E3	1.42	1.52	1.62
E4	1.57	1.67	1.77
E5	0.12	0.17	0.22
E6	0.21	0.26	0.31
E7	0.27	0.32	0.37
e	0.50 BSC		
e/2	0.35 BSC		
e/3	0.15 BSC		
L	0.29	0.34	0.39
L1	0.25	0.30	0.35
L2	0.23	0.28	0.33
L3	0.35	0.40	0.45
L4	0.56	0.61	0.66
L5	0.21	0.26	0.31
L6	0.07	0.12	0.17



BOTTOM VIEW





GENERIC MARKING DIAGRAM

A	= LOCATION CODE ASSY
LL	= ASSY LOT TRACEABILITY
Y	= YEAR CODE
W	= WORK WEEK CODE
XXXX	= DEVICE CODE
XXXXXX	= DEVICE CODE

*THIS INFORMATION IS GENERIC. PLEASE REFER TO DEVICE DATA SHEET FOR ACTUAL PART MARKING.

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