FS791/92/94

Low EMI Spectrum Spread Clock

Features

- **Spread Spectrum Clock Generator (SSCG) with 1x, 2x and 4x outputs**
- **80- to 140-MHz operating frequency range**
- **Modulates external clocks including crystals, crystal oscillators, and ceramic resonators**
- **Programmable modulation with simple R-C external loop filter (LF)**
- **Center spread modulation**
- **3–5 Volt power supply**
- **TTL/CMOS compatible outputs**
- **Low short-term jitter**
- **Low Power Dissipation;**
  - **3.3 VDC = 73 mW—typical**
  - **5.0 VDC = 225 mW—typical**
- **Available in 8-pin SOIC package**

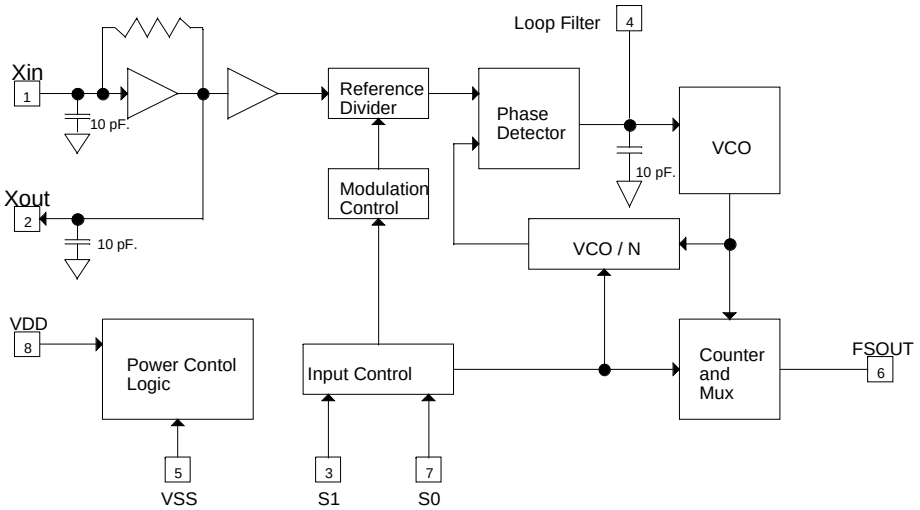
Applications

- **Desktop/Notebook computers**
- **VGA, XGA, and SXGA LCD displays**
- **High-speed printers and copiers**
- **CD-ROM, VCD, and DVD**
- **Embedded systems**
- **Networking, LAN/WAN**
- **Modems**

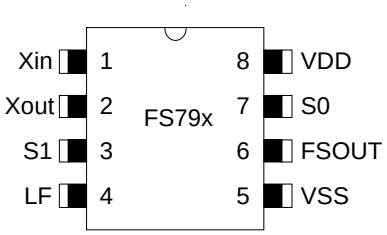
Benefits

- **Programmable EMI reduction**
- **Fast time-to-market**
- **Lower cost of compliance**
- **No degradation in Rise/Fall time**
- **Lower component and PCB layer count**

Block Diagram



Pin Configuration



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Pin Description

Pin	Name	I/O	Type	Description
1,2	Xin/Xout	I/O	analog	Pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. XIN may be connected to TTL/CMOS external clock other than crystal, leave XOUT (pin 2) unconnected.
3,7	S1/S0	I	CMOS/TTL	Digital control inputs used to select the input frequency range and output frequency scaling. Refer *Table 1* for selection. S1 has internal pull-up(1) and S0 has internal pull-down(0).
4	LF	I	Analog	Loop filter. Single ended three-state output of the phase detector. A single-pole low-pass filter is connected to the loop filter (LF).
5	VSS	P	Power	Power Supply Ground.
6	FSOUT	O	CMOS/TTL	Modulated Clock Output. The output frequency is centered on and a multiple of the input (Xin) as follows: FS791 = 1X; FS792 = 2X; FS794 = 4X
8	VDD	P	Power	Positive Power Supply.

Table 1. Output Frequency Selection – FSOUT SSCG (Modulated Output Clock) Product Selection

Product Number	FSOUT Frequency Scaling	Description
FS791	1X	1X Modulated Frequency of Input Clock
FS792	2X	2X Modulated Frequency of Input Clock
FS794	4X	4X Modulated Frequency of Input Clock

General Description

The Cypress FS791/2/4 are Spread Spectrum Clock Generator ICs (SSCG) designed for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital systems.

The FS791/2/4 SSCG clocks use an Cypress proprietary technology to modulate the input clock frequency, FSOUT, by modulating the frequency of the digital clock. By modulating the reference clock the measured EMI at the fundamental and harmonic frequencies of FSOUT is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements without degrading digital waveforms.

The FS791/2/4 are designed to operate over a very wide range of input frequencies and provide 1x, 2x, and 4x modulated clock outputs.

The bandwidth of the frequency spread at FSOUT is determined by the values of the loop filter components. The modulation rate is determined internally by the input frequency and the selected input frequency range.

The bandwidth of these products can be programmed from as little as 0.6% up to as much as 4.0% by selecting the proper loop filter value. Refer to the Loop Filter Selection chart on page 4 for recommended values. Due to a wide range of application requirements, an external loop filter (LF) is used on the FS79x products.

The user can select the exact amount of frequency modulation suitable for the application. Using a fixed internal loop filter would severely limit the use of a wide range of modulation bandwidths (Spread%) to a few discrete values.

The Cypress FS791/2/4 Spread Spectrum Clock Generator (SSCG) products are versatile devices to use in a wide range of applications.

Refer to FS781/2/4 products for applications requiring a 6 to 82 MHz frequency range.

Absolute Maximum Ratings[1, 2]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Operating Voltage	3.0	6.0	VDC
VIR_{VSS}	Input, relative to V_{SS}	–0.3	V_{DD} + 0.3	VDC
VOR_{VSS}	Output, relative to V_{SS}	–0.3	V_{DD} + 0.3	VDC
ΔV_{PP}	AV_{DD} relative to DV_{DD}	–100	+100	mV
ΔV_{SS}	AV_{SS} relative to DV_{SS}	–100	+100	mV
T_{OP}	Temperature, operating	0	+70	°C
T_{ST}	Temperature, Storage	–65	+150	°C

Table 2. DC Electrical Characteristics: Test measurements performed at V_{DD} = 3.3V and 5.0V ±10%, Xin = 100 MHz, Ta = 0°C to 70°C

Parameter	Description	Min.	Typ.	Max.	Unit.
V_{IL}	Input Low Voltage			0.8	VDC
V_{IH}	Input High Voltage	2.0			VDC
I_{IL}	Input Low Current			100	µA
I_{IH}	Input High Current			100	µA
V_{OL}	Output Low Voltage I_{OL}= 10 mA, V_{DD} = 5V			0.4	VDC
V_{OH}	Output High Voltage I_{OH} = 10 mA, V_{DD} = 5V	V_{DD} – 1.0			VDC
V_{OL}	Output Low Voltage I_{OL} = 6 mA, V_{DD} = 3.3V			0.4	VDC
V_{OH}	Output High Voltage I_{OH} = 5 mA, V_{DD} = 3.3V	2.4			VDC
C_{in1}	Input Capacitance (Pin-1)	6	8	10	pF
C_{in2}	Output Capacitance (Pin-2)	6	8	10	pF
I_{CC}	5-Volt Dynamic Supply Current (C_L = O)		45	55	mA
I_{CC}	3.3-Volt Dynamic Supply Current (C_L = O)		22	28	mA
I_{SC}	Short Circuit Current (FM-OUT)		25		VDC

Table 3. Timing Characteristics: Test measurements performed at V_{DD} = 3.3V and 5.0V ±10%, Ta = 0°C to 70°C, CL = 20 pF, Xin = 100 MHz

Parameter	Description	Min.	Typ.	Max.	Unit
t_{TLH}	Output Rise Time Measured at 10% - 90% @ 5 VDC	2.0	2.2	2.5	ns
t_{THL}	Output Fall Time Measured at 10% - 90% @ 5 VDC	1.7	2.0	2.2	ns
t_{TLH}	Output Rise Time Measured at 0.8V - 2.0V @ 5 VDC	0.50	0.65	0.75	ns
t_{THL}	Output Fall Time Measured at 0.8V - 2.0 V @ 5 VDC	0.50	0.65	0.75	ns
t_{TLH}	Output Rise Time Measured at 10% - 90% @ 3.3 VDC	2.60	2.65	2.90	ns
t_{THL}	Output Fall Time Measured at 10% - 90% @ 3.3 VDC	2.00	2.10	2.20	ns
t_{TLH}	Output Rise Time Measured at 0.8V - 2.0V @ 3.3 VDC	0.80	0.95	1.10	ns
t_{THL}	Output Fall Time Measured at 0.8V - 2.0 V @ 3.3 VDC	0.78	0.85	0.90	ns
T_{symF1}	Output Duty Cycle	45	50	55	%
t_{j1s}	Peak-to Peak Jitter One Sigma	-	150	250	ps

Note:

1. **Single Power Supply:** The voltage on any input or I/O pin cannot excceed the power pin during power-up.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range, $V_{SS} < (V_{in}$ or $V_{out}) < V_{DD}$. All digital inputs are tied HIGH or LOW internally. Refers to electrical specifications for operating supply range.

Table 4. Range Selection Table[3]

Part Number	S1 (Pin 3)	S0 (Pin 7)	Fin (Pin 1 & 2)	Modulation Rate	FSOUT (Pin 6)
FS791	1	1	80–140MHz	Fin/720	80–140MHz
FS792	1	0	40–70MHz	Fin/480	80–140MHz
FS794	0	1	20–35MHz	Fin/240	80–140MHz

Loop Filter Selection Chart

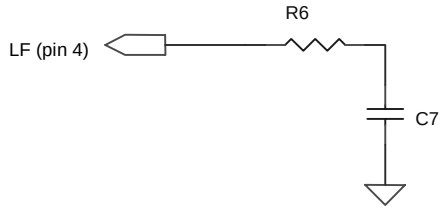


Figure 1. Loop Filter Selection

Table 5 provides a list of recommended loop filter values for the FS791/2/4. The FS79x products operate at both 3.3 and 5.0VDC. The loop filter shown in *Figure 1* is representative of the loop filter components in *Table 5*

Table 5. FS79x Recommended Loop Filter Values[4]

+3.3 to 5.0VDC, ±5% (R6 = 3.3K)				
Input (MHz)	BW = 1% (*note 5*)	BW = 2% (*note 5*)	BW = 3% (*note 5*)	BW = 4% (*note 5*)
All C7 capacitor values are in picofarads (pF)				
80	1000	220	190	170
90	510	190	130	90
100	250	150	96	65
110	200	120	74	47
120	150	80	52	38
130	120	55	33	26
140	100	43	22	16

Notes:
3. Fin is the frequency of the crystal connected to pins 1 & 2 to form an oscillator circuit or the frequency of a clock source connected to pin 1, derived from other means. When the clock source is from other than a crystal, pin 2 must be left unconnected.
4. Component values are industry standards and are readily available from component suppliers.
5. All bandwidths indicated above are total peak-to-peak spread, example: 1% = +0.5% to –0.5% and 4% = +2.0% to –2.0%

SSCG Modulation Profile

The modulation frequency of the FS79x can be computed dividing the input frequency by this 720. The formula to compute the Modulation Frequency is Fm = fin / 720.

Example: Fin = 108 MHz
Range = 1,1
Fm = 108 MHz / 720 = 150 kHz

With the correct loop filter connected to pin 4, the following profile will provide the best EMI reduction. This profile can be seen on a Time Domain Analyzer. See *Figure 3*.

SSCG Theory of Operation

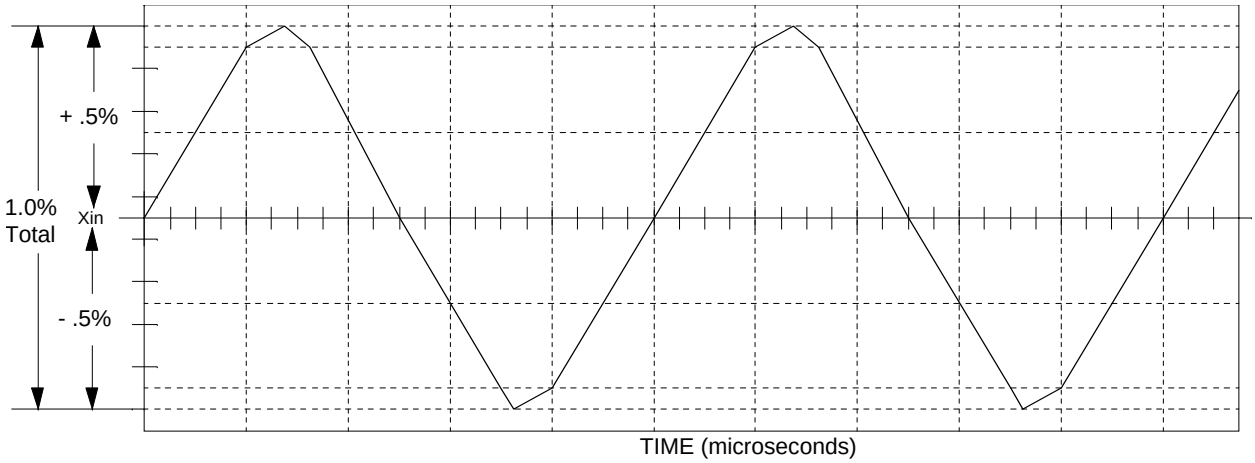


Figure 2. Frequency Profile in Time Domain

The FS791/2/4 devices are Phase-Locked Loop (PLL) type clock generators using Direct Digital Synthesis (DDS). By precisely controlling the bandwidth of the output clock, the FS791/792/794 products become Low EMI clock generators. The theory and detailed operation of these products will be discussed in the following sections.

EMI

All clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; 3rd, 5th, 7th etc. It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for Electro-Magnetic Interference (EMI). Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCBs etc. The FS791/2/4 products use the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q of the clock.

SSCG

The FS791/2/4 products use a unique method of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak-to-peak and cycle-to-cycle. The FS79x products take a narrow band digital reference clock in the range 80–140 MHz and produce a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to an SSCG clock, consider that we have a 100-MHz clock with a 50% duty cycle. From a 100-MHz clock we know the following;

Clock Frequency = fc = 100 MHz

Clock Period = Tc =1/100 MHz = 10 ns

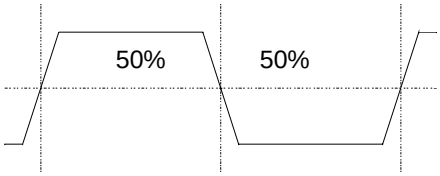


Figure 3. Unmodulated Clock

Consider that this 100-MHz clock is applied to the Xin input of the FS79x, either as an externally driven clock or as the result of a parallel resonant crystal connected to pins 1 and 2 of the FS79x. Also consider that the products are operating from a 5-volt DC power supply and the loop filter is set for a total bandwidth spread of 2%. Refer to *Table 5* on page 4.

From the above parameters, the output clock at FSOUT will be sweeping symmetrically around a center frequency of 100 MHz.

The minimum and maximum extremes of this clock will be +1.0 MHz and –1.0 MHz. So, we have a clock that is sweeping from 99.0 MHz to 101.0 MHz and back again. If we were to look at this clock on a spectrum analyzer we would see the picture in *Figure 4*. Keep in mind that this is a drawing of a perfect clock with no noise.

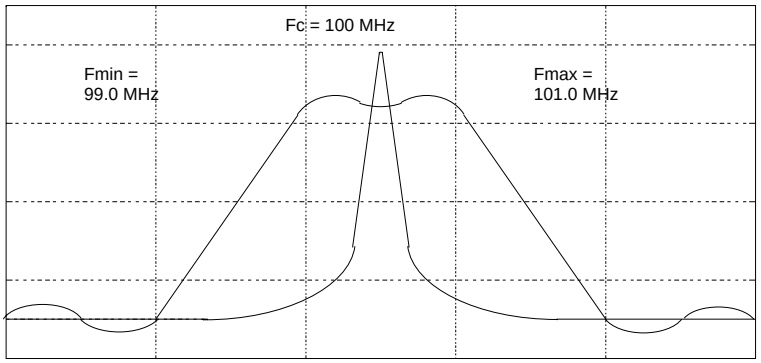


Figure 4. 100-MHz Spectrum

We see that the original 100-MHz reference clock is at the center Frequency, Cf, and the minimum and maximum extremes are positioned symmetrically about the center frequency. This type of modulation is called Center-Spread. *Figure 5* shows a 100-MHz clock, as it would be seen on an oscilloscope. The top trace is the non-modulated reference clock. The bottom trace is the modulated clock at pin 6. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock is increasing. The Tc measurements on the left and right of the bottom trace indicate the max. and min. extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this figure would show the clock going from min. extreme back to the high extreme**.**

Looking at *Figure 4*, you will note that the peak amplitude of the 100-MHz non-modulated clock is higher than the wideband modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. This figure refers to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the fundamental frequency is multiplied by the harmonic number. In other words, if the bandwidth of a 100-MHz clock is 2.0 MHz, the bandwidth of the 3rd harmonic will be 3 times 2.0, or 6.0 MHz. The amount of bandwidth is relative to the amount of energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Most applications will not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the 9th harmonic of a 100-MHz clock is 900 MHz. With a total spread of 2.0 MHz at 100 MHz, the spread at the 9th harmonic would be 18.0 MHz which greatly reduces the peak energy content. It is typical to see as much as 12 to 20 dB reduction at the higher harmonics, due to a modulated clock.

The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications will see a 2–3 dB reduction at the fundamental and as much as 8–10 dB reduction at the intermediate harmonics, 3rd, 5th, 7th etc. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 20 dB.

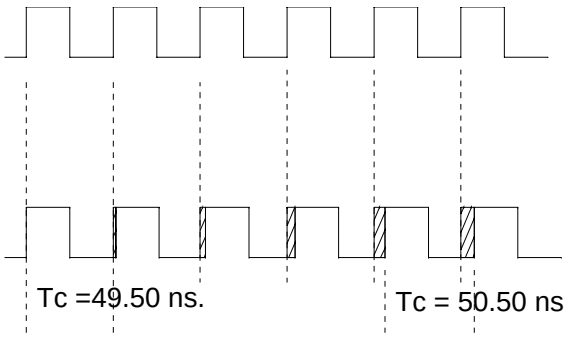


Figure 5. Period Comparison Chart

Application Notes and Schematics

The schematics below demonstrate the use of the FS791/FS792/FS794 in a practical application.

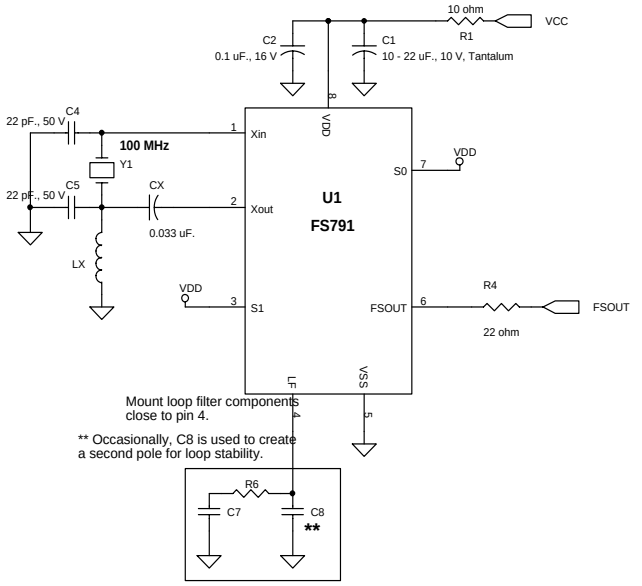


Figure 6.

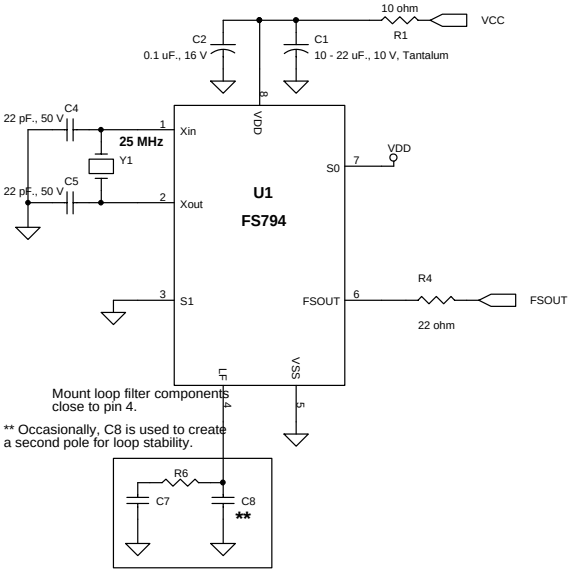


Figure 8.

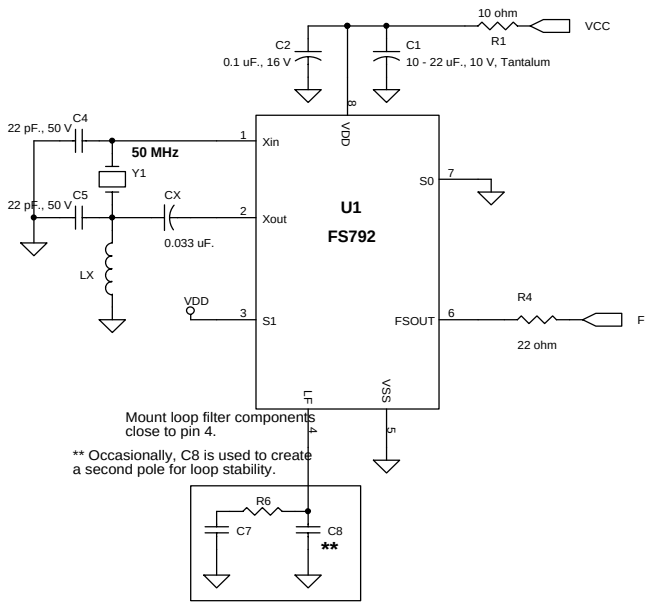


Figure 7.

The schematics on this page demonstrate how to use the FS791, FS792 and FS794 in a practical application.

Note that the crystal circuit in *Figure 6* and *Figure 7* are designed for a 3rd overtone crystal. This requires an inductor and DC blocking capacitor referenced as LX and CX in the above circuits.

Figure 8 at the right uses a 25-MHz crystal and assumes it is not a 3rd overtone cut. If it is a 3rd overtone crystal, LX and CX must be installed as in *Figure 6* and *Figure 7*.

Refer to the crystal or ceramic resonator manufacturer's specifications for the exact values of C4, C5 and LX. Cin (pin 1) and Cout (pin 2) = 8 pF each, which must be included in calculating the value of C4 and C5.

Ordering Information[6]

Part Number	Package Type	Product Flow
IMIFS791BZ	8 Pin SOIC	Commercial, 0° to 70°C
IMIFS791BZT	8 Pin SOIC - Tape and Reel	Commercial, 0° to 70°C
IMIFS792BZ	8 Pin SOIC	Commercial, 0° to 70°C
IMIFS792BZT	8 Pin SOIC - Tape and Reel	Commercial, 0° to 70°C
IMIFS794BZ	8 Pin SOIC	Commercial, 0° to 70°C
IMIFS794BZT	8 Pin SOIC - Tape and Reel	Commercial, 0° to 70°C

Note:
6. The ordering part number differs from the marking on the actual device.

Marking: Example:

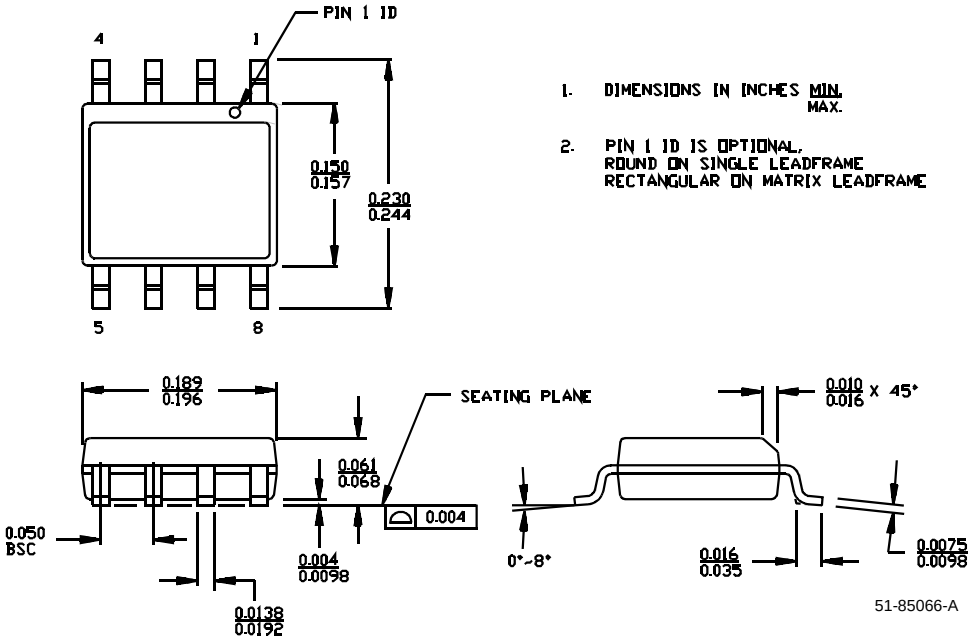
IMI
FS791BS(792BS or 794BS)
Date Code, Lot#

FS791 B S

- Package: S = SOIC
- Revision
- IMI Device Number

Package Drawing and Dimensions

8-Lead (150-Mil) SOIC S8



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Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114377	04/24/02	OXC	Convert from IMI to Cypress Convert from Word to Frame Maker Change Package Suffix
*A	122700	12/28/02	RBI	Added power up requirements to maximum ratings information.