



January 2010

FSA2270T Low-Voltage, Dual-SPDT (0.4 Ω) Analog Switch with Negative Swing Audio Capability

Features

- 0.4Ω Typical On Resistance (R_{ON}) for +3.0V Supply
- 0.25Ω Maximum R_{ON} Flatness for +3.0V Supply
- -3db Bandwidth: > 50MHz
- Low-I_{CCT} Current Over Expanded Control Input Range
- Packaged in 10-Lead UMLP
- Power-Off Protection on Common Ports
- Broad V_{CC} Operating Range: 1.65 to 4.3V
- Noise Immunity Termination Resistors
- Low Electrostatic Discharge (ESD)
 - Human Body Model (JEDEC: JESD22-A114)
 - Power to GND
 I/O to GND
 All other pins
 8kV
 - Charged Device Model (JEDEC: JESD22-A101)

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2270T is a high-performance, dual Single-Pole Double-Throw (SPDT) analog switch with negative swing audio capability. The FSA2270T features ultra-low R_{ON} of 0.4Ω (typical) at 3.0V V $_{\text{CC}}$. The FSA2270T operates over a wide V $_{\text{CC}}$ range of 1.65V to 4.3V, is fabricated with submicron CMOS technology to achieve fast switching speeds, and is designed for break-before-make operation. The select input is TTL-level compatible.

The FSA2270T features very low quiescent current even when the control voltage is lower than the $V_{\rm CC}$ supply. This feature suits mobile handset applications by allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

The FSA2270T includes termination resistors that improve noise immunity during overshoot excursions, off-isolation coupling, or "pop-minimization."

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	© Eco Status	Package Description
FSA2270TUMX	НК	Green	10-Lead, Quad Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm, 0.4mm pitch

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Analog Symbol

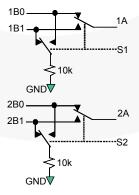


Figure 1. FSA2270T

Pin Configuration

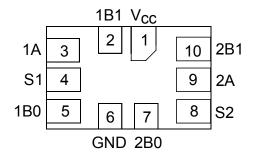


Figure 2. 10-Pin UMLP (Top Through View)

Pin Descriptions

Pin#	Name	Description			
1	V _{CC}	Supply Voltage			
3, 9	1A, 2A	Data Points			
4, 8	S1, S2	Switch Select Pins			
5, 7	1B0, 2B0	Data Ports			
6	GND	Ground			
2, 10	1B1, 2B1	Data Ports			

Truth Table

Control Input, Sn	Function
LOW Logic Level	nB0 connected to nA; nB1 terminated to GND
HIGH Logic Level	nB1 connected to nA; nB0 terminated to GND

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. Absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V _{CC}	Supply Voltage		-0.5	5.5	V
V _{SW}	Switch I/O Voltage ⁽¹⁾	1B0, 1B1, 2B0, 2B1, 1A, 2A Pins	V _{CC} - 4.3V	V _{CC} + 0.3V	V
V_{CNTRL}	Control Input Voltage ⁽¹⁾	S1, S2	-0.5V	V _{CC} + 0.3V	
I _{IK}	Input Clamp Diode Curren	t		-50mA	mA
I _{SW}	Switch I/O Current (Contin	uous)		350mA	mA
I _{SWPEAK}	Peak Switch Current (Puls	ed at 1ms Duration, <10% Duty Cycle)		500mA	mA
T _{STG}	Storage Temperature Ran	ge	-65	+150	°C
TJ	Maximum Junction Tempe	rature		+150	°C
T _L	Lead Temperature Solderi	ng, 10 seconds		+260	°C
		Power to GND		16	kV
	Human Body Model, JEDEC: JESD22-A114	I/O to GND		11	kV
ESD	02020. 020022-A114	All Other Pins		8	kV
	Charged Device Model, JE	DEC: JESD22-C101		2	kV

Note:

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
Vcc	Supply Voltage	1.65	4.30	V
V _{S1, S2}	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	V _{CC} -4.3V	V_{CC}	V
T _A	Operating Temperature	-40	+85	°C

^{1.} Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

DC Electrical Characteristics

All typical values are for V_{CC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =+25°C			T _A =-40 to +85°C		Units	
-				Min.	Тур.	Max.	Min.	Max.		
			3.60 to 4.30				1.7			
.,	Innut Valtage I ligh		2.70 to 3.60				1.5			
V_{IH}	Input Voltage High		2.30 to 2.70				1.4		V	
			1.65 to 1.95				0.9			
			3.60 to 4.30					0.7	V	
V_{IL}	Input Voltago Low		2.70 to 3.60					0.5		
V IL	Input Voltage Low		2.30 to 2.70					0.4	V	
			1.65 to 1.95					0.4		
I _{IN}	Control Input Leakage (S1,S2)	V _{IN} =0 to V _{CC}	1.65 to 4.30				-0.5	0.5	μA	
I _{A(ON)}	On Leakage Current of Port nA	nA=0.5V, V_{CC} =0.5V nB0 or nB1= V_{CC} =0.5V, 0.5V, or Floating Figure 5	1.95 to 4.30				-1	1	μΑ	
I _{OFF}	Power-Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A), V _{IN} =0V to 4.3V, V _{CC} =0V nB0, nB1=0V or Floating	0				-45	45	μΑ	
	Switch On	I _{ON} =100mA, nB0 or nB1=0.7V, 3.6V, 4.3V Figure 3	4.30		0.30					
D		I _{ON} =100mA, nB0 or nB1=0.7V, 3.6V, 4.3V Figure 3	3.00		0.40			0.80	Ω	
R _{ON}	Resistance ^(2,5)	I _{ON} =100mA, nB0 or nB1=0V, 0.7V, 1.6V, 2.3V Figure 3	2.30		0.52				Ω	
		I _{ON} =100mA, nB0 or nB1=0V, 0.7V, 1.65V Figure 3	1.65		1.00					
			4.30		0.04			0.13		
ΔR_{ON}	On Resistance Matching	I _{ON} =100mA, nB0 or	3.00		0.06			0.13	Ω	
ΔIXON	Between Channels ⁽³⁾	nB1=0.7V	2.30		0.12				32	
			1.65		1.00					
			4.30					0.25		
R _{FLAT(ON)} On F	On Resistance	I _{OUT} =100mA, nB0 or	3.00					0.25	Ω	
	Flatness ⁽⁴⁾	nB1=0V to V _{CC}	2.30		0.5				32	
			1.65		0.6					
R _{TERM}	Internal Termination Resistors ⁽⁵⁾				10				kΩ	
I _{cc}	Quiescent Supply Current	V_{IN} =0 or V_{CC} , I_{OUT} =0	4.30	-100		100	-500	500	nA	
	In any and the I	Input at 2.6V	4.00		3.0			10.0		
I _{CCT}	Increase in I _{CC} per Input	Input at 1.8V	4.30		7.0			15.0	μA	

Notes:

- On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
- Δ R_{ON}=R_{ONmax} R_{ONmin} measured at identical V_{CC}, temperature, and voltage. Flatness is defined as the difference between the maximum and minimum value of on resistance (R_{ON}) over the specified range of conditions.
- 5. Guaranteed by characterization, not production tested.

AC Electrical Characteristics

All typical value are for V_{CC} =3.3V at 25°C unless otherwise specified.

Cumple of	Parameter	Conditions	V 00	-	T _A =+250	С	T _A =-40	to +85°C	l luita	Fi
Symbol P	Parameter		V _{CC} (V)	Min.	Тур.	Max.	Min.	Max.	Units	Figure
			3.60 to 4.30			60	15	65		
+	Turn-On Time	nB0 or nB1=1.5V,	2.70 to 3.60			65	15	70	ns	Figure 6
t _{ON}	Tulli-Oli Tillie	$R_L=50\Omega$, $C_L=35pF$	2.30 to 2.70			80	15	85	115	Figure 7
			1.65 to 1.95		100					
			3.60 to 4.30			55	5	60		
toff	Turn-Off Time	nB0 or nB1=1.5V,	2.70 to 3.60			60	5	65	ne	Figure 6 Figure 7
LOFF	Tuni-On Time	$R_L=50\Omega$, $C_L=35pF$	2.30 to 2.70			65	5	70	ns	
			1.65 to 1.95		65					
			3.60 to 4.30		3		1		ns	Figure 8
t _{BBM}	Break-Before-	nB0 or nB1=1.5V, R_L =50 Ω , C_L =35pF	2.70 to 3.60		5		2			
чввм	Make Time		2.30 to 2.70		10		2			
			1.65 to 1.95		15		2			
Q	Charge Injection	C_L =1.0nF, V_S =0V, R_S =0 Ω	1.65 to 4.30		25				рС	Figure 12
OIRR	Off Isolation	$\begin{array}{l} \text{f=100kHz, R}_{\text{L}}\text{=}50\Omega, \\ \text{C}_{\text{L}}\text{=}0\text{pF} \end{array}$	1.65 to 4.30		-70				dB	Figure 10
Xtalk	Crosstalk	$\begin{array}{l} \text{f=100kHz, R}_{\text{L}}\text{=}50\Omega, \\ \text{C}_{\text{L}}\text{=}0\text{pF} \end{array}$	1.65 to 4.30		-70				dB	Figure 11
BW	-3db Bandwidth	$R_L=50\Omega$, $C_L=0pF$	1.65 to 4.30		>50				MHz	Figure 9
THD	Total Harmonic Distortion	f=20Hz to 20kHz, R _L =32 Ω , V _{IN} =2V _{pp} V _{BIAS} =0V	1.65 to 4.30		.06				%	Figure 15

Capacitance

Symbol	Parameter	Conditions	V (\(\)	Т	_A =+25°C	Units	Figure		
Symbol	Farameter	Conditions	V _{CC} (V)	Min.	Тур.	Max.	Ullits	rigure	
C _{IN}	Control Pin Input Capacitance	f=1MHz	0		2.5		pF	Figure 13	
C_{OFF}	B Port Off Capacitance	f=1MHz	3.3		30		pF	Figure 13	
C _{ON}	A Port On Capacitance	f=1MHz	3.3		120		pF	Figure 14	

Test Diagrams

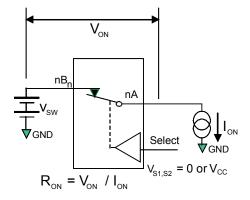
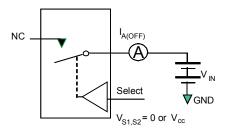


Figure 3. On Resistance



Each switch port is tested separately.

Figure 4. Off Leakage

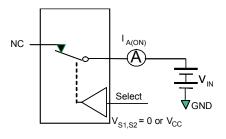


Figure 5. On Leakage

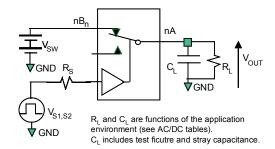


Figure 6. Test Circuit Load

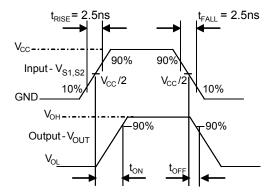


Figure 7. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)

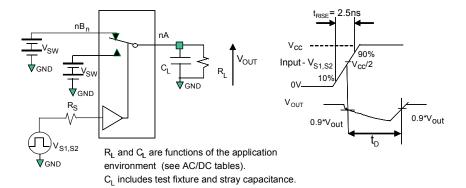


Figure 8. Break-Before-Make Interval Timing

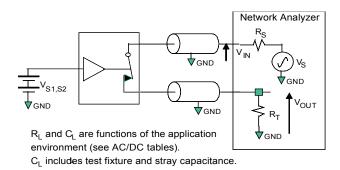


Figure 9. Bandwidth

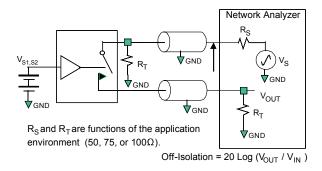


Figure 10. Channel Off Isolation

Test Diagrams (Continued)

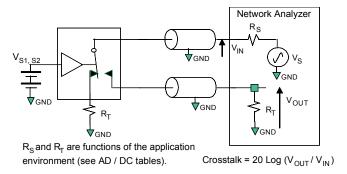


Figure 11. Adjacent Channel Crosstalk

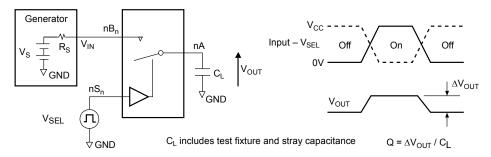


Figure 12. Charge Injection Test

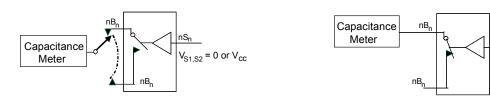


Figure 13. Channel Off Capacitance

Figure 14. Channel On Capacitance

V_{S1,S2}= 0 or V_{cc}

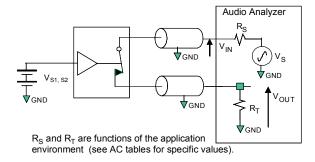
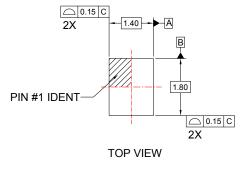
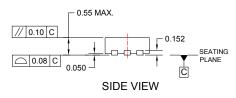
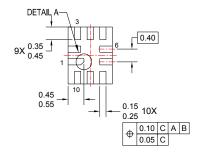


Figure 15. Total Harmonic Distortion

Physical Dimensions



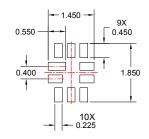




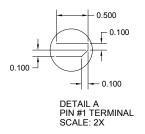
BOTTOM VIEW

0.663 9X 0.563 0.563 0.400 10X 0.400 10X 0.225

RECOMMENDED LAND PATTERN



OPTIONAL MINIMIAL TOE LAND PATTERN



NOTES:

- A. DIMENSIONS ARE IN MILLIMETERS.
- B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- C. DRAWING FILENAME: UMLP10Arev2

Figure 16. 10-Lead, Quad Ultrathin Molded Leadless Package (UMLP)

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