

May 2012

FSA3157B Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

Features

- Useful in Both Analog and Digital Applications
- Ultra-Small, MicroPak[™] Leadless Package
- Low On Resistance: <10Ω Typical at 3.3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Rail-to-Rail Signal Handling
- Power-Down, High-Impedance Control Input
- Over-Voltage Tolerance of Control Input to 7.0V
- Break-Before-Make Enable Circuitry
- 250MHz, 3dB Bandwidth

Description

The FSA3157B is a high-performance, Single-Pole / Double-Throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V $V_{\rm CC}$ operating range. The control input tolerates voltages up to 5.5V, independent of the $V_{\rm CC}$ operating range.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSA3157BL6X	-40 to +85°C	7G	6-Lead, MicroPak™ 1.0mm Wide Package	5000 Units on Tape and Reel
FSA3157BFHX	-40 to +85°C	7G	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape and Reel

Analog Symbols

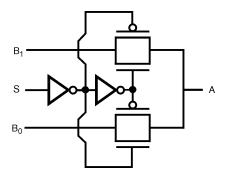


Figure 1. Logic Symbol

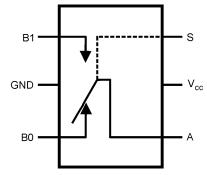


Figure 2. Analog Symbol

Pin Configuration

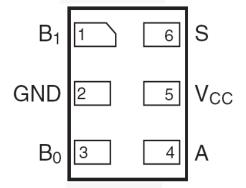


Figure 3. Pad Assignments

Function Table

Input (S)	Function
Logic Level LOW	B ₀ Connected to A
Logic Level HIGH	B₁ Connected to A

Pin Descriptions

Pin#	Name	Description
1	B ₁	Data Ports
2	GND	Ground
3	B ₀	Data Ports
4	A	Data Ports
5	V _{CC}	Power Supply
6	S	Control Input

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{cc}	Supply Voltage	-0.5	7.0	V
Vs	DC Switch Voltage ⁽¹⁾	-0.5	V _{CC} +0.5	V
V _{IN}	DC Input Voltage ⁽¹⁾	-0.5	7.0	V
I _{IK}	DC Input Diode Current at V _{IN} < 0V	-50		mA
I _{OUT}	DC Output Current		128	mA
I _{CC/IGND}	DC V _{CC} or Ground Current		±100	mA
T _{STG}	Storage Temperature Range	-65	+150	°C
TJ	Junction Temperature Under Bias		+150	°C
TL	Junction Lead Temperature (Soldering, 10 seconds)		+260	°C
P _D	Power Dissipation at +85°C		180	mW
ESD	Electrostatic Discharge Capability Human Body Mode JESD22-A114	el,	5	kV

Note:

1. Input and output negative voltage ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Par	Parameter			Unit	
V _{CC}	Supply Voltage Operating	1.65	5.50	V		
V _{IN}	Control Input Voltage ⁽²⁾	0	V _{CC}	V		
V _{IN}	Switch Input Voltage ⁽²⁾	0	V _{CC}	V		
V _{OUT}	Output Voltage ⁽²⁾	0	V _{CC}	V		
T _A	Operating Temperature		-40	+85	°C	
	A A Legat Disc and Fall Time	Control Input V _{CC} =2.3V-3.6V	0	10	20/1	
t_r , t_f	Input Rise and Fall Time	Control Input V _{CC} =4.5V-5.5V	0	5	ns/V	

Note:

2. Control input must be held HIGH or LOW; it must not float.

Electrical Characteristics

Cumbal	Doromotor	Conditions	V 00	1	Γ _A =+25°	С	T _A =-40 t	o +85°C	Units
Symbol	Parameter	Conditions	V _{cc} (V)	Min.	Тур.	Max.	Min.	Max.	
	High Level Input		1.65 to 1.95	0.75V _{CC}			0.75V _{CC}		
V _{IH} Voltage			2.30 to 5.50	0.7V _{CC}			0.7V _{CC}		V
\ /	Low Level Input		1.65 to 1.95			0.25V _{CC}		0.25V _{CC}	V
V_{IL}	Voltage		2.30 to 5.50			0.3V _{CC}		0.3V _{CC}	V
I _{IN}	Input Leakage Current	$0 \leq V_{IN} \leq 5.5V$	0 to 5.50		±0.05	±0.1		±1	μΑ
I _{OFF}	Off State Leakage Current	$0 \le A, B \le V_{CC}$	1.65 to 5.50		±0.05	±0.1		±1	μΑ
		V _{IN} =0V, I _O =30mA			3.0	7.0		7.0	
		$V_{IN}=2.4V, I_{O}=-30mA$	4.50		5.0	12.0		12.0	
		V _{IN} =4.5V, I _O =-30mA			7.0	15.0		15.0	
	0 11 0	V _{IN} =0V, I _O =24mA	3.00		4.0	9.0		9.0	
R _{ON} Switch On Resistance ⁽³⁾	$V_{IN}=3V$, $I_O=-24mA$	3.00		10.0	20.0		20.0	Ω	
	V _{IN} =0V, I _O =8mA	2.30		5.0	12.0		12.0		
	V _{IN} =2.3V,I _O =-8mA	2.30		13.0	30.0		30.0		
	V _{IN} =0V, I _O =4mA	1.65		6.5	20.0		20.0		
	V _{IN} =1.65V, I _O =-4mA			17.0	50.0		50.0		
I _{cc}	Quiescent Supply Current: All Channels On or Off	V _{IN} =V _{CC} or GND I _{OUT} =0	5.50			1		10	μA
	Analog Signal Range		V _{cc}	0		V _{cc}	0	V _{cc}	V
		$I_A = -30 mA, \\ 0 \le V_{Bn} \le V_{CC}$	4.50					25	
D	On Resistance	$ \begin{aligned} &I_A \!\!=\!\! -24mA, \\ &0 \leq V_{Bn} \leq V_{CC} \end{aligned} $	3.00					50	
R _{RANGE}	Over Signal Range ^(3,7)	$ \begin{aligned} &I_A \!\!=\!\! -8mA, \\ &0 \leq VBn \leq V_{CC} \end{aligned} $	2.30					100	Ω
		$I_A = -4mA, \\ 0 \le V_{Bn} \le V_{CC}$	1.65					300	
		I _A =-30mA, V _{Bn} =3.15	4.50		0.15				7
۸D	On Resistance Match Between	I _A =-24mA, V _{Bn} = 2.1	3.00		0.20	- 4			Ω
ΔKON	ΔR _{ON} Match Between Channels ^(3,4)	I _A =-8mA, V _{Bn} =1.6	2.30		0.50	- //			2.2
	70.	I _A =-4mA, V _{Bn} =1.15	1.65		0.50				
On Resistar		$ I_A = -30 mA, \\ 0 \le V_{Bn} \le V_{CC} $	5.00		6				
	On Resistance	$I_A = -24mA, \\ 0 \le V_{Bn} \le V_{CC}$	3.00		12				Ω
THLAI	Flatness ^(3,4,6)	$I_A = -8mA, \\ 0 \le V_{Bn} \le V_{CC}$	2.50		28				22
		$ \begin{aligned} I_A &= -4mA, \\ 0 &\leq V_{Bn} \leq V_{CC} \end{aligned} $	1.80		125				$\langle \cdot \rangle$

Notes:

- Measured by the voltage drop between the A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
- Parameter is characterized, but not tested in production.
- $\Delta R_{ON} = R_{ON}$ maximum R_{ON} minimum measured at identical V_{CC} , temperature, and voltage levels. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
- 7. Guaranteed by design.

AC Electrical Characteristics

Cumbal	Symbol Parameter		V 00	Т	_=+25°	С	T _A =-40 t	o +85°C	Units	Ciaura
Symbol	Parameter	Conditions	V _{cc} (V)	Min.	Тур.	Max.	Min.	Max.	Units	Figure
			1.65 to 1.95			3.5		3.5		
	Propagation Delay	V ODEN	2.30 to 2.70			1.2	1	1.2		Figure 10
t _{PLH} , t _{PLH}	Bus-to-Bus ⁽⁸⁾	V _{IN} =OPEN	3.00 to 3.60			0.8		0.8	ns	Figure 11
			4.05 to 5.50			0.3		0.3		
			1.65 to 1.95	7.0		23.0		24.0		
	Output Enable Time	$V_{IN}=2x V_{CC}$ for $t_{PZL} V_{IN}=0V$	2.30 to 2.70	3.5		13.0		14.0		Figure 10
t _{PZL} , t _{PZH}	Turn-On Time (A to B _n)	for t _{PZH}	3.00 to 3.60	2.5		6.9		7.6	ns	Figure 11
	.,,		4.50 to 5.50	1.7		5.2		5.7		
			1.65 to 1.95	3.0		12.5		13.0		
	Output Disable Time Turn-Off Time	$V_{IN}=2x V_{CC}$ for $t_{PLZ} V_{IN}=0V$	2.30 to 2.70	2.0		7.0		7.5	no	Figure 10
IPLZ, IPHZ	t _{PLZ} , t _{PHZ} Turn-Off Time (A Port to B Port)	for t _{PHZ1}	3.00 to 3.60	1.5		5.0		5.3	ns	Figure 11
	`		4.50 to 5.50	0.8		3.5		3.8	=	
			1.65 to 1.95	0.5			0.5			
t	Break-Before-Make		2.30 to 2.70	0.5			0.5		ns	Figure 12
t _{BBM}	Time ⁽⁹⁾		3.00 to 3.60	0.5		1	0.5		115	i iguie iz
			4.50 to 5.50	0.5			0.5			
Q	Charge Injection ⁽⁹⁾	$C_L=0.1nF,$ $V_{GEN}=0V$	5.00		7				рC	Figure 13
	,	$R_{GEN}=0\Omega$	3.30		3					
OIRR	Off Isolation ⁽¹⁰⁾	R _L =50Ω, f=10MHz	1.65 to 5.50		-57				dB	Figure 14
Xtalk	Crosstalk	R _L =50Ω, f=10MHz	1.65 to 5.50		-54					Figure 15
BW	-3dB Bandwidth	R _L =50Ω	1.65 to 5.50		250				dB	Figure 18
THD	Total Harmonic Distortion ⁽⁹⁾	R _L =600Ω, 0.5V _{PP} , f=600Hz to 20KHz	5.00		.011				%	

Notes

- 8. This parameter is guaranteed by design, but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance when driven by an ideal voltage source (zero output impedance).
- 9. Guaranteed by design.
- 10. Off Isolation = $20 \log_{10} [V_A / V_{Bn}]$.

Capacitance

 T_A = +25°C, f=1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typical	Units	Figure
C _{IN}	Control Pin Input Capacitance	V _{CC} =0V	2.3	pF	
C _{IO-B}	B Port Off Capacitance	V _{CC} =5.0V	6.5	pF	Figure 16
C _{IOA-ON}	A Port Capacitance, Switch Enabled	V _{CC} =5.0V	18.5	pF	Figure 17

Typical Performance Characteristics

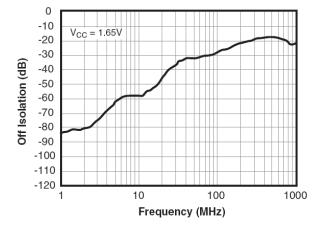


Figure 4. Off Isolation, V_{CC}-1.65V

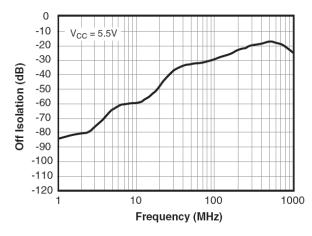


Figure 5. Off Isolation, V_{CC}-5.5V

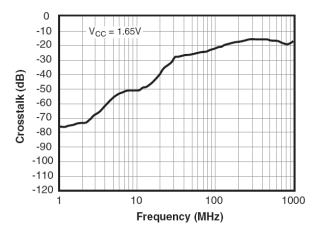


Figure 6. Crosstalk, V_{CC}=1.65V

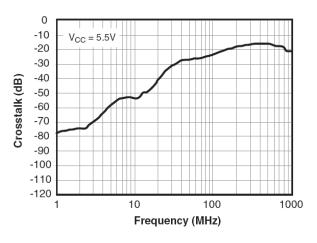


Figure 7. Crosstalk, V_{CC}=5.5V

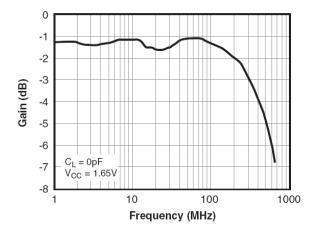


Figure 8. Bandwidth, V_{CC} =1.65V

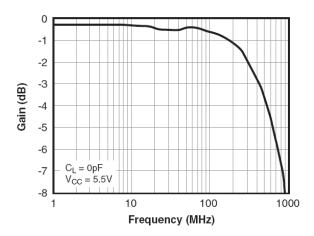
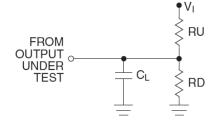


Figure 9. Bandwidth, V_{CC}=5.5V

AC Loading and Waveforms



Notes:

Input driven by 50Ω source terminated in 50Ω C_L includes load and stray capacitance Input PRR $\,=1.0$ MHz; $t_W=500$ ns

Figure 10. AC Test Circuit

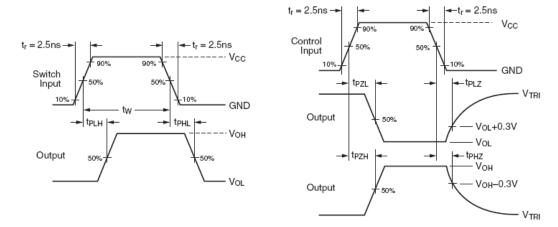


Figure 11. AC Waveforms

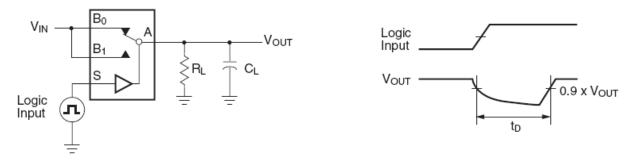
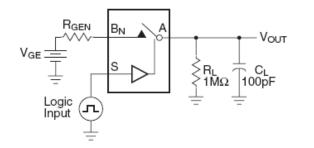


Figure 12. Break-Before-Make Interval Timing

AC Loading and Waveforms (Continued)



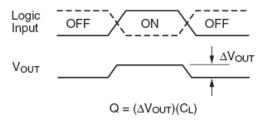
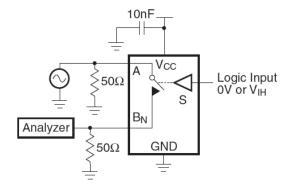


Figure 13. Charge Injection Test



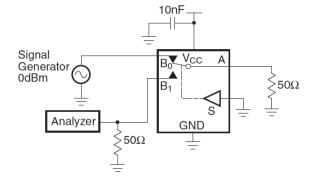
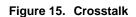
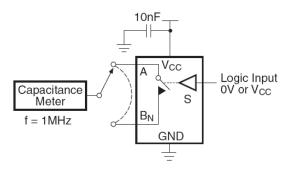


Figure 14. Off Isolation





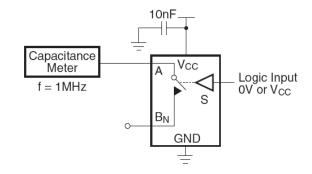


Figure 16. Channel Off Capacitance

Figure 17. Channel On Capacitance

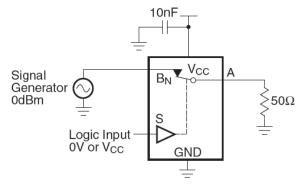
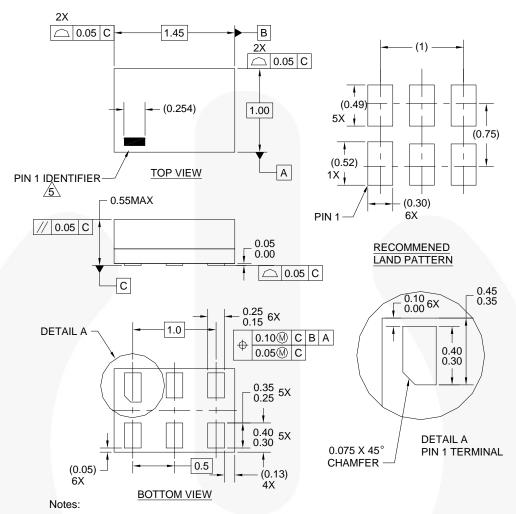


Figure 18. Bandwidth

Physical Dimensions



- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5 PIN ONE IDENTIFIER IS 2X LENGTH OF ANY

OTHER LINE IN THE MARK CODE LAYOUT.

Figure 19. 6-Lead, MicroPak™ 1.0mm Wide Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	ckage Designator Tape Section		Cavity Status	Cover Type Status	
	Leader (Start End)	125 (Typical)	Empty	Sealed	
L6X	Carrier	5000	Filled	Sealed	
	Trailer (Hub End)	75 (Typical)	Empty	Sealed	

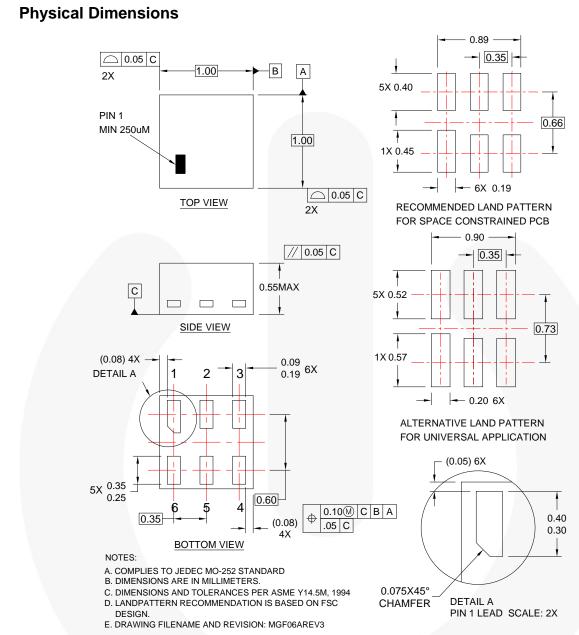


Figure 20. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/MicroPAK2 6L tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
FHX	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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