Features

- On Resistance: 5Ω Typical, V_{DDC}=2.7V
- f_{toggle}: >75MHz

SEMICONDUCTOR

- Low On Capacitance: 6pF Typical
- Low Power Consumption: 2µA Maximum
- Supports Secure Digital (SD), Secure Digital I/O (SDIO), and Multimedia Card (MMC) Specifications
- Supports 1-Bit / 4-Bit Host Controllers (V_{DDH1/H2}=1.65V to 3.6V) Communicating with High-Voltage (2.7-3.6V) and Dual-Voltage Cards (1.65-1.95V, 2.7-3.6V)
 - V_{DDC}=1.65 to 3.6V, V_{DDH1/H2}=1.65 to 3.6V
- 24-Lead MLP and UMLP Packages

Applications

- Cell Phone, PDA, Digital Camera, Portable GPS, and Notebook Computer
- LCD Monitor, TV, and Set-Top Box

Related Resources

- FSSD07 Evaluation Board
- Evaluation Board Users Guide
- For samples, questions, or board requests; please contact <u>analogswitch@fairchildsemi.com</u>

Description

The FSSD07 is a 2:1 multiplexer that allows dual Secure Digital (SD), Secure Digital I/O (SDIO), and Multimedia Card (MMC) host controllers to share a common peripheral. The host controllers can be equal to, greater than, or less than peripheral card supply with minimal power consumption. This configuration enables dual host CMD, CLK, and D[3:0] signals to be multiplexed to a common peripheral.

The architecture includes the necessary bi-directional data and command transfer capability for single high-voltage cards or dual-voltage supply cards. The clock path is a uni-directional buffer.

Typical applications involve switching in portables and consumer applications: cell phones, digital cameras, home theater monitors, set-top boxes, and notebooks.



Figure 1. Analog Symbol Diagram

Ordering Information								
Part Number	Top Mark	Operating Temperature Range	Package Description	Packing Method				
FSSD07BQX	FSSD07	-40°C to +85°C	24-Lead Molded Leadless Package (MLP), JEDEC MO-220, 3.5 x 4.5mm	Tape & Reel				
FSSD07UMX	JK	JK -40°C to +85°C 24-Lead Ultra-thin Molded Leadless Package (UMLP), 0.4mm pitch		Tape & Reel				



Truth Table

OE	S	Function
HIGH	LOW	1CMD, 1CLK, 1DAT[3:0] connected to CMD, CLK, DAT[3:0]
HIGH	HIGH	2CMD, 2CLK,2DAT[3:0] connected to CMD, CLK, DAT[3:0]
LOW	Х	CMD, DAT[3:0] ports high impedance; CLK is function of selected nCLK



Functional Description

The FSSD07 enables the multiplexing of dual ASIC / baseband processor hosts to a common peripheral card or module, providing bi-directional support of the dualvoltage SD/SDIO or MMC cards available in the marketplace. Each host SDIO port has its own supply rail, such that hosts with different supplies can be interfaced to a common peripheral module or card. The peripheral card supply must be equal to or greater than the host(s) to minimize power consumption. The independent V_{DDC} , V_{DDH1} , and V_{DDH2} are defined by the supplies connected from the application Power Management ICs (PMICs) to the FSSD07. The clock path is a uni-directional buffered path rather than a bidirectional switch port. The supplies (V_{DDC}, V_{DDH1}, and V_{DDH2}) have an internal termination resistor (typically $3M\Omega$) to ensure the supply rails internally do not float if the application turns off one or all of these sources.

CMD, DAT Bus Pull-ups

The CMD and DAT[3:0] ports do not have, internally, the system pull-up resistors as defined in the MMC or SD card system bus specifications. The system bus pull-up must be added external to the FSSD07. The value, within the specific specification limits, is a function of the individual application and type of card or peripheral connected. For SD card applications, the R_{CMD} and R_{DAT} pull-ups should be between 10k Ω and 100k Ω . For MMC applications, the R_{CMD} pull-ups should be between 4.7k Ω and 100k Ω , and the R_{DAT} pull-ups between 50k Ω and 100k Ω . The card-side CMD and DAT[3:0] outputs have a circuit that facilitates incident wave switching, so the external pull-up resistors ensure retention of the output high level.

The OE pin can be used to place the CMD and DAT[3:0] into high-impedance mode during power-up sequencing or when the system enters IDLE state (*see IDLE State CMD/DAT Bus "Parking"*).

CLK Bus

The 1CLK and 2CLK inputs are bi-state buffer architectures, rather than a switch I/O, to ensure 52MHz incident wave switching. Since most host controllers also have a clock enable register bit to enable or disable the system clock when in IDLE mode, the CLK output is not disabled by the OE pin. Instead, the CLK output is a function of whichever host controller clock is selected by the S pin.

Consequently, there is always a clock path connected between the selected host and the card. The state of the CLK pin is a function of the selected host controller nCLK output pin, which facilitates retaining clock duty cycle in the system or performing read / wait operations.

IDLE State & Power-Up CMD/DAT Bus "Parking"

The SD and MMC card specifications were written for a direct point-to-point communication between host controller and card. The introduction of the FSSD07 in that path, as an expander, requires that the functional operation and system latency not be impacted by the switch characteristics. Since there are various card formats, protocols, and configurable controllers, an OE pin is available to facilitate a fast IDLE transition for the CMD/DAT[3:0] outputs. Some controllers, rather than placing CMD/DAT into high-impedance mode, pull the outputs HIGH for a clock cycle prior to going into high-impedance mode (referred to as "parking" the output). Some legacy controllers pull their outputs HIGH versus high impedance.

If the OE pin is pulled HIGH and the controller places its command and data outputs into high-impedance (driving nCMD/nDAT[3:0]), the FSSD07 CMD/DAT[3:0] output rise time is a function of the RC time constant through the switch path. Pulling OE LOW puts the switches into high impedance, disabling communication from the host to card, and the CMD/DAT[3:0] outputs are pulled HIGH by the system pull-up resistors chosen for the application. This mechanism facilitates power-up sequencing by holding OE LOW until supplies are stable and communication between the host(s) and card is enabled.

Power Optimization

Since the FSSD07 has multiple supplies (V_{DDC} , V_{DDH1} , and V_{DDH2}), the control signals have been referenced to the card peripheral side (V_{DDC}). To minimize power consumption, current paths between supplies are isolated when one or more supplies are not present. This includes the configuration of the removal of V_{DDC} with host controller supplies remaining present.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{DDC}	Card Supply Voltage		-0.5	4.6	V
V _{DDH1} ,V _{DDH2}	Host Controller Supply Voltage		-0.5	4.6	V
V _{sw}	Switch I/O Voltage ⁽¹⁾	1DAT[3:0], 2DAT[3:0], 1CMD, 2CMD Pins	-0.5	V _{DDx} ⁽²⁾ + 0.3V (4.6V maximum)	V
V _{SW}	Switch i/O Voltage	DAT[3:0], CMD Pins	-0.5	V _{DDx} ⁽²⁾ + 0.3V (4.6V maximum)	V
V _{CNTRL}	Control Input Voltage ⁽¹⁾	S, OE	-0.5	4.6	V
V _{CLKI}	CLK Input Voltage (1)	1CLK, 2CLK	-0.5	4.6	V
V _{CLKO}	CLK Output Voltage ⁽¹⁾	CLK	-0.5	V _{DDx} ⁽²⁾ + 0.3V (4.6V maximum)	V
I _{INDC}	Input Clamp Diode Current			-50	mA
I _{sw}	Switch I/O Current	SDIO Continuous		50	mA
I _{SWPEAK}	Peak Switch Current	SDIO Pulsed at 1ms Duration, <10% Duty Cycle		100	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
TJ	Maximum Junction Temperature			+150	°C
TL	Lead Temperature	Soldering, 10 Seconds		+260	°C
		I/O to GND		8	
505	Human Body Model, JEDEC: JESD22-A114	Supply to GND		10	kV
ESD		All Other Pins		5	
	Charged Device Model, JEDEC-JES	D-C101		2	

Notes:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

2. V_{DDx} references the specific SDIO port V_{DD} rail (i.e. V_{DDH1}, V_{DDH2}, V_{DDC}).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Param	Min.	Max.	Unit	
V _{DDC}	Supply Voltage - Card Side		1.65	3.60	V
$V_{DDH1,}V_{DDH2}$	Supply Voltage - Dual Host Cont	roller	1.65	3.60	V
V _{CNTRL}	Control Input Voltage - V _S , V _{OE}	0	V _{DDC}	V	
V _{CLKI}	Clock Input Voltage - V _{CLKI}	0	V _{DDH1/H2}	V	
		CMD, DAT[3:0]	0	V _{DDC}	V
V_{SW}	Switch I/O Voltage	1CMD, 1DAT[3:0]	0	V _{DDH1}	V
		2CMD, 2DAT[3:0]	0	V _{DDH2}	V
T _A	Operating Temperature	-40	+85	°C	
θ_{JA}	Thermal Resistance, Free Air	MLP Package		+50	°C/W

DC Electrical Characteristics at 1.8V V_{DDC}

All typical values are for V_{DDC} =1.8V at 25°C unless otherwise specified.

Cumb al	Devementer		V _{DDH1} /	Conditions	T _A =-40 to +85°C			11
Symbol	Parameter	(V)	V _{DDH2} (V)	Conditions	Min.	Тур.	Max.	Unit
Common Pi	ns							
V _{IK}	Clamp Diode Voltage	1.80	1.80	I _{IK} =-18mA			-1.2	V
V _{IH}	Control Input Voltage High	1.80	1.80		1.3			V
V _{IL}	Control Input Voltage Low	1.80	1.80				0.5	V
I _{IN}	S, OE Input High Current	1.95	1.95	V _{CNTRL} =0V to V _{DDC}	-1		1	μA
I _{OZ}	Off Leakage, Current of all ports	1.95	1.95	V _{SW} =0V to V _{DDC}	-1.0	0.5	1.0	μA
V _{OHC}	CLK Output Voltage High ⁽³⁾	1.95	1.95	I _{OH} =-2mA	1.6			V
V _{OLC}	CLK Output Voltage Low ⁽³⁾	1.65	1.65	I _{OL} =-2mA			90	mV
R _{ON}	Switch On Resistance ⁽⁴⁾	1.65	1.65	$V_{CMD, DAT[3:0]}=0V,$ $I_{ON}=-2mA$ Figure 5			10	Ω
ΔR_{ON}	Delta On Resistance ^(3, 5)	1.65	1.65	V _{CMD, DAT[3:0]} =0V, I _{ON} =- 2mA		0.85		Ω
Power Supp	ly							
I _{CC(VDDC)}	Quiescent Supply Current (Card)	1.95	0	V _{sw} =0 or V _{DDC} , I _{OUT} =0			2	μA
I _{CC(VDDH1/H2)}	Quiescent Supply Current (Hosts)	1.95	1.95	$ \begin{array}{c} V_{SW} = 0 \text{ or } V_{DDx,} I_{OUT} = 0, \\ V_{CLKI} = V_{DDHx,} \\ V_{CLKO} = Open, OE = V_{DDC} \end{array} $			2	μA
ΔI_{HOST}	Delta I _{CC(VDDH1, VDDH2)} for One Host Powered Off	1.95	1.95 / 0 0 / 1.95				2	μA

Notes:

3. Guaranteed by characterization, not production tested.

4. On resistance is determined by the voltage drop between the switch I/O pins at the indicated current through the switch.

5. $\Delta R_{ON} = R_{ON max} - R_{ON min}$ measured at identical V_{CC}, temperature, and voltage.

DC Electrical Characteristics at 2.7V V_{DDC}

All typical values are for V_{DDC} =2.7V at 25°C unless otherwise specified.

Queen la c	Desemptor	V 00	V _{DDH1} /	Conditions	T _A =-	Unit		
Symbol	Parameter	V _{DDC} (V)	V _{DDH2} (V)	Conditions	Min.	Тур.	Max.	Unit
Common	Pins				•			
V _{IK}	Clamp Diode Voltage	2.7	2.7	I _{IK} =-18mA			-1.2	
V _{IH}	Control Input Voltage High	2.7	2.7		1.8			V
V _{IL}	Control Input Voltage Low	2.7	2.7				0.8	
I _{IN}	S, OE Input High Current	3.6	3.6	V _{CNTRL} =0V to V _{DDC}	-1		1	μA
I _{oz}	Off Leakage Current of all Ports	3.6	3.6	V_{SW} =0V to V_{DDC}	-1.0	0.5	1.0	μA
V _{OHC}	CLK Output Voltage High ⁽⁶⁾	2.7	2.7	I _{OH} =-2mA	2.4			V
V _{OLC}	CLK Output Voltage Low ⁽⁶⁾	3.6	3.6	I _{OL} =-2mA			90	mV
R _{on}	Switch On Resistance ⁽⁷⁾	2.7	2.7	V _{CMD, DAT[3:0]} =0V, I _{ON} =-2mA Figure 5		5.0	8.0	Ω
ΔR_{ON}	Delta On Resistance ^(6, 8)	2.7	2.7	V _{CMD, DAT[3:0]} =0V, I _{ON} =- 2mA		0.8		Ω
Power Su	ipply							
I _{CC(VDDC)}	Quiescent Supply Current (Card)	3.6	0	V _{sw} =0 or V _{DDC} , I _{OUT} =0			2	μA
I _{CC} (VDDH1/C2)	Quiescent Supply Current (Hosts)	3.6	3.6	V_{SW} =0 or V_{DDx} , I_{OUT} =0, V_{CLKi} = V_{DDHX} , V_{CLKO} =Open, OE = V_{DDC}			2	μA
ΔI_{HOST}	Delta I _{CC(VDDH1, VDDH2)} for One Card Powered Off	3.6	3.6 / 0 0 / 3.6	V_{SW} =0 or $V_{DDx,}$ I_{OUT} =0, V_{CLKI} = V_{DDHx} , V_{CLKO} =Open, OE= V_{DDC}			2	μA

Notes:

6. Guaranteed by characterization, not production tested.

7. On resistance is determined by the voltage drop between the switch I/O pins at the indicated current through the switch.

8. $\Delta R_{ON} = R_{ON max} - R_{ON min}$ measured at identical V_{CC}, temperature, and voltage.

AC Electrical Characteristics at 1.8V V_{DDC}

All typical values are for V_{DDC} =1.8V at 25°C unless otherwise specified.

• • • •	Parata		V _{DDH1} /		T _A =-40 to +85°C			11
Symbol	Parameter	V _{DDC} (V)	V _{DDH2} (V)	Conditions	Min.	Тур.	Max.	Unit
t _{on}	Turn-On Time, S, OE to CMD, DAT[3:0]	1.65 to 1.95	1.65 to 3.6	V _{SW} =0V, R _L =1kΩ, C _L =20pF Figure 7, Figure 8		8	18	ns
t _{OFF}	Turn-Off Time, S, OE to CMD, DAT[3:0]	1.65 to 1.95	1.65 to 3.6	V _{SW} =0V, R _L =1kΩ, C _L =20pF Figure 7, Figure 8		6	13	ns
t _{RISE1/} FALL1	CMD/DAT Output Edge Rates ⁽⁹⁾	1.65 to 1.95	1.65 to 3.6	R _L =1kΩ, C _L =20pF (10-90%) Figure 7, Figure 8		3		ns
t _{PD}	Switch Propagation Delay ⁽⁹⁾	1.65 to 1.95	1.65 to 3.6	$R_L=1k\Omega$, $C_L=20pF$ Figure 7, Figure 89		4.5	9	ns
t _{pLH}	LH Propagation Delay 1CLK, 2CLK to CLK	1.65 to 1.95	1.65 to 3.6	C _L =20pF Figure 10, Figure 11		4	6	ns
t _{pHL}	HL Propagation Delay 1CLK, 2CLK to CLK	1.65 to 1.95	1.65 to 3.6	C _L =20pF Figure 10, Figure 11		4	6	ns
t _{RISE2/} FALL2	CLK Output Edge Rates ⁽⁹⁾	1.65 to 1.95	1.65 to 3.6	C _L =20pF (10-90%) Figure 7, Figure 8		3		ns
O _{IRR}	Off Isolation ⁽⁹⁾	1.8	1.65 to 3.6	f=10MHz, R _T =50Ω, C _L =20pF, Figure 12		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk ⁽⁹⁾	1.8	1.65 to 3.6	f=10MHz, R _T =50Ω, C _L =20pF, Figure 13		-60		dB
f _{toggle}	Clock Frequency ⁽⁹⁾	1.8	1.65 to 3.6	C _L =20pF		75		MHz

Note:

9. Guaranteed by characterization, not production tested.

AC Electrical Characteristics at 3.3V V_{DDC}

All typical values are for V_{DDC} =3.3V at 25°C unless otherwise specified.

Sumhel	Parameter		V _{DDH1} / V _{DDH2}	Conditions	T _A =-40 to +85°C			11
Symbol	Parameter	V _{DDC} (V)	(V)	Conditions	Min.	Тур.	Max.	Unit
t _{on}	Turn-On Time, S, OE to CMD, DAT[3:0]	2.7 to 3.6	1.65 to 3.6	V _{sw} =0V, R _L =1kΩ, C _L =20pF Figure 7, Figure 8		8	18	ns
t _{OFF}	Turn-Off Time, S, OE to CMD, DAT[3:0]	2.7 to 3.6	1.65 to 3.6	V_{SW} =0V, R _L =1k Ω , C _L =20pF Figure 7, Figure 8		6	13	ns
t _{RISE1/} FALL1	CMD/DAT Output Edge Rates ⁽¹⁰⁾	2.7 to 3.6	1.65 to 3.6	R _L =1kΩ, C _L =20pF (10- 90%) Figure 7, Figure 8		3		ns
t _{PD}	Switch Propagation Delay ⁽¹⁰⁾	2.7 to 3.6	1.65 to 3.6	$R_L=1k\Omega$, $C_L=20pF$ Figure 7, Figure 8		2.5	6	ns
t _{pLH}	LH Propagation Delay 1CLK, 2CLK to CLK	2.7 to 3.6	1.65 to 3.6	C _L =20pF Figure 10, Figure 11		4	6	ns
t _{pHL}	HL Propagation Delay 1CLK, 2CLK to CLK	2.7 to 3.6	1.65 to 3.6	C _L =20pF Figure 10, Figure 11		4	6	ns
t _{RISE2/} FALL2	CLK Output Edge Rates ⁽¹⁰⁾	2.7 to 3.6	1.65 to 3.6	C _L =20pF (10-90%) Figure 7, Figure 8		3		ns
O _{IRR}	Off Isolation ⁽¹⁰⁾	2.7	1.65 to 3.6	f=10MHz, R _T =50Ω, C _L =20pF Figure 12		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk ⁽¹⁰⁾	2.7	1.65 to 3.6	f=10MHz, R _T =50Ω, C _L =20pF, Figure 13		-60		dB
f _{toggle}	Clock Frequency ⁽¹⁰⁾	2.7	1.65 to 3.6	C _L =20pF		75		MHz

Note:

10. Guaranteed by characterization, not production tested.

Capacitance

Symbol	Deremeter	V _{DDC}	V _{DDH1/H2}	Conditions	T _A =-4	Unit		
Symbol	Parameter	(V)	(V)	Conditions	Min.	Тур.	Max.	Unit
C _{IN(S, OE,} CLK)	Control and nCLK Pin Input Capacitance ⁽¹¹⁾	0	2.7	V _{DDC} =0V		2.5		pF
C _{ON}	Common Port On Capacitance ⁽¹¹⁾ (C _{DAT[3:0], CMD})	2.7	2.7	V _{OE} =V _{DDC} , V _{bias} =0.5V, f=1MHz Figure 14		7.5		pF
C _{OFF}	Input Source Off Capacitance ⁽¹¹⁾	2.7	2.7	V _{OE} =0V, V _{bias} =0.5V, f=1MHz Figure 15		4		pF

Note:

11. Guaranteed by characterization, not production tested.





Each switch port tested separately.

Figure 6. Off Leakage



Figure 8. Turn On/Off Time Waveforms



environment (see AC Tables for specific values)

C_L includes test fixture and stray capacitance Figure 10. AC Test Circuit Load (CLK)

/_{ddx}/2

50%

tpLH

Figure 9. Switch Propagation Delay (t_{PD}) Waveform

10%

V_{OH}

VOL

Output- V_{OUT}

GND.

V_{ddx}/2

ζрΗ

10%

50%







FSSD07 —

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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