FAIRCHILD SEMICONDUCTOR®

May 2011

FXLP4555
1.8V / 3.0V SIM Card Power Supply and Level Shifter

Features

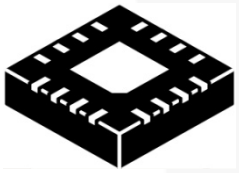
- Supports 1.8V or 3.0V SIM Cards
- LDO Supplies >50mA Under 1.8V and 3.0V
- Built-in Pull-up Resistor for I/O Pin in Both Directions
- ESD Protection: 8kV (Human Body Model, According to ISO-7816 Specifications)
- Supports Clock ≥ 5MHz
- Supports “Clock Stop” Power Management per ISO7816-3 Specifications
- Low-Profile 3x3mm MLP-16 Package

Applications

- SIM Card Interface Circuit for 2G, 2.5G, and 3G Mobile Phones
- Identification Module
- Smart Card Readers
- Wireless PC Cards

Description

The FXLP4555 is a level-shifter analog circuit designed to translate the voltages between a SIM card and an external baseband. A built-in LDO-type DC-DC converter allows the FXLP4555 to drive 1.8V and 3.0V SIM cards. The device fulfills the ISO7816-3 smart-card interface standard as well as GSM 11.11 (11.12 and 11.18) and 3G mobile requirements (IMT-2000/3G UICC standard). The EN pin enables a low-current Shutdown Mode that extends battery life. The card power supply voltage (VCC_C) is selected using a single pin (VSEL).



Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FXLP4555MPX	-40 to +85°C	FXLP 4555	16-Lead,MLP,Quad,JEDEC MO-220,3MM Square	3000 Units on Tape & Reel

Application Diagram

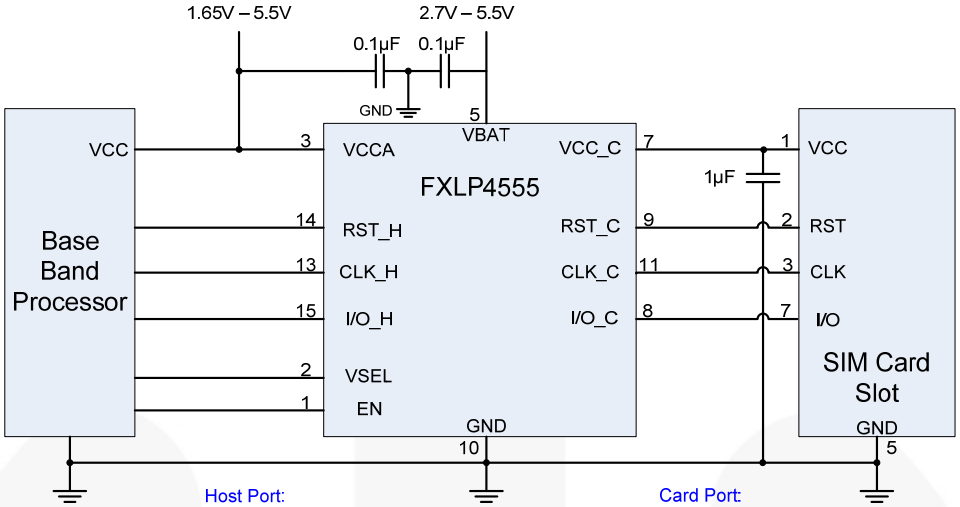


Figure 1. Typical Application

Functional Block Diagram

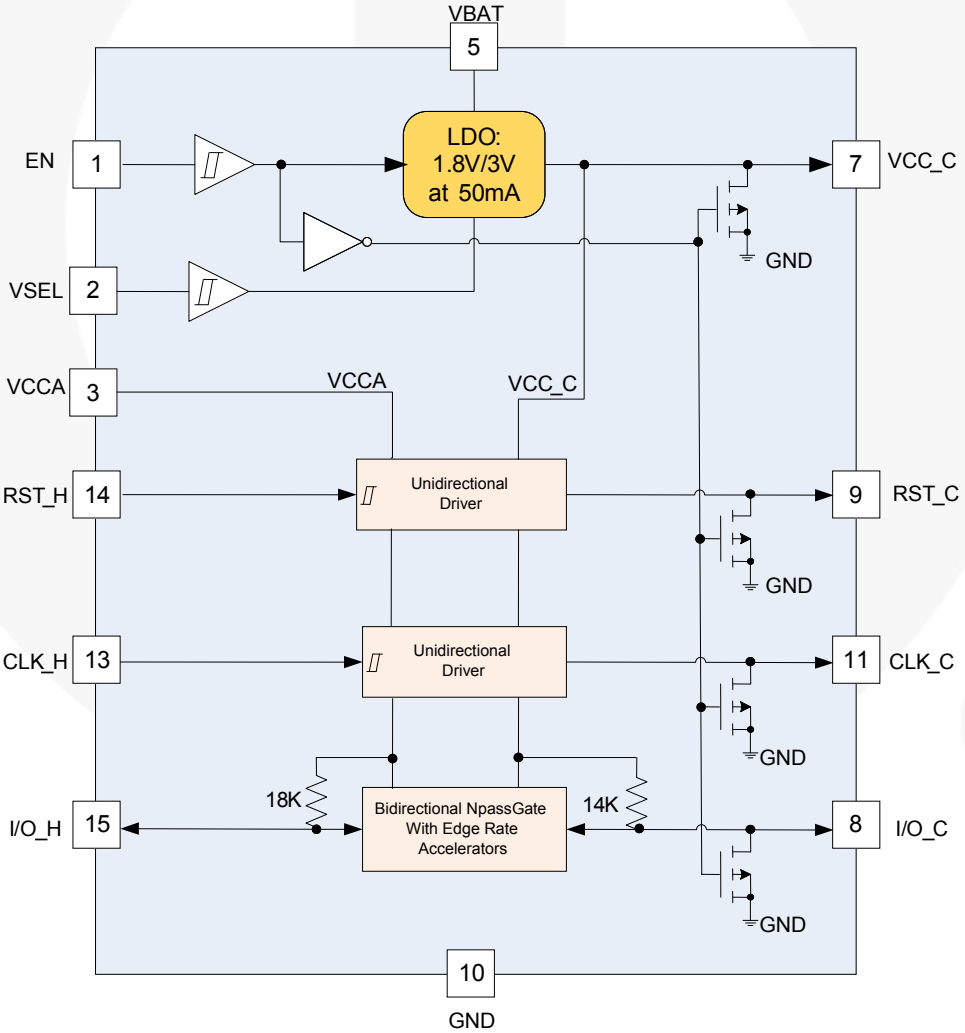


Figure 2. Block Diagram

Pin Configuration

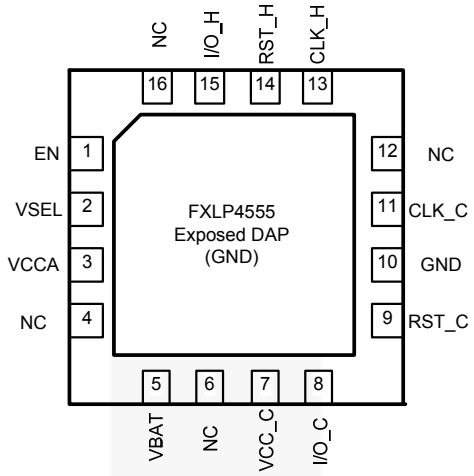


Figure 3. Pin Assignments (Top View)

Pin Definitions

Pin	Name	Type	Description
1	EN	INPUT	Power-Down Mode. EN=LOW → low-current Shutdown Mode activated. EN=HIGH → normal operation. A LOW level on this pin resets the SIM interface, switching off the V_{CC_C}.
2	VSEL	INPUT	The signal present on this pin programs the SIM_V_{CC} value: VSEL=LOW → SIM_V_{CC}=1.8V; VSEL=HIGH → SIM_V_{CC}=3V.
3	VCCA	POWER	Connected to the baseband power supply; this pin configures the level shifter input stage to accept signals from the baseband. A 0.1µF capacitor is used to bypass the power supply voltage. When V_{CCA} is below 1.1V (typical), the V_{CC_C} (SIM Card V_{CC}) is disabled and FXLP4555 enters Shutdown Mode.
4	NC		No connect. It is recommended to solder to PCB GND.
5	VBAT	POWER	LDO converter supply input. The input voltage ranges from 2.7V to 5.5V. This pin needs to be bypassed by a 0.1µF capacitor.
6	NC		No connect. It is recommended to solder to PCB GND.
7	VCC_C	POWER	Connected to the SIM card power supply pin. An internal LDO converter is programmable by the external baseband to supply either 1.8V or 3.0V output voltage. An external 1.0µF minimum ceramic capacitor must be connected across V_{CC_C} and GND. During a normal operation, the V_{CC_C} voltage can be set to 1.8V, followed by a 3.0V value, or can start directly at either of these values.
8	I/O_C	INPUT/ OUTPUT	Handles the connection to the serial I/O of the card connector. A bi-directional level translator adapts the serial I/O signal between the card and the baseband. A 14kΩ (typical) pull-up resistor provides a high-impedance state for the SIM card I/O link.
9	RST_C	OUTPUT	Connected to the RESET pin of the card connector. A level translator adapts the external reset (RST) signal to the SIM card.
10	GND	GROUND	Ground reference for the integrated circuit and associated signals. Care must be taken to avoid voltage spikes when the device operates in normal operation.
11	CLK_C	OUTPUT	Connected to the CLOCK pin of the card connector. The CLOCK (CLK) signal comes from the external clock generator; the internal level shifter adapts the voltage defined for the V_{CC_C}.
12	NC		No connect. It is recommended to solder to PCB GND.
13	CLK_H	INPUT	The clock signal, coming from the external controller, must have a duty cycle within the range defined by the specification (typically 50%). The built-in level shifter translates the input signal to the external SIM card CLK input.

Pin Definitions (Continued)

Pin	Name	Type	Description
14	RST_H	INPUT	The RESET signal present at this pin is connected to the SIM card through the internal level shifter, which translates the level according to the V_{CC_C} programmed value.
15	I/O_H	INPUT/ OUTPUT	This pin is connected to the baseband. A bidirectional level translator adapts the serial I/O signal between the smart card and the baseband. A built-in constant 18kΩ (typical) resistor provides a high-impedance state when not activated.
16	NC		No connect. It is recommended to solder to pcb GND.
17	Exposed DAP	Ground	Must be soldered to PCB ground plane.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=+25°C.

Symbol	Parameter			Min.	Typ.	Max.	Unit
V_{BAT}	LDO Power Supply Voltage			-0.5	V_{BAT}	6.0	V
V_{CCA}	Power Supply from Baseband Side			-0.5	V_{CCA}	6.0	V
V_{CC_C}	External Card Power Supply			-0.5	V_{CC_C}	6.0	V
V_{IN}	Digital Input Pin Voltage			-0.5	V_{IN}	V_{CCA}+0.5, but <6.0	V
I_{IN}	Digital Input Pin Current			-5		+5	mA
V_{OUT}	Digital Output Pin Voltage			-0.5	V_{OUT}	V_{CCA}+0.5, but <6.0	V
I_{OUT}	Digital Output Pin Current			-10		+10	mA
V_{OUT_SIM}	SIM Card Output Pin Voltage			-0.5	V_{OUT}	SIM_V_{CC}+ 0.5<6.0	V
I_{OUT_SIM}	SIM Card Output Pin Current(1)					15	mA
P_D	Power Dissipation at T_A=+85°C					440	mW
Θ_{JA}	Thermal Resistance, Junction-to-Air					72	°C/W
T_A	Operating Ambient Temperature Range			-40		+85	°C
T_J	Operating Junction Temperature Range			-40		+125	°C
T_{JMAX}	Maximum Junction Temperature					+125	°C
T_{STG}	Storage Temperature Range			-65		+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114 R=1500Ω, C=100pF	SIM Card Pins (7,8,9,10,11)	8000			V
			All Other Pins	2000			
		Charged Device Model, JESD22-C101	SIM Card Pins (7,8,9,10,11)	2000			
			All Other Pins	600			
	Moisture Sensitivity Level			1			Level

Notes:

1. Internally limited.
2. Meets or exceeds JEDEC specification EIA/JESD78 IC latchup test.

Electrical Characteristics

T_A=-40°C to +85°C. Device meets the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supply Section						
V_{BAT}	Power Supply		2.7		5.5	V
I V_{BAT}	Operating Current	I_{CC}=0mA, V_{BAT} > 3.0V if V_{SEL}=1 or V_{BAT} > 2.7V if V_{SEL}=0		16	25	µA
I V_{BAT_SD}	Shutdown Current	EN=Low			3	µA
V_{CCA}	Operating Voltage		1.65		5.50	V
I_{VCCA}	Operating Current(3)	fCLK=1MHz		7	12	µA
IV_{CCA_SD}	Shutdown Current	EN=Low			1	µA
V_{CCA}	Under-Voltage Lockout		0.6		1.5	V
V_{CC_C}	SIM Card Supply Voltage	V_{SEL}=High, V_{BAT}=3.0V, IV_{CC_C}=50mA		2.8		V
		V_{SEL}=High, V_{BAT}=3.3V – 5.5V, IV_{CC_C}=0mA - 50mA	2.8	3.0	3.2	
		VSEL=Low, V_{BAT}=2.7V – 5.5V, IV_{CC_C}=0mA - 50mA	1.7	1.8	1.9	
$I_{VCC\_C\_SC}$	Short-Circuit Current	V_{CC_C} Shorted to Ground, T_A=25°C			175	mA
Digital Input / Output Section (CLK, RST, I/O, EN, VSEL**)**						
V_{IN}	Input Voltage Range	EN, VSEL, RST_H, CLK_H, I/O_H	0		V_{CCA}	V
I_{IH}, I_{IL}	Input Current	EN, VSEL, RST_H, CLK_H	-100		100	nA
V_{IH}	High Level Input Voltage	RST_H, CLK_H, EN, VSEL	0.7 • V_{CCA}		V_{CCA}	V
V_{IL}	Low Level Input Voltage	RST_H, CLK_H			0.2 * V_{CCA}	V
		EN, VSEL	0		0.4	
$V_{OH\_I/O}$	High Level Output Voltage	I/O_C=V_{CC_C}, $I_{OH\_I/O}$=-20µA	0.7 • V_{CCA}		V_{CCA}	V
$V_{OL\_I/O}$	Low Level Output Voltage	I/O_C=0 V, $I_{OL\_I/O}$=200µA	0		0.4	V
I_{IH}	High Level Input Current	I/O	-20		20	µA
I_{IL}	Low Level Input Current	I/O			1.0	mA
R_{pu_I/O_H}	I/O Pull-Up Resistor		12	18	24	kΩ

Continued on the following page…

Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SIM Interface Section[4]						
RST_C	V_{CC_C} =+3.0V (V_{SEL}=HIGH)	Output RST_C V_{OH} at I_{RST_C}=-20µA	0.9 • V_{CC_C}		V_{CC_C}	V
		Output RST_C V_{OL} at I_{RST_C}=+200µA	0		0.4	V
		Output RST_C Rise Time at C_{OUT}=30pF (10% - 90%)[3]			1	µs
		Output RST_C Fall Time at C_{OUT}=30pF (90% - 10%)[3]			1	µs
	V_{CC_C} =+1.8V (V_{SEL}=LOW)	Output RST_C V_{OH} at I_{RST_C}=-20µA	0.9 • V_{CC_C}		V_{CC_C}	V
		Output RST_C V_{OL} at I_{RST_C}=+200µA	0		0.4	V
		Output RST_C Rise Time at C_{OUT}=30pF (10% - 90%)[3]			1	µs
		Output RST_C Fall Time at C_{OUT}=30pF (90% - 10%)[3]			1	µs
CLK_C	V_{CC_C} =+3.0V (V_{SEL}=HIGH)	Output Duty Cycle	40		60	%
		Maximum Output Frequency	5			MHz
		Output V_{OH} at I_{CLK_C}=-20µA	0.9 • V_{CC_C}		V_{CC_C}	V
		Output V_{OL} at I_{CLK_C}=+200µA	0		0.4	V
		Output CLK_C Rise Time at C_{OUT}=30pF (10% - 90%)[3]			18	ns
		Output CLK_C Fall Time at C_{OUT}=30pF (90% - 10%)[3]			18	ns
	V_{CC_C} =+1.8V (V_{SEL}=LOW)	Output Duty Cycle	40		60	%
		Maximum Output Frequency	5			MHz
		Output V_{OH} at I_{CLK_C}=-20µA	0.9 • V_{CC_C}		V_{CC_C}	V
		Output V_{OL} at I_{CLK_C}=+200µA	0		0.4	V
		Output CLK _C Rise Time at C_{OUT}=30pF (10% - 90%)[3]			18	Ns
		Output CLK_C Fall Time at C_{OUT}=30pF (90% - 10%)[3]			18	ns

Continued on the following page…

Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I/O_C	V_{CC_C}=+3.0V (V_{SEL}=HIGH)	Output V_{OH} at I_{I/O_C}=-20µA, $V_{I/O}$=V_{DD}	0.8 • V_{CC_C}		V_{CC_C}	V
		Output V_{OL} at I_{I/O_C}=+1mA, $V_{I/O}$=0V	0		0.4	V
		I/O_C Rise Time at C_{OUT}=30pF (10% - 90%)(3)			1	µs
		I/O_C Fall Time at C_{OUT}=30pF (90% - 10%)(3)			1	µs
	V_{CC_C}=+1.8V (V_{SEL}=LOW)	Output V_{OH} at I_{I/O_C}=-20µA, $V_{I/O}$=V_{DD}	0.8 • V_{CC_C}		V_{CC_C}	V
		Output V_{OL} at I_{I/O_C}=+1mA, $V_{I/O}$=0V	0		0.3	V
		I/O_C Rise Time at C_{OUT}=30Pf (10% - 90%)(3)			1	µs
		I/O_C Fall Time at C_{OUT}=30pF (90% - 10%)(3)			1	µs
R_{pu_I/O_C}	Card I/O Pull-Up Resistor		10	14	18	kΩ

Notes:

3. Guaranteed by design over the specified operating temperature range.
4. All the dynamic specifications (AC specifications) are guaranteed by characterization over the specified operating temperature range, unless otherwise indicated.

Typical Performance Characteristics

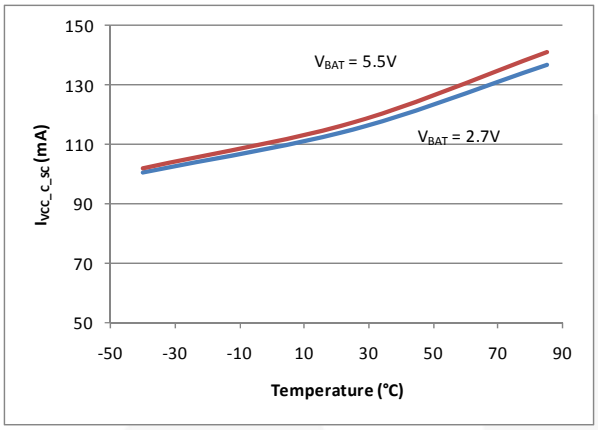


Figure 4. Short-Circuit Current ,($I_{VCC\_C\_SC}$) vs. Temperature V_{CC_C}=1.8V (V_{SEL}=LOW)

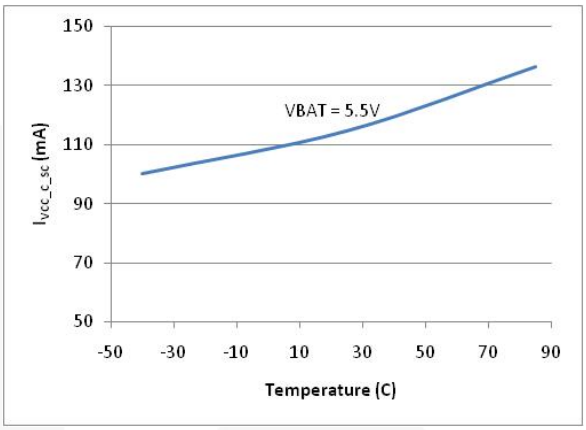


Figure 5. Short-Circuit Current, ($I_{VCC\_C\_SC}$) vs. Temperature V_{CC_C}=3.0V (V_{SEL}=HIGH)

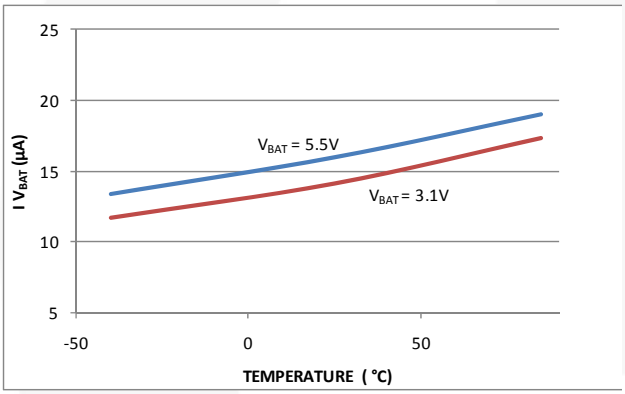


Figure 6. IV_{BAT} vs. Temperature at V_{CC_C}=3.0V (V_{SEL}=HIGH)

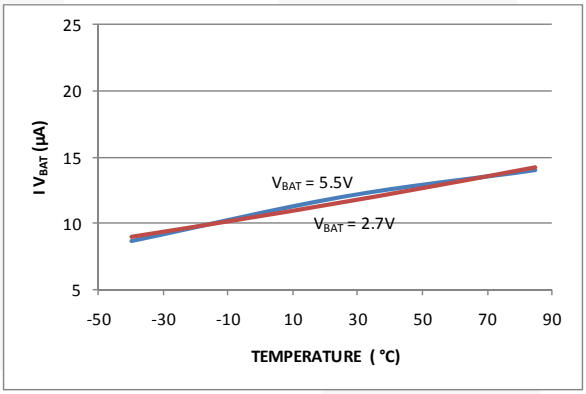


Figure 7. IV_{BAT} vs. Temperature at V_{CC_C}=1.8V (V_{SEL}=LOW)

Application Information

Card Supply Converter

The FXLP4555 interface DC-DC converter is a Low Dropout (LDO) voltage regulator capable of supplying a current in excess of 50mA under 1.8V or 3.0V. Quiescent current is typically lower than 20µA *(see Figure 6 and Figure 7).* VSEL is a select input, allowing a logic level signal to select a regulated voltage of 1.8V (VSEL = LOW) or 3.0V (VSEL = HIGH).

FXLP4555 has a shutdown input (EN) that allows it to turn off or turn on the regulator output. Figure 8 shows a simplified view of the voltage regulator. The V_{CC_C} output is internally current limited and protected against short circuits. The short-circuit current ($I_{VCC\_C\_SC}$) is constant over the SIM Card V_{CC} and $V_{BAT,}$ while it varies with operating temperature, typically in the range of 90mA to 140mA (Figure 4 and Figure 5).

To guarantee a stable LDO, the VCC_C output is connected to a 1.0µF bypass ceramic capacitor to ground. At the input, V_{BAT} is bypassed to ground with a 0.1µF ceramic capacitor.

Level Shifters

The level shifters accommodate any voltage difference between the Baseband (BB) Processor (1.65V – 5.5V) and the SIM card (1.8V or 3V). The RESET and CLOCK level shifters are uni-directional (from BB to SIM).

The bidirectional I/O line automatically adapts the voltage difference between the baseband and the SIM card in both directions. In addition, with the pull-up resistor, an active edge rate accelerator circuit (*see Figure 9*) provides a fast charge of the stray capacitance, yielding a rise time within the ISO7816-3 specifications.

The typical waveform provided in Figure 10 shows how the accelerator operates. Two distinct slew rates are observed. From 0V to approximately VCC/2, the slew rate is the RC time constant of the pull-up resistor and the stray capacitance. When the input slope crosses the VCC/2 threshold, the edge rate accelerator is activated, resulting in the faster slew rate from approximately VCC/2 to V_{CC} as depicted in Figure 10.

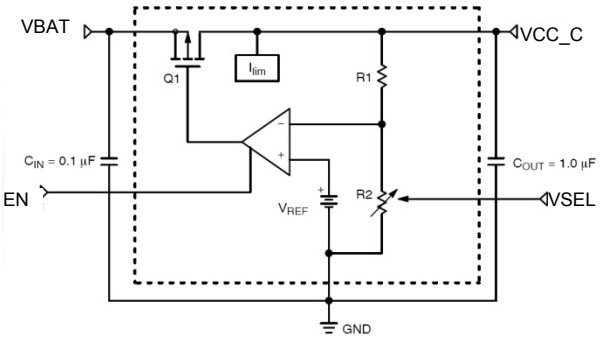


Figure 8. Simplified Block Diagram of the LDO Voltage Regulator

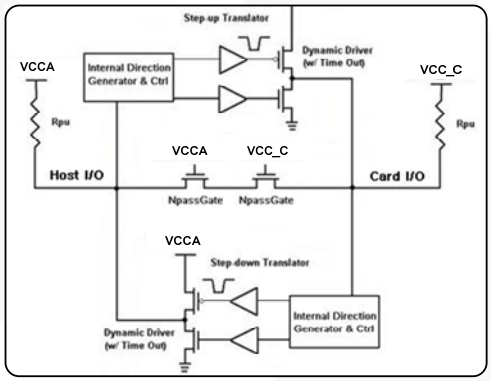


Figure 9. Basic I/O Line Interface

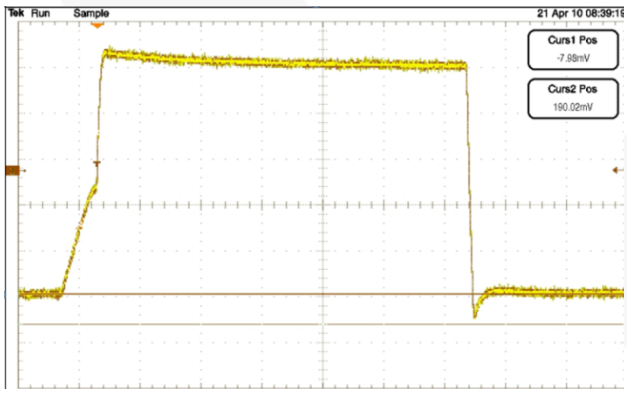


Figure 10. SIM_IO Typical Rise and Fall Times with Stray Capacitance > 30pF (33pF Capacitor Connected on the Board)

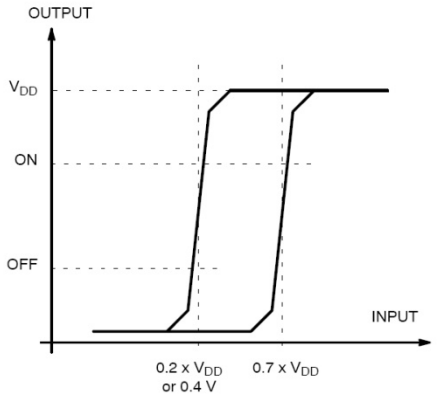


Figure 11. Typical Schmitt Trigger Characteristics

Applications Information (Continued)

Input Schmitt Triggers

All the logic input pins (except I/O_H and I/O_C) have built-in Schmitt trigger circuits to prevent uncontrolled operation. Typical dynamic characteristics of the related pins are depicted in Figure 11.

The output signal is guaranteed to go HIGH when the input voltage is above 0.7 x V_{DD} and go LOW when the input voltage is below 0.4V. *See Electrical Characteristics section.*

Shutdown Operating

To save power, it is possible to put the FXLP4555 in Shutdown Mode by setting the pin EN LOW. The device enters Shutdown Mode automatically when V_{CCA} goes lower than 1.1V typically.

ESD Protection

The FXLP4555 SIM interface features an HBM ESD voltage protection in excess of 7kV for all the SIM pins (IO_C, CLK_C, RST_C, VCC_C and GND). All the other pins (Host side) sustain at least 2kV. The HBM ESD voltage required by the ISO7816 standard is 4kV.

Printed Circuit Board (PCB) Layout

Careful layout routing should be applied to achieve efficient operating of the device in its mobile or portable environment and to fully exploit its performance.

The bypass capacitors must be connected as close as possible to the device pins (VCC_C, VCCA, or VBAT) to reduce possible parasitic behaviors (ripple and noise). It is recommended to use ceramic capacitors.

The exposed pad should be connected to ground as well as the unconnected pins (NC). A relatively large ground plane is recommended.

Clock Stop

Section 6.3.2 of ISO7816-3 identifies the “Power Management” feature of Clock Stop. For cards supporting Clock Stop, when the interface device expects no transmission from the card and when I/O has remained at state H for at least 1,860 clock cycles (delay t_g), then according to Figure 13, the interface device may stop the clock on CLK (at time t_e) while the SIM card V_{CC} remains powered and RST at state H.

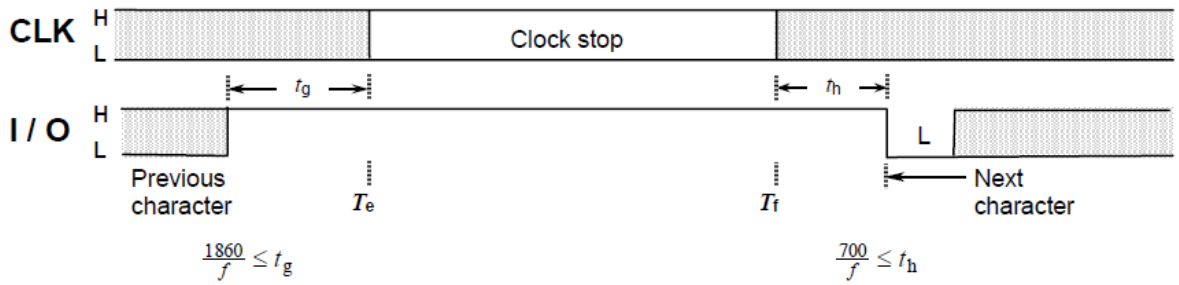


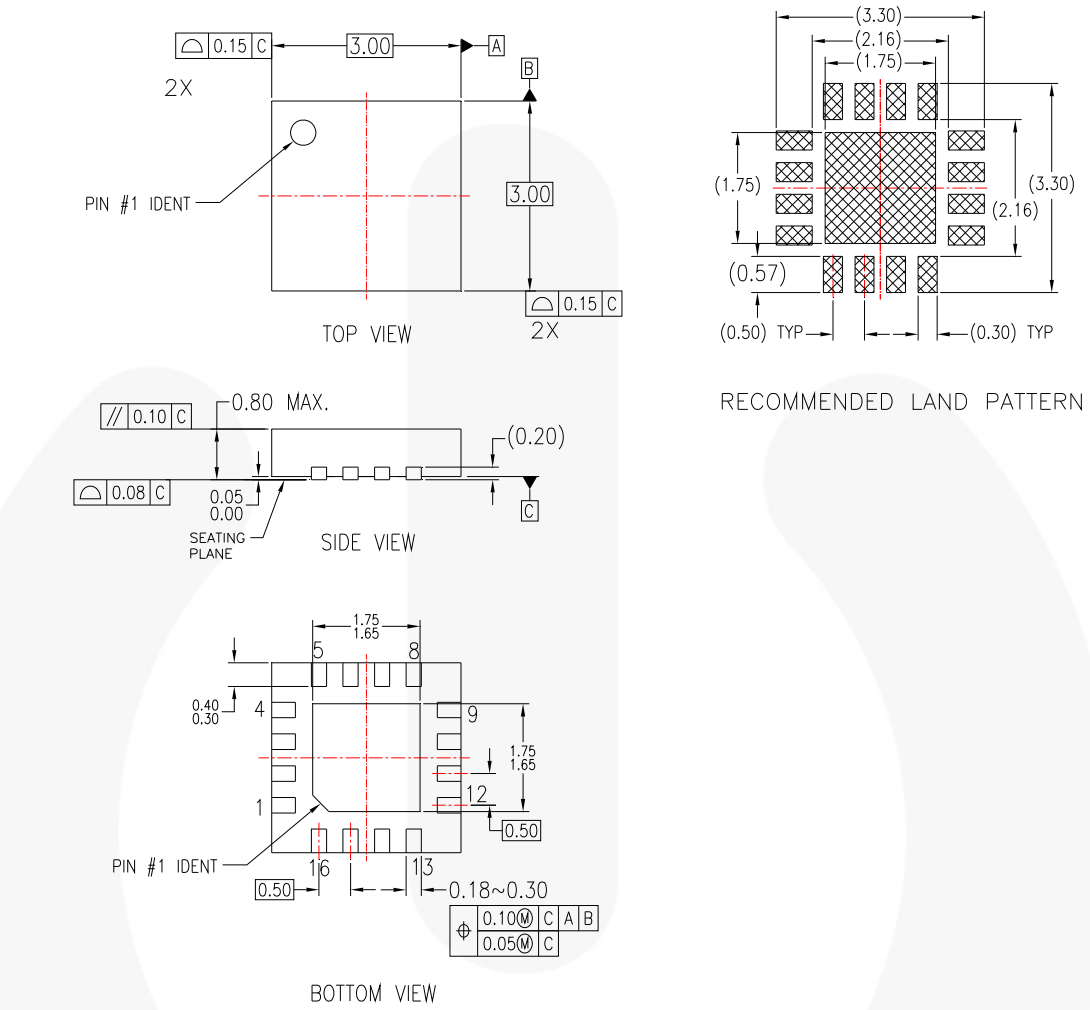
Figure 12. Clock Stop

When the clock is stopped (from time t_e to time t_f), CLK shall be maintained either at state H or at state L, according to the clock stop indicator X defined in section 8.3 of the ISO7816-3 specification.

At time t_f, the interface device restarts the clock and the information exchange on I/O may continue after at least 700 clock cycles (at time $t_f + t_h$).

The FXLP4555 supports the above description of Clock Stop per ISO7816-3 specifications.

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WEED-Pending, DATED pending

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MLP16BrevB

Figure 13. 16-Lead, Molded Leadless Package (MLP), QUAD, JEDEC MO-220, 3mm Square

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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http://www.fairchildsemi.com/packaging/MLP16B.html.

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EcoSPARK®
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ESBC™
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FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
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Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
mWSaver™
OptoHiT™
OPTOLOGIC®
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Power-SPM™
PowerTrench®
PowerXS™
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QFET®
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Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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