HARRIS SEMICONDUCTOR

HC5520

CO/PABX Polarity Reversal Subscriber Line Interface Circuit

April 1997

Features

- Normal and Reversed DC Feed
- Current Limited Loop Feed
- Ringing, Test-In, and Test-Out Relay Drivers
- Thermal Shutdown Protection with Alert Signal
- On-Hook Transmission
- Selectable Transmit and Receive Gain Setting
- Selectable 2-Wire Impedance Matching
- Zero Crossing Ring Trip Detection and Ring Relay Release
- Parallel Digital Control and Status Monitoring
- Protection Resistors Inside Feedback Loop Allows the Use of PTC Devices Without Impact on Longitudinal Balance
- Thermal Management Features

Applications

- CO/PABX Line Circuits

Description

The HC5520 is a Monolithic Subscriber Line Interface Circuit (SLIC) for Analog Subscriber Line cards in Central Office and PABX switches.

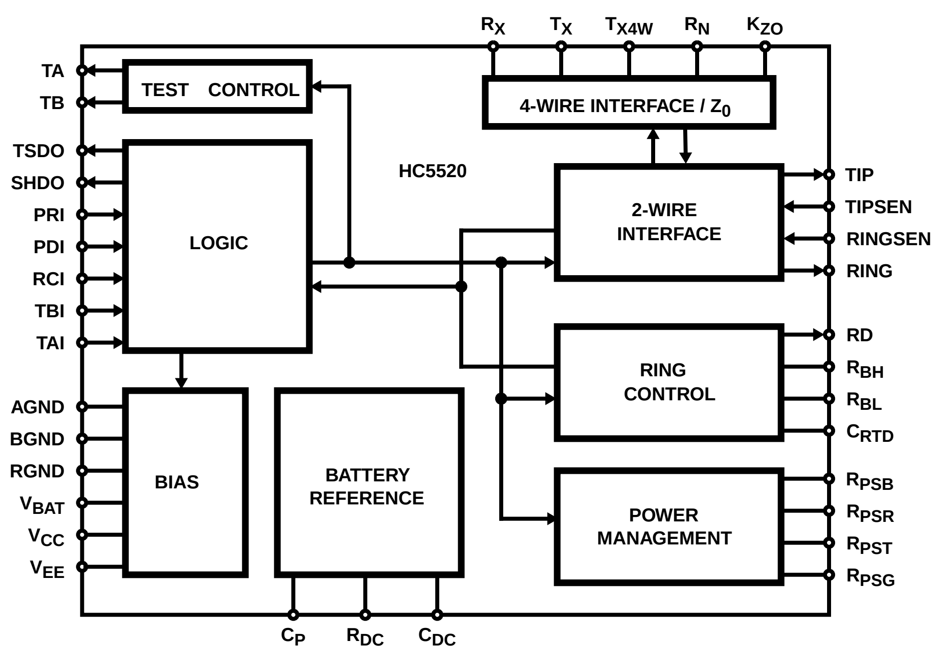
The HC5520 provides a comprehensive set of features for these applications including loop reversal, zero crossing ringing relay operation, long loop drive and a mutually independent setting of the receive and transmit gains, and the two wire impedance synthesis. Advanced power management features combined with a small 44 lead MQFP package allow significant board space to be freed up for additional line circuits.

The HC5520 is fabricated in a Harris state-of-the-art Bonded Wafer High Voltage process, providing freedom from traditional JI latch-up phenomena without the use of additional power supply filtering components or substrate tie connections. The very low parasitics and leakages associated with this process provide an exceptionally flat performance over frequency and temperature.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HC5520CQ	0 to 70	44 Ld MQFP	Q44.10x10
HC5520CM	0 to 70	44 Ld PLCC	N44.65

Block Diagram



Absolute Maximum Ratings (Note 1)

V_{CC} to AGND 7V
V_{EE} to AGND . . . . -7V
V_{BAT} to BGND 80V
AGND to BGND . . . . ±3V
Digital Pins to AGND . . . . -0.5V to 7V
ESD Withstand (Human Body Model) 500V

Operating Conditions

Temperature Range
HC5520CQ . . . . 0^oC to 70^oC
HC5520CM . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
MQFP Package	66
PLCC Package	46

Maximum Power Dissipation
MQFP package 1.21W
PLCC Package 1.74W
Maximum Junction Temperature . . . . 150^o
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(Lead tips only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Recommended Operating Conditions

For maximum integrity, nominal operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Supply	V_{BAT}		-42	-48	-58	V_{DC}
Positive Supply	V_{CC}		4.75	5	5.25	V_{DC}
Negative Supply	V_{EE}		-4.75	-5	-5.25	V_{DC}
Ringing Supply	$V_{RINGING}$		60	75	90	V_{RMS}
Loop Resistance	R_L		200	-	1800	Ω
Ambient Temperature	T_A		0	25	70	^oC
Die Temperature	T_D		-	-	150	^oC

Electrical Specifications

Unless Otherwise Specified: Typical Parameters are at $T_A = 25^oC$, $V_{CC} = +5V$, $V_{EE} = -5V$, $V_{BAT} = -48V$, AGND = BGND = RGND = 0V, Min-Max Parameters are Over Power Supply and Operating Temperature Range. All Transmission Parameters are Specified at 600Ω 2-Wire Terminating Impedance with 0dB transmit and receive gain.

PARAMETER	CONDITIONS					MIN	TYP	MAX	UNITS
	MODE	LOAD	V_{BAT}	OTHER CONDITIONS	FREQ/ LEVEL				
POWER SUPPLY CURRENTS (Figure 4)									
I_{CC}	normal reverse p'down	Open	-48V	$V_{CC} = 5V$		5.0 6.0 2.0	8.0 8.9 3.7	11.0 12.0 5.5	mA mA mA
I_{EE}	normal reverse p'down	Open	-48V	$V_{EE} = -5V$		-6.0 -7.0 -3.0	-3.6 -4.9 -1.7	-2.0 -3.0 -0.7	mA mA mA
I_{BB}	normal reverse p'down	Open	-48V	$V_{CC} = 5V$, $V_{EE} = -5V$		-7.0 -7.0 -1.0	-4.2 -4.0 -0.4	-2.0 -2.0 0.0	mA mA mA
THERMAL SHUTDOWN									
Thermal Shutdown Temperature, Die Temperature	normal reverse		-48V			-	150	-	^oC
BATTERY FEED CHARACTERISTICS - 2W VOLTAGES (Figure 4)									
V_{TIP}	normal reverse	Open	-48V			-5.50 -46.00	-4.16 -43.60	-2.46 -42.00	V V

Electrical Specifications Unless Otherwise Specified: Typical Parameters are at T_A = 25°C, V_{CC} = +5V, V_{EE} = -5V, V_{BAT} = -48V, AGND = BGND = RGND = 0V, Min-Max Parameters are Over Power Supply and Operating Temperature Range. All Transmission Parameters are Specified at 600Ω 2-Wire Terminating Impedance with 0dB transmit and receive gain. **(Continued)**

PARAMETER	CONDITIONS					MIN	TYP	MAX	UNITS
	MODE	LOAD	V_{BAT}	OTHER CONDITIONS	FREQ/ LEVEL				
V_{RING}	normal reverse	Open	-48V			-45.54 -6.00	-43.80 -4.26	-42.50 -2.00	V V
V_{TIP}	normal reverse	Open	-42V			-5.00 -40.00	-3.68 -38.12	-2.46 -37.00	V V
V_{RING}	normal reverse	Open	-42V			-39.54 -5.00	-38.34 -3.78	-37.00 -2.00	V V
BATTERY FEED CHARACTERISTICS - LOOP CURRENT (Figure 5)									
Normal Loop Current	normal reverse	1800Ω	-42V			14.5 14.5	16.5 16.3	19.0 19.0	mA mA
Normal Loop Current	normal reverse	1800Ω	-48V			18.0 18.0	18.8 18.6	22.0 22.0	mA mA
Short Circuit Loop Current Limit	normal reverse	100Ω	-48V			22.0 22.0	26.4 27.0	42.0 42.0	mA mA
LOOP SUPERVISION - SWITCH HOOK DETECTION (Figure 6)									
Off-Hook Detection	normal reverse		-48V			2.4K	4.6K	9K	Ω
LOOP SUPERVISION - DIAL PULSE DISTORTION (Figure 7)									
Dial Pulse Distortion	normal	100Ω	-58V	25°C		-	0.1	3	%
Dial Pulse Distortion	normal	1800Ω	-42V	25°C		-	0.1	3	%
LOOP SUPERVISION - RING TRIP DETECTION (Figure 8)									
Ring Trip Detect	Ringing	1800Ω +1REN	-42V $60V_{RMS}$			-	-	150	ms
Ring Trip Non-Detect	Ringing	3REN// 20KΩ	-58V $90V_{RMS}$			20K	-	-	Ω
LOOP SUPERVISION - POLARITY REVERSAL TIME (Figure 9)									
Polarity Reversal Time	normal to reverse	1800Ω	-42V			-	0.04	10	ms
Polarity Reversal Time	reverse to normal	1800Ω	-42V			-	0.04	10	ms
LOOP SUPERVISION - DIGITAL INTERFACE									
Input Low Voltage, V_{IL}	All Digital Inputs					-	-	0.8	V
Input High Voltage, V_{IH}	All Digital Inputs					2.0	-	-	V
Input Low Current, I_{IL}	AGND < V_{IN} < V_{IL}					-20	-	-	µA
Input High Current, I_{IH}	V_{IH} < V_{IN} < V_{CC}					-	0	+10	µA
Output Low Voltage, V_{OL}	1 LSTTL Load					-	-	0.4	V
Output High Voltage, V_{OH}	1 LSTTL Load					2.4	-	-	V
Relay Driver Output Low Voltage, V_{OL}	V_{CC} = 4.75V, Load = 35mA					-	0.4	0.8	V
Relay Driver Output High Current, I_{OH}	V_{CC} = 5.25V					-	-	10	µA

Electrical Specifications Unless Otherwise Specified: Typical Parameters are at $T_A = 25^oC$, V_{CC} = +5V, V_{EE} = -5V, V_{BAT} = -48V, AGND = BGND = RGND = 0V, Min-Max Parameters are Over Power Supply and Operating Temperature Range. All Transmission Parameters are Specified at 600Ω 2-Wire Terminating Impedance with 0dB transmit and receive gain. **(Continued)**

PARAMETER	CONDITIONS					MIN	TYP	MAX	UNITS
	MODE	LOAD	V_{BAT}	OTHER CONDITIONS	FREQ/ LEVEL				
TRANSMISSION PARAMETERS - 4-WIRE TO 2-WIRE RECEIVE GAIN (Figure 10)									
Absolute Receive Gain, ARG	normal reverse	600Ω	-48V		1020Hz 0dBm	-0.2	0	+0.2	dB
TRANSMISSION PARAMETERS - 4-WIRE TO 2-WIRE FREQUENCY RESPONSE (Figure 10)									
Receive Frequency Response Relative to ARG	normal reverse	600Ω	-48V	300 to 3.4kHz	0dBm	-0.15	0	+0.15	dB
TRANSMISSION PARAMETERS - 4-WIRE TO 2-WIRE GAIN TRACKING (Figure 10)									
Receive Gain Tracking Relative to ARG	normal reverse	600Ω	-48V	+3 to -40dBm0 -40 to -50dBm0	1020Hz	-0.12 -	0 0	+0.12 -	dB dB
TRANSMISSION PARAMETERS - 4-WIRE TO 2-WIRE SIGNAL TO DISTORTION (Figure 10)									
Receive Signal to Distortion and Noise	normal reverse	600Ω	-48V	+3 to -40dBm0 -40 to -50dBm0	1020Hz	33 -	38 33	- -	dB dB
TRANSMISSION PARAMETERS - 4-WIRE TO 2-WIRE IDLE CHANNEL NOISE (Figure 10)									
Idle Channel Noise	normal reverse	600Ω	-48V	P-Message		73	78	-	dBm0P
TRANSMISSION PARAMETERS - 2-WIRE TO 4-WIRE TRANSMIT GAIN (Figure 11)									
Absolute Transmit Gain, ATG	normal reverse	600Ω	-48V		1020Hz 0dBm	-0.2	-0.07	+0.2	dB
TRANSMISSION PARAMETERS - 2-WIRE TO 4-WIRE FREQUENCY RESPONSE (Figure 11)									
Transmit Frequency Response Relative to ATG	normal reverse	600Ω	-48V	300 to 3.4kHz	0dBm	-0.2	-0.04	+0.2	dB
TRANSMISSION PARAMETERS - 2-WIRE TO 4-WIRE GAIN TRACKING (Figure 11)									
Transmit Gain Tracking Relative to ATG	normal reverse	600Ω	-48V	+3 to -40dBm0 -40 to -50dBm0	1020Hz	-0.12 -	0 0.02	+0.12 -	dB dB
TRANSMISSION PARAMETERS - 2-WIRE TO 4-WIRE SIGNAL TO DISTORTION (Figure 11)									
Transmit Signal to Distortion and Noise	normal reverse	600Ω	-48V	+3 to -40dBm0 -40 to -50dBm0	1020Hz	33 -	38 33	-	dB dB
TRANSMISSION PARAMETERS - 2-WIRE TO 4-WIRE IDLE CHANNEL NOISE (Figure 11)									
Idle Channel Noise	normal reverse	600Ω	-48V	P Message		73	78	-	dB
TRANSMISSION PARAMETERS - 2-WIRE RETURN LOSS (Figure 12)									
2-Wire Return Loss	normal reverse	600Ω	-48V	R_N = 6490Ω K_{ZO} = 15400Ω	1020Hz 0dBm	30	45	-	dB
TRANSMISSION PARAMETERS - 4-WIRE TO 4-WIRE INSERTION LOSS (Figure 13)									
4-Wire to 4-Wire Insertion Loss	normal reverse	600Ω	-48V		1020Hz 0dBm	-0.2	-0.02	+0.2	dB
TRANSMISSION PARAMETERS - TRANSHYBRID BALANCE (Figure 13)									
Transhybrid Balance	normal reverse	600Ω	-48V		1020Hz 0dBm	30	38	-	dB

Electrical Specifications Unless Otherwise Specified: Typical Parameters are at $T_A = 25^oC$, V_{CC} = +5V, V_{EE} = -5V, V_{BAT} = -48V, AGND = BGND = RGND = 0V, Min-Max Parameters are Over Power Supply and Operating Temperature Range. All Transmission Parameters are Specified at 600Ω 2-Wire Terminating Impedance with 0dB transmit and receive gain. **(Continued)**

PARAMETER	CONDITIONS					MIN	TYP	MAX	UNITS
	MODE	LOAD	V_{BAT}	OTHER CONDITIONS	FREQ/ LEVEL				
TRANSMISSION PARAMETERS - 4-WIRE TO 4-WIRE ABSOLUTE DELAY									
Absolute Delay	normal reverse	600Ω	-48V		1020Hz 0dBm		1.5		µs
TRANSMISSION PARAMETERS - OVER LOAD LEVEL (Figures 14, 15)									
Receive Over Load Level at 4W and 2W	normal reverse	600Ω	-42V	1% THD	1020Hz	2.5	-	-	V_{PEAK}
Transmit Over Load Level at 2W and 4W	normal reverse	600Ω	-42V	1% THD	1020Hz	2.15	-	-	V_{PEAK}
TRANSMISSION PARAMETERS - LONGITUDINAL IMPEDANCE (Figure 16)									
Longitudinal Impedance per Wire	normal reverse	-	-48V		40Hz to 100Hz	-	50	-	Ω
TRANSMISSION PARAMETERS - LONGITUDINAL CURRENT CAPABILITY (Figure 17)									
Longitudinal Current Limit per Wire	normal reverse	-	-42V	Triangle Waveform	40Hz to 100Hz	15	-	-	mA_{PEAK}
TRANSMISSION PARAMETERS - LONGITUDINAL BALANCE (Figure 18)									
2-Wire Longitudinal Balance	normal reverse	368Ω + 368Ω	-48V		300Hz 1020Hz 3400Hz	42 48 48	62.2 58.7 69.5	-	dB dB dB
4-Wire Longitudinal Balance	normal reverse	368Ω + 368Ω	-48V		300Hz 1020Hz 3400Hz	42 48 48	66.0 67.2 77.0	-	dB dB dB
POWER SUPPLY REJECTION RATIO (Figure 19)									
PSRR V_{BAT} To 4-Wire	normal reverse	600Ω	-48V	V_{BAT} = -48V + $100mV_{RMS}$	300Hz	30	42	-	dBC
PSRR V_{BAT} To 2-Wire	normal reverse	600Ω	-48V	V_{BAT} = -48V + $100mV_{RMS}$	300Hz	30	42	-	dBC
PSRR V_{CC} To 4-Wire	normal reverse	600Ω	-48V	V_{CC} = 4.75V + $100mV_{RMS}$	300Hz	20	33	-	dBC
PSRR V_{CC} To 2-Wire	normal reverse	600Ω	-48V	V_{CC} = 4.75V + $100mV_{RMS}$	3420Hz	20	24	-	dBC
PSRR V_{EE} To 4-Wire	normal reverse	600Ω	-48V	V_{EE} = -4.75V + $100mV_{RMS}$	2500Hz	20	30	-	dBC
PSRR V_{EE} To 2-Wire	normal reverse	600Ω	-48V	V_{EE} = -4.75V + $100mV_{RMS}$	2500Hz	20	32	-	dBC

Circuit Operation and Design Information

The HC5520 is a current feed voltage sense **S**ubscriber **L**ine **I**nterface **C**ircuit (SLIC). It provides extensive digitally controlled supervisory functions, DC loop feed functions, and user selectable 2 wire impedance matching functions.

Modes of Operation

The HC5520 has seven possible modes of operation. These modes of operation are either controlled by the digital control inputs to the SLIC or controlled by the loop status output of the SLIC. The modes of operation and the function of the digital control inputs are given in Table 1.

TABLE 1.

OPERATION	MODE	SLIC FUNCTION	CONTROL INPUTS
Normal Loop Feed	Normal	Normal	PRI = High
Reverse Loop Feed	Reverse	Normal	PRI = Low
Loop Powerdown	P'down	Loop power down	PDI = Low
Ringing	Ringing	Ring trip detection only	RCI = Low
Test out	Test-out	Normal	TAI = Low
Test in	Test-in	Normal	TBI = Low
Thermal Shut Down	TSD	Loop Powerdown	

Normal Loop Feed Mode

When PDI = 1, setting the PRI to a logic "1" places the SLIC in the Normal Loop Feed mode. This is the normal operational mode of the SLIC. With a nominal battery supply of -48V and an on-hook condition, the voltage at the Tip terminal will be approximately 8% of the battery supply voltage. In this case the Tip voltage is about -3.8V. Similarly, the voltage at the Ring terminal will be approximately 92% of the battery supply voltage or about -44.2V.

In the Normal mode the Tip voltage is more positive than the Ring voltage; therefore, in an off-hook condition, the DC loop current flows from Tip to Ring. The loop feeding characteristics will be given in the battery feed section. All of the specifications applicable to this mode of operation are provided in the electrical specifications portion of the HC5520 data sheet.

Reverse Loop Feed Mode

When PDI = 1, setting the PRI to a logic "0" places the SLIC in the Reverse Loop Feed mode. In this mode, the Ring terminal voltage is more positive than the Tip terminal voltage. Thus, in an off-hook condition, the DC loop current flows from Ring to Tip. The loop feeding characteristics in the Reverse mode are the same as in the Normal mode. All of the specifications applicable to this mode of operation are provided in the electrical specifications portion of the HC5520 data sheet.

Battery Feed

The HC5520 is designed to provide a 300Ω resistive feed (150Ω per wire) for long loop applications. It will supply a DC loop feed current of 18mA into an 1800Ω loop at the nominal battery supply of -48V. At shorter loop lengths or higher battery supply voltages, the DC feed is current-limited to nominally 26mA in order to conserve power. For internal chip power management purposes, external power sharing resistors are used to provide some of the DC loop current. This allows a substantial amount of the power to be dissipated off the chip, particularly in short loop applications. A typical loop feeding characteristic for Normal and Reverse Loop Feed Modes of operation is shown in Figure 1.

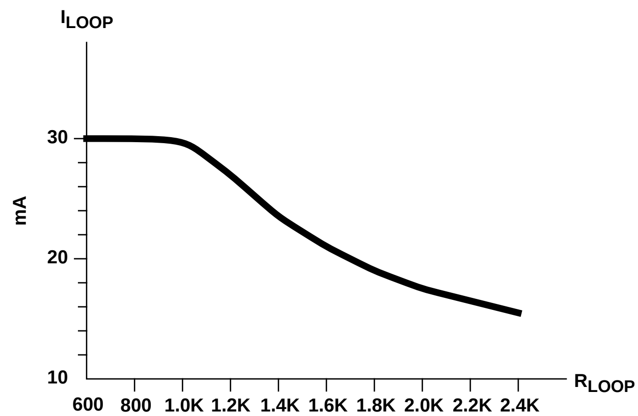


FIGURE 1. BATTERY FEED CHARACTERISTICS

Loop Supervision - Switch Hook Detection

The Loop Supervision circuit operates in the Normal and Reverse Loop Feed modes. The DC loop current is monitored and the off-hook condition is indicated when the loop resistance is less than 2.4kΩ. When this occurs, the SHDO output will be set to a logic low in order to signal the system that an off-hook condition exists. If the subscriber is using a rotary dial telephone, the system can monitor the dial pulses through the SHDO output.

Ringing - Ring Trip Detection Mode

The ringing voltage is cadenced to a subscriber loop by applying a logic signal to the Rci input. When a logic "0" is received at the RCI input, the HC5520 will set the RD output to low and thus pull current through the ring relay coil and energize the ring relay. This causes the subscriber's telephone to begin ringing. At this time the ringing current through the ring ballast resistor is monitored to determine whether an off-hook condition is present. Once the subscriber goes off-hook, the ring trip circuit will turn off the ring relay after the next occurrence of a zero net current flow through the ring ballast resistor. At the same time, the SHDO output will be set to a logic low to indicate the ring trip detection. The ring relay can not be reenergized until the system acknowledges that a ring trip has occurred. Acknowledgment is achieved by setting the RCI to a logic high.

If the subscriber goes off-hook during the silent portion of the ringing cadence, the off-hook condition is detected in the same manner as a switch hook detection. The SHDO output will be set to a logic low in order to indicate that the subscriber has answered the call and that ringing of the line should cease.

Loop Power Down Mode

Under any condition when PDI is set to a logic “0”, the SLIC will power down the two wire loop. During loop power down, the voltages at Tip and Ring are both collapsed to one-half of the battery voltage and the outputs of the Tip and Ring feed amplifiers are in a high impedance state. Therefore all of the supervisory functions and transmission functions are disabled. The HC5520 will resume normal operation once the loop power down command is removed.

Thermal Shutdown Mode

The SLIC will power down the loop by itself once the temperature of the SLIC die reaches 150^{o}C. During this thermal shutdown condition, both TSDO and SHDO outputs will be set to a default logic low to indicate the condition. The supervisory functions and transmission functions are disabled. Once the SLIC die temperature drops 10^{o}C lower than the thermal shutdown temperature, the SLIC will resume operation.

Test-Out and Test-In Modes

Two additional relay drivers are provided for test-out and test-in functions. Unlike the ring relay driver circuit, these relay drivers are operated independently of the rest of the HC5520 circuitry. The designation of test-out and test-in is purely arbitrary. When desired, the subscriber’s loop condition can be interrogated through the test-out relay. Likewise, through the test-in relay, the various SLIC functions and signal integrity can be examined.

Hybrid Transmission Model

Figure 2 shows a simplified model for bidirectional signal transmission and 2-wire impedance synthesis. The term R_{SENSE} used in the equations below refers to the pair of external 100kΩ sense resistors R_{TPS} and R_{RGS}. The HC5520 architecture gives the user the flexibility to set the gains and 2-wire impedance with external resistors and resistor ratios. However, to prevent adversely affecting other SLIC control functions, the value of R_{SENSE} should always be selected to be 100kΩ.

2W Impedance

The 2W impedance is the AC input impedance synthesized by the SLIC between the Tip and Ring terminals and will be referred to as ZO. The value of ZO is user programmable by varying the value R_N and Z_{KZO}. R_N is recommended to be less than 7kΩ. Z_{KZO} can be either a real resistance or a complex impedance network. ZO is determined by the following equation:

$$ZO = \frac{R_{SENSE} \bullet Z_{KZO}}{400 \bullet R_N}$$

where R_{SENSE} is constrained to be 100kΩ.

4W to 2W Gain

The signal level voltage gain from the 4-wire analog input (R_X) to the 2-wire ΔV_{TR} voltage is user programmable using the following equation:

$$A_{4-2} = \frac{-R_{SENSE}}{R_X}$$

where R_{SENSE} is constrained to be 100kΩ. The SLIC has a built-in +6.02dB gain to compensate for the divider effect of matching the load impedance, making it transparent to the user.

2W to 4W Gain

The signal level voltage gain from the Tip and Ring terminals (ΔV_{TR}) to the output of the 4-wire signal amplifier (R_{4W}) is user programmable using the following equation:

$$A_{2-4} = \frac{R_{4W}}{R_{SENSE}}$$

Transhybrid Balance

Functionally, when a voice signal is received at V_{RX} a current which is proportional to the voice signal will pass through the SLIC 4 wire input R_X pin. This voice input current will be amplified and inverted to drive the load across the Tip and Ring. The AC voltages at Tip and Ring are fed back to the SLIC and reproduced as the transmit signal at the T_X pin. This received voice signal returned from 2 wire side of the SLIC will have the same amplitude as the received AC signal but will be 180 degrees out of phase. This signal needs to be eliminated from transmission to prevent far end echo.

The most common way of implementing the transhybrid balance function is to use the analog voice input amplifier in the Combo as a summing amplifier. The circuit connections are as shown in Figure 3. Notice that the input impedance networks for both received signal and returned signal are bascally the same, if the 62pF capacitor were not added. The addition of the 62pF capacitor to ground is to compensate for the phase shift of the returned signal to achieve 15dB or more improvement in the 2k to 4kHz frequency band as compared to the data collected from the test circuit.

Sensitive Pins

Tipsen, Ringsen Pins - These pins are very low impedance virtual grounds used for providing feedback current to the HC5520 DC, AC, and Longitudinal control loops. Parasitic capacitance on these pins from the PC board layout and external components should be minimized to prevent oscillation.

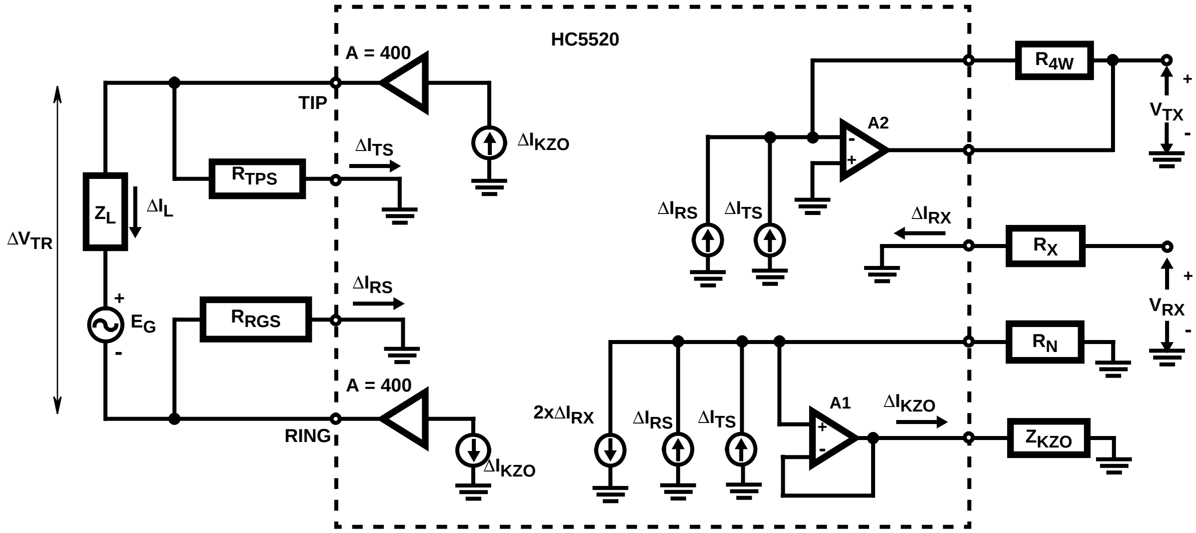


FIGURE 2. SIMPLIFIED AC TRANSMISSION CIRCUIT

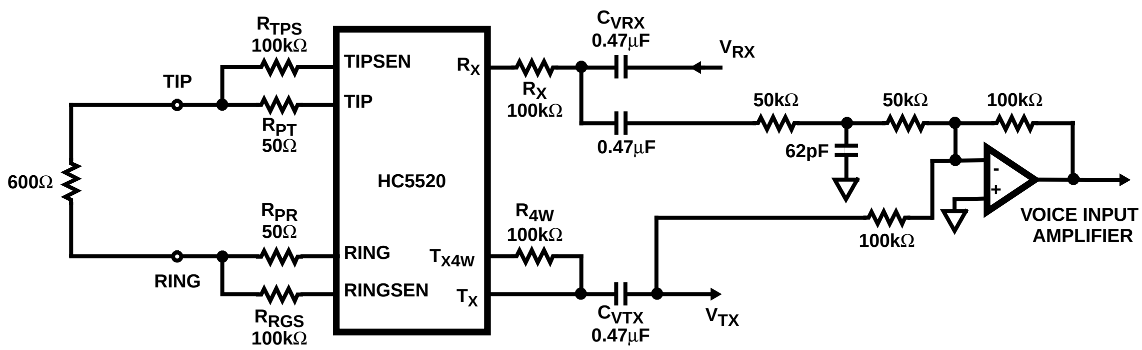


FIGURE 3. TRANSHYBRID BALANCE CIRCUIT WITH HIGH AND LOW FREQUENCY COMPENSATION

K_{ZO} Pin - The 2-wire impedance that is synthesized by the HC5520 is a direct function of the network connected to this pin (see equations). Parasitic capacitance and inductance from the PC board layout and the external components is magnified by the same K factor that is utilized to synthesize the 2-wire impedance. Excessive parasitics can cause insertion loss and return loss degradation, especially at higher voice band frequencies. Good PC board layout techniques and proper component selection can minimize these effects to a negligible level.

R_N Pin - This pin connects an external resistor to the input of an internal buffer. The value of this resistor is user specified based upon the impedance desired at the 2-wire interface (see equations). The value chosen must not have a value greater than 7kΩ or the input voltage range of the buffer may be exceeded during transients.

R_{DC} Pin - An external resistor connected to V_{CC} is required at this pin to provide an accurate reference for the DC currents which feed the subscriber loop. PC board traces should be made to have low resistance and should connect directly to V_{CC}.

C_{DC} Pin - This pin provides a connection to the DC reference nodes that control the DC loop feed current. These internal blocks are referenced to V_{EE} and it is important that the capacitor be referenced to V_{EE} or else the PSRR performance will be degraded.

C_P Pin - Capacitor C_P connects to this pin to create a lowpass filter for the half-battery internal reference point. It is important that this capacitor be referenced to BGND/AGND to minimize the effect of noise injected into the subscriber loop from the battery supply.

R_{PSG}, R_{PST}, R_{PSR}, R_{PSB} Pins - These pins are connected to critical nodes inside the HC5519R3931 feedback control loops. Parasitic capacitance should be minimized in order to prevent oscillations.

RD, TB, TA Pins - The pins connect to the driver coils of the Ring and Test relays and activate the relays by pulling down the coil voltage to ground. The driver outputs are internally clamped to V_{CC} by diodes to prevent the inductive voltage transient during relay turn-off from damaging the driver. Relays attached to any voltage other than V_{CC} will not function properly.

Test Information

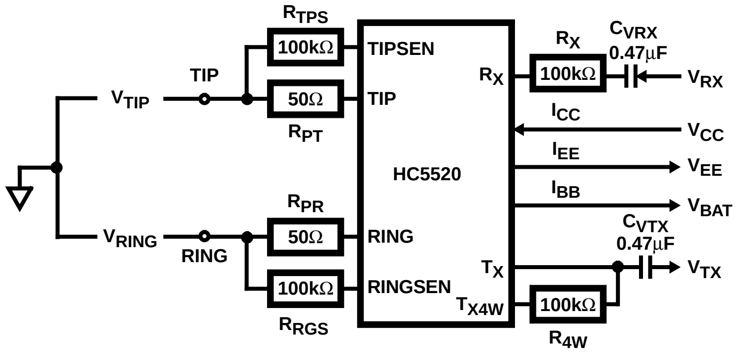


FIGURE 4. POWER SUPPLY CURRENT AND TIP AND RING VOLTAGE TEST CIRCUIT

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
Power Supply Current, I_{CC}	V_{CC} = +4.75 ~ +5.25V	I_{CC} Direct Measurement	I_{CC}
Power Supply Current, I_{EE}	V_{EE} = -4.75 ~ -5.25V	I_{EE} Direct Measurement	I_{EE}
Power Supply Current, I_{BB}	V_{BAT} = -42 ~ -58V	I_{BB} Direct Measurement	I_{BB}
V_{TIP}	V_{BAT}	V_{TIP} Direct Measurement	V_{TIP}
V_{RING}	V_{BAT}	V_{RING} Direct Measurement	V_{RING}

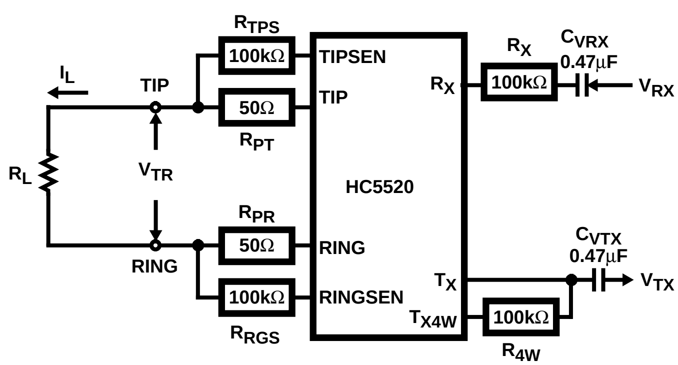


FIGURE 5. LOOP CURRENT TEST CIRCUIT

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
Loop Current, I_L	V_{BAT} and R_L	V_{TR}	$I_L = V_{TR}/R_L$
Short Circuit Loop Current	V_{BAT} = -48V and R_L = 100Ω	V_{TR}	$I_L = V_{TR}/R_L$

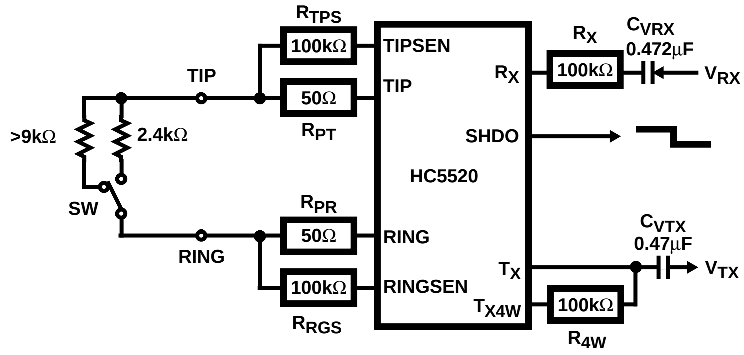


FIGURE 6. SWITCH HOOK DETECTION TEST CIRCUIT

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
On Hook Condition	SW = Left	SHDO	SHDO = Hi
Off Hook Detection	SW = Right	SHDO	SHDO = Lo

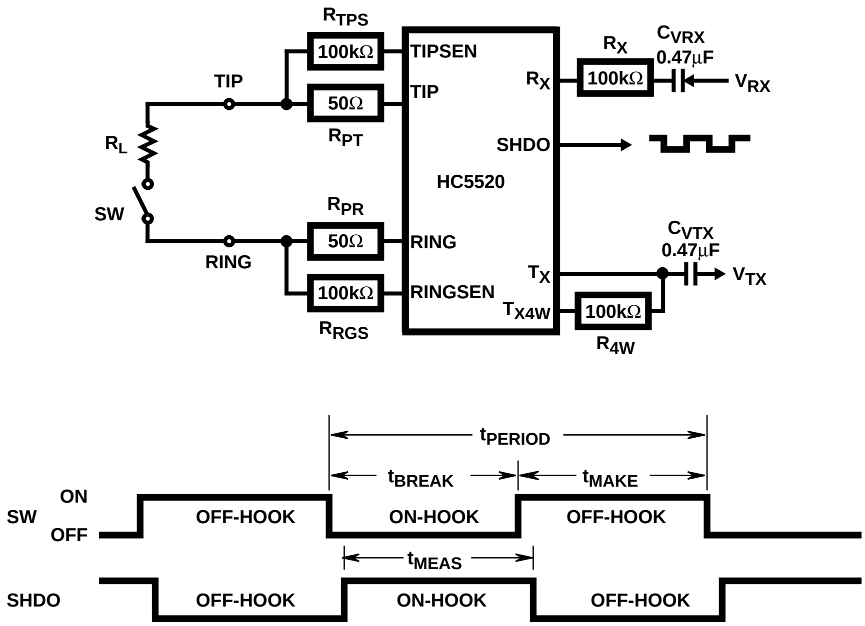


FIGURE 7. DIAL PULSE DISTORTION TEST CIRCUIT AND WAVEFORMS

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
Percent Break	SW = On, Off, . . .	t_{BREAK} and t_{PERIOD}	(t_{BREAK}/t_{PERIOD}) x 100%
Dial Pulse Distortion	SW = On, Off, . . .	t_{BREAK} and t_{PERIOD} and t_{MEAS}	Abs$[(t_{BREAK} - t_{MEAS})/t_{PERIOD}]$ x 100%

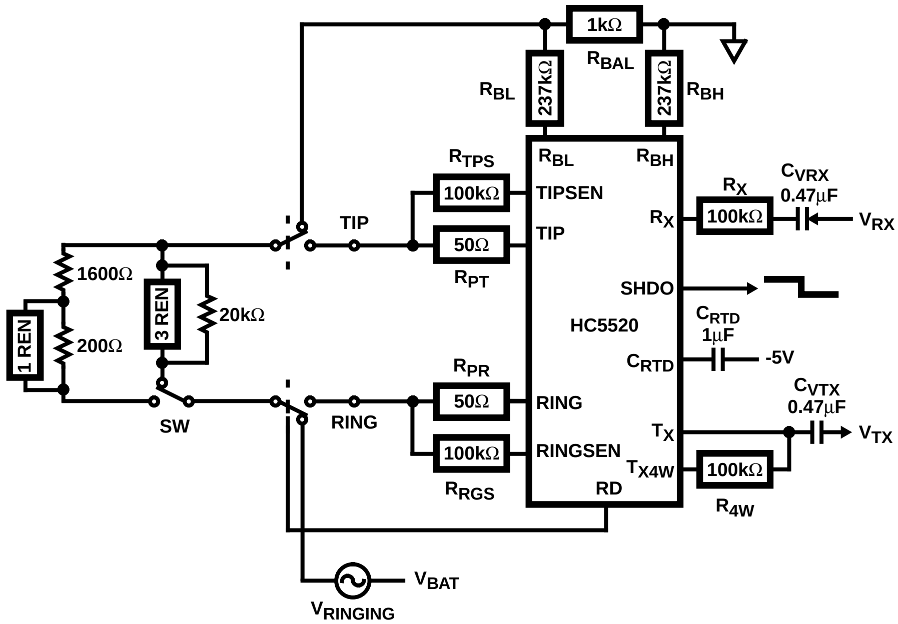


FIGURE 8. RING TRIP DETECTION TEST CIRCUIT

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
No Ring Trip Detection	SW = Up	SHDO	SHDO = Hi
Ring Trip Detection	SW = Down	SHDO	SHDO = Lo

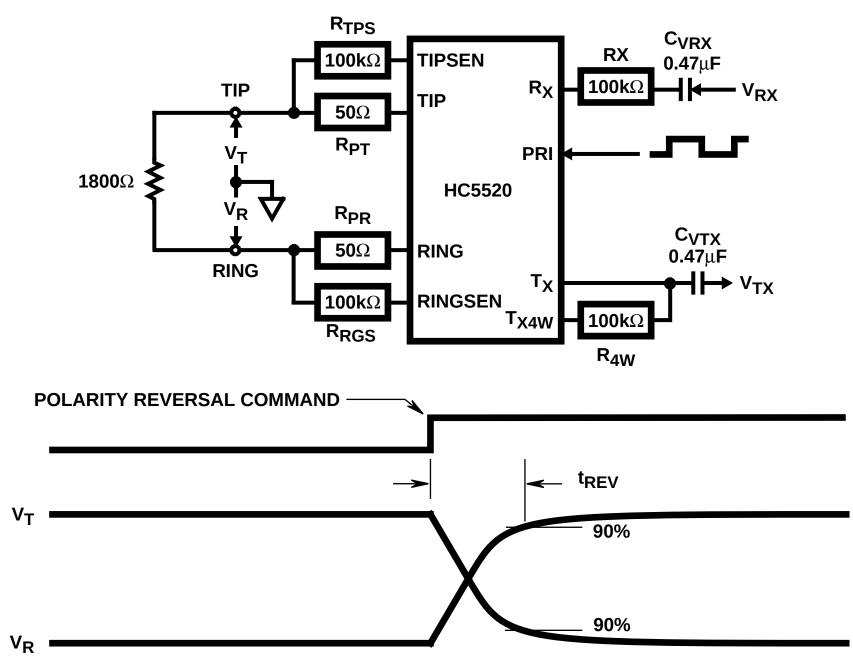


FIGURE 9. POLARITY REVERSAL TIME TEST CIRCUIT AND WAVEFORMS

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
Polarity Reversal Time	Reversal Command	t_{REV}	t_{REV}

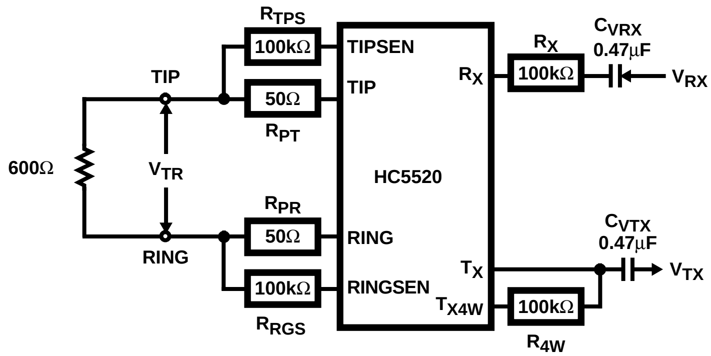


FIGURE 10. 4W TO 2W TRANSMISSION TEST CIRCUIT - NORMAL AND REVERSE MODES

PARAMETER	INPUT AT VRX	MEASUREMENT	SPECIFICATIONS AT 600Ω
Absolute Receive Gain, AGR	0dBm0 at 1020Hz	V_{TR} at 1020Hz	AGR = 20log(V_{TR}/V_{RX})
Receive Frequency Response	0dBm0 at Freq	V_{TR} at Freq	20log(V_{TR}/V_{RX}) - AGR
Receive Gain Tracking	Level at 1020Hz	V_{TR} at 1020Hz	20log(V_{TR}/Level) - AGR
Receive Signal to Distortion	Level at 1020Hz	V_{TR} at 2nd to 5th Harmonics	20log(Level/V_{TR})
Receive Idle Channel Noise	$0V_{RMS}$	V_{TR}	20log(V_{TR}/$0.7746V_{RMS}$)

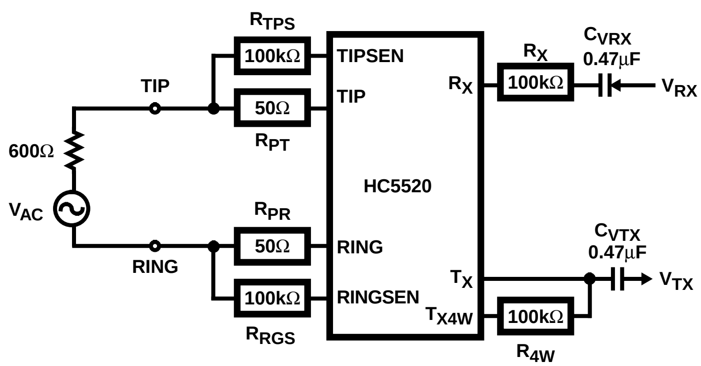


FIGURE 11. 2W TO 4W TRANSMISSION TEST CIRCUIT - NORMAL AND REVERSE MODES

PARAMETER	INPUT AT V_{AC}	MEASUREMENT	SPECIFICATIONS AT 600Ω
Absolute Transmit Gain, AGT	2x(0dBm0) at 1020Hz	V_{TX} at 1020Hz	AGT = 20log(V_{TX}/$0.7746V_{RMS}$)
Transmit Frequency Response	2x(0dBm0) at Freq	V_{TX} at Freq	20log(V_{TX}/$0.7746V_{RMS}$) - AGT
Transmit Gain Tracking	2x(Level) at 1020Hz	V_{TX} at 1020Hz	20log(V_{TX}/Level) - AGT
Transmit Signal to Distortion	2x(Level) at 1020Hz	V_{TX} at 2nd to 5th Harmonics	20log(Level/V_{TX})
Transmit Idle Channel Noise	$0V_{RMS}$	V_{TX}	20log(V_{TX}/$0.7746V_{RMS}$)

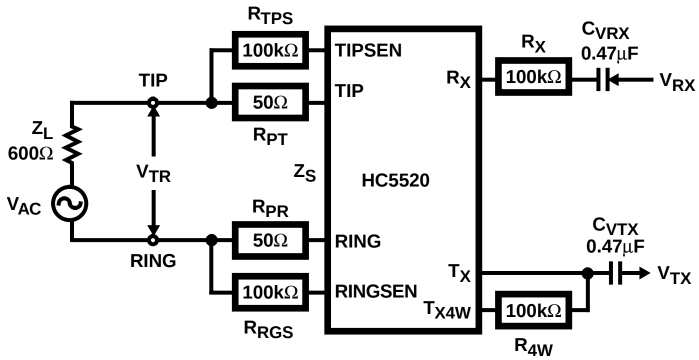


FIGURE 12. 2W RETURN LOSS TEST CIRCUIT - NORMAL AND REVERSE MODES

DEFINITION : 2W Return Loss = 20 log[(Z_S + Z_L) / Abs(Z_S - Z_L)]. Where Z_S is the source impedance and Z_L is the load impedance.

PARAMETER	INPUT AT V_{AC}	MEASUREMENT	SPECIFICATIONS FOR 600Ω
2W Return Loss	0dBm0 at Freq	V_{TR} at Freq	20log[V_{AC}/Abs(2xV_{TR} - V_{AC})]

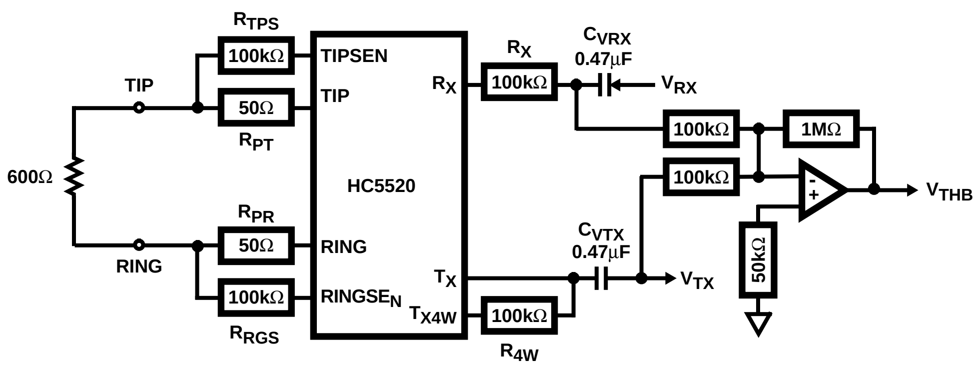


FIGURE 13. 4W TO 4W INSERTION LOSS AND TRANSHYBRID BALANCE - NORMAL AND REVERSE MODES

PARAMETER	INPUT AT V_{RX}	MEASUREMENT	SPECIFICATIONS FOR 600Ω
4W to 4W Insertion Loss	0dBm0 at Freq	V_{TX} at Freq	20log[V_{RX}/V_{TX}]
Transhybrid Balance	0dBm0 at Freq	V_{THB} at Freq	20log[V_{RX}/V_{THB}] + 20dB

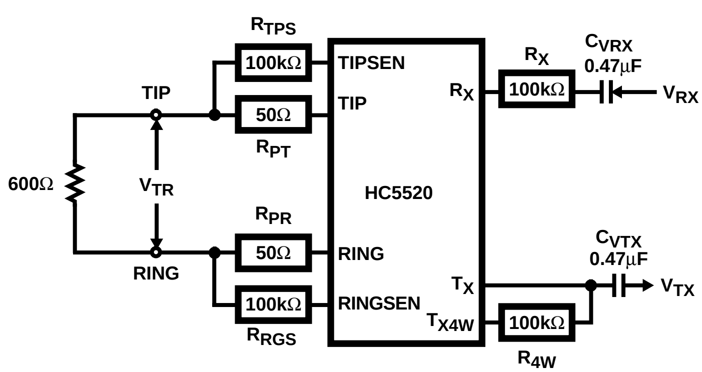


FIGURE 14. RECEIVE OVER LOAD LEVEL AT 4W AND 2W TEST CIRCUIT - NORMAL AND REVERSE MODES

INPUT AT VRX AT 1kHz	SLIC OUTPUT IMPEDANCE	SLIC VOLTAGE GAIN	MEASUREMENT	SPECIFICATION AT 600Ω
V_{RX} = 2.50V_{PEAK}	600Ω	0dB	V_{TR} at 2nd to 5th Harmonics	20log(V_{TR}/V_{RX})

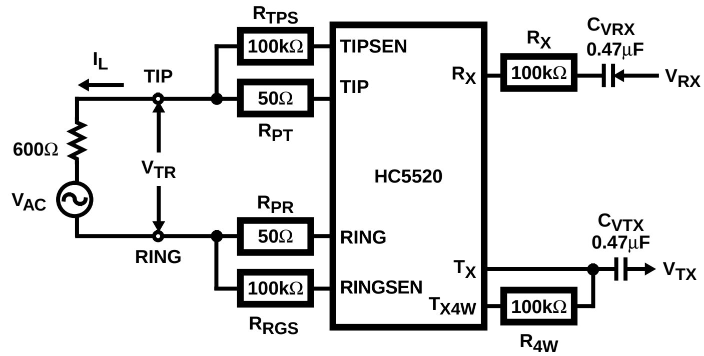


FIGURE 15. TRANSMIT OVER LOAD LEVEL AT 2W AND 4W TEST CIRCUIT - NORMAL AND REVERSE MODES

INPUT AT V_{AC} AT 1kHz	SLIC OUTPUT IMPEDANCE	SLIC TRANSMIT GAIN	MEASUREMENT	SPECIFICATION AT 600Ω
V_{AC} = 2x(2.15V_{PEAK})	600Ω	0dB	V_{TR} and V_{TX} at 2nd to 5th Harmonics	20log[V_{TR}/(V_{AC}/2)] and 20log[V_{TX}/(V_{AC}/2)]

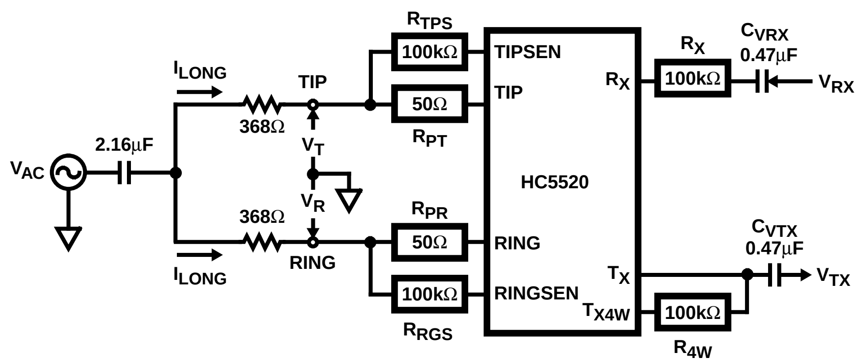


FIGURE 16. LONGITUDINAL IMPEDANCE TEST CIRCUIT - NORMAL AND REVERSE MODES

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
Longitudinal Impedance, Tip Side	V_{AC} = 0dBm0 at Freq	I_{LONG} (rms) and V_T (rms)	Z_{LONG} = V_T/I_{LONG}
Longitudinal Impedance, Ring Side	V_{AC} = 0dBm0 at Freq	I_{LONG} (rms) and V_R (rms)	Z_{LONG} = V_R/I_{LONG}

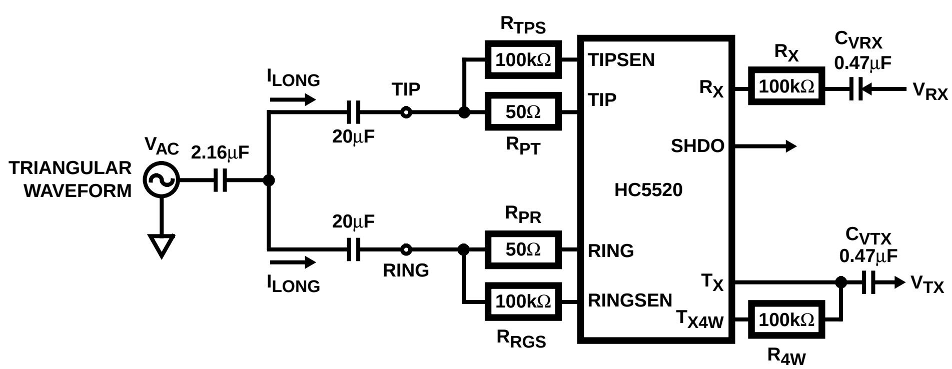


FIGURE 17. ON-HOOK LONGITUDINAL CURRENT LIMIT TEST CIRCUIT - NORMAL AND REVERSE MODES

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
Longitudinal Current Limit	V_{AC} at Freq, I_{LONG} = 15mA_{PEAK}	SHDO	SHDO = Hi

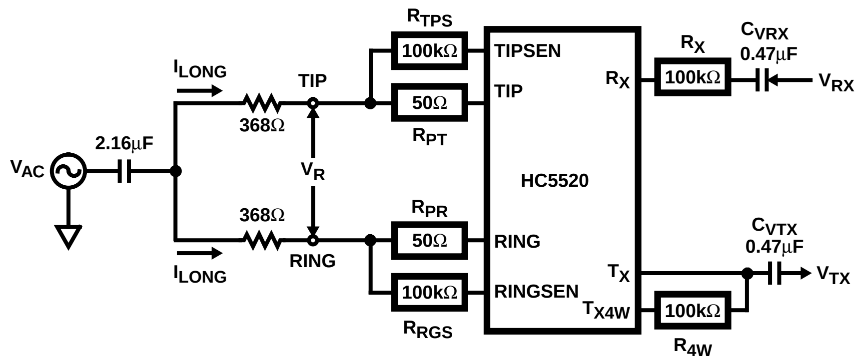


FIGURE 18. 2W AND 4W LONGITUDINAL BALANCE TEST CIRCUIT - NORMAL AND REVERSE MODES

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
2W Longitudinal Balance	V_{AC} = 0dBm0 at Freq	V_{TR} at Freq	$20\log(V_{AC}/V_{TR})$
4W Longitudinal Balance	V_{AC} = 0dBm0 at Freq	V_{TX} at Freq	$20\log(V_{AC}/V_{TX})$

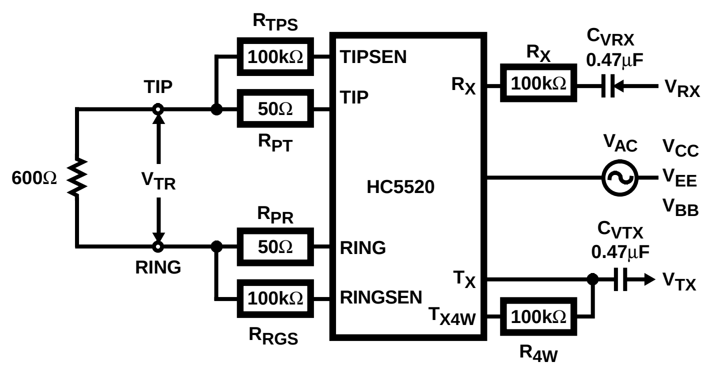


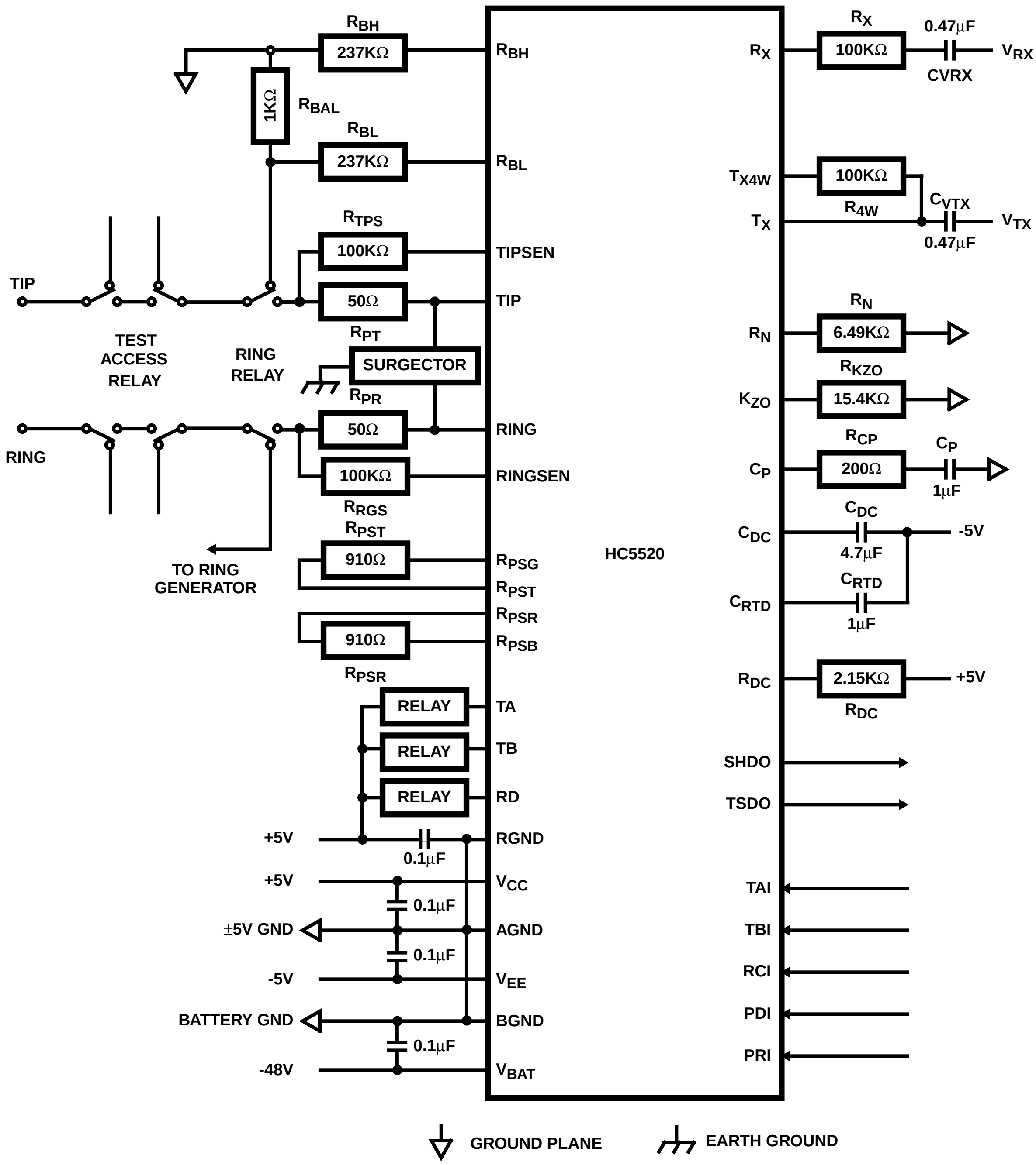
FIGURE 19. OFF HOOK PSRR 4W AND 2W TEST CIRCUIT - NORMAL AND REVERSE MODES

PARAMETER	INPUT	MEASUREMENT	SPECIFICATIONS
PSRR V_{BAT} to 4W	V_{BAT} = -48V + V_{AC}	V_{TX} at Freq	$20\log(V_{AC}/V_{TX})$ at Freq
PSRR V_{BAT} to 2W	V_{BAT} = -48V + V_{AC}	V_{TR} at Freq	$20\log(V_{AC}/V_{TR})$ at Freq
PSRR V_{CC} to 4W	V_{CC} = +5V + V_{AC}	V_{TX} at Freq	$20\log(V_{AC}/V_{TX})$ at Freq
PSRR V_{CC} to 2W	V_{CC} = +5V + V_{AC}	V_{TR} at Freq	$20\log(V_{AC}/V_{TR})$ at Freq
PSRR V_{EE} to 4W	V_{EE} = -5V + V_{AC}	V_{TX} at Freq	$20\log(V_{AC}/V_{TX})$ at Freq
PSRR V_{EE} to 2W	V_{EE} = -5V + V_{AC}	V_{TR} at Freq	$20\log(V_{AC}/V_{TR})$ at Freq

Pin Descriptions

MQFP	PLCC	SYMBOL	DESCRIPTION
1	7	R_X	4W receive input pin, a ground referenced current sense input.
2	8	AGND	Analog ground pin. This pin must be tied to the BGND and RGND pins.
3	9	T_X	4W transmit output pin, a ground referenced voltage source.
4	10	T_{X4W}	Transmit gain setting pin - connecting a resistor between T_{X4W} and T_X establishes the 2W to 4W gain.
5	11	K_{ZO}	2W impedance setting pin, connecting a network $K(Z_L)$ between K_{ZO} pin and AGND will program the 2W impedance to be Z_L.
6	12	R_N	Resistor divider pin for ZO, in conjunction with K_{ZO} it defines the 2W impedance.
7	13	R_{DC}	DC feed reference pin.
8	14	C_{DC}	DC feeding circuit low pass filter capacitor pin.
9	15	C_P	Half battery voltage reference pin.
10	16	V_{EE}	Negative power supply pin, V_{EE} = -5V at 5%.
11	17	TIPSEN	Tip sense input pin.
12	18	BGND	Battery ground pin. This pin must be tied to the AGND and RGND pins.
13	19	R_{PSG}	Power sharing resistor ground side connection pin.
14		NC	No connect.
15	20	R_{PST}	Power sharing resistor Tip side connection pin.
16	21	TIP	Tip feed pin.
17	22	NC	No connect.
18	23	RING	Ring feed pin.
19	24	R_{PSR}	Power sharing resistor Ring side connection pin.
20	25	NC	No connect.
21	26	R_{PSB}	Power sharing resistor battery side connection pin.
22	27	V_{BAT}	Battery power supply pin, V_{BAT} = -42V to -58V.
23	28	RINGSEN	Ring sense input pin.
24	29	R_{BH}	Ring trip amplifier ground side sense input pin.
25	30	R_{BL}	Ring trip amplifier line side sense input pin.
26	31	C_{RTD}	Ring trip capacitor pin.
27	32	RD	Ring relay driver pin, open collector output. Diode protected internally.
28	33	TB	Test access relay driver pin, open collector output. Diode protected internally.
29	34	TA	Test access relay driver pin, open collector output. Diode protected internally.
30	35	RGND	Relay driver ground current return pin. This pin must be tied to the AGND and BGND pins.
31	36	V_{CC}	Positive power supply pin, V_{CC} = +5V at 5%.
32	37	NC	No connect.
33	38	NC	No connect.
34	39	NC	No connect.
	40	NC	No connect.
35	41	TAI	TA Relay Driver Control Input.
36	42	TBI	TB Relay Driver Control Input.
37	43	RCI	RD Relay Driver Control Input.
38	44	PRI	Loop Feed Polarity Control Input.
39	1	PDI	Loop Feed Control Input.
40	2	NC	No connect.
41	3	NC	No connect.
42	4	TSDO	Thermal Shutdown Indicator Output.
43	5	SHDO	Off Hook Detect Indicator Output.
44	6	NC	No connect.

Typical Application Circuit Diagram

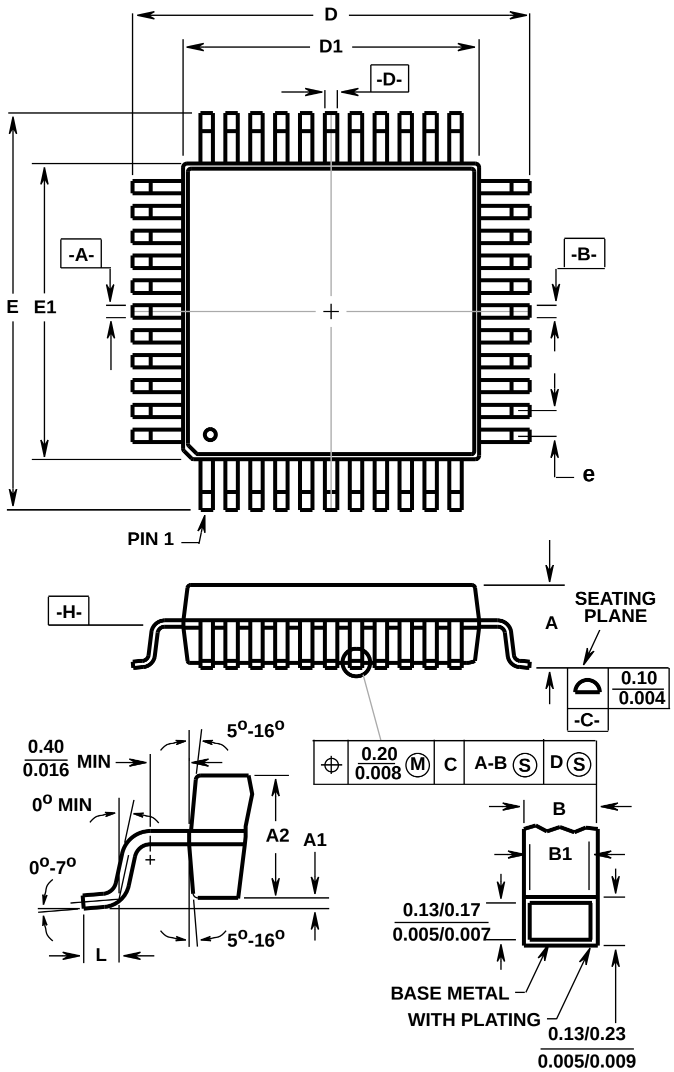


NOTE: The HC5520 application circuit is configured to provide a receive gain of 0dB, a transmit gain of 0dB, and a synthesized 2W impedance of 593Ω. Note, the value of R_{TPS}, R_{RGS} should always be selected to be 100kΩ.

External Component List for Application Circuit

NAME	VALUE	TOLERANCE	RATING
R_X, R_{4W}, R_{TPS}, R_{RGS}	100kΩ	1%	1/10W
R_N	6.49kΩ	1%	1/10W
R_{DC}	2.15kΩ	1%	1/10W
R_{BH}, R_{BL}	237kΩ	1%	1/10W
R_{PT}, R_{PR}	50Ω	5%	2.5W or PTC
R_{BAL}	1000Ω	5%	1W
R_{KZ0}	15.4kΩ	1%	1/10W
R_{CP}	200Ω	5%	1/10W
R_{PST}, R_{PSR}	910Ω	5%	2W
C_{VRX}, C_{VTX}	0.47µF	20%	10V
C_{DC}	4.7µF	10%	10V Tantalum
C_P	1µF	10%	35V Tantalum
C_{RTD}	1µF	10%	10V Tantalum
C DECOUPLING	0.1µF	20%	10V except on Vb
SURGECTOR	TISP1072F3SL		Texas Instruments
PTC	TR250-120u		Raychem

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q44.10x10 **(JEDEC MO-108AA-2 ISSUE A)**

44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

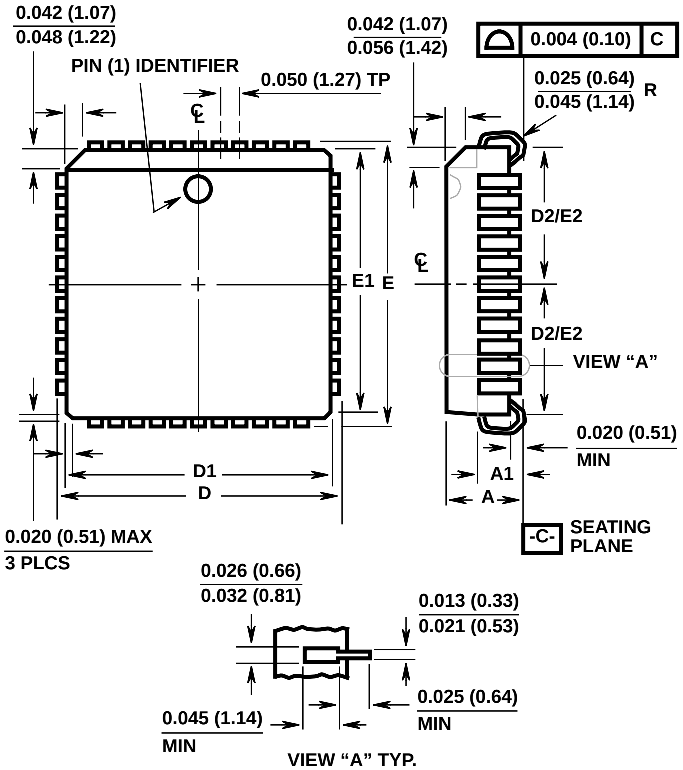
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 1 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C- .
4. Dimensions D1 and E1 to be determined at datum plane -H- .
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. “N” is the number of terminal positions.

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